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Investigation of temperature variations on a Class-E inverter and proposing a compensation circuit to prevent harmful effects on biomedical implants

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In this paper, a Class-E inverter and a thermal compensation circuit for wireless power transmission in biomedical implants are designed, simulated, and fabricated. In the analysis of the Class-E inverter, the voltage-dependent non-linearities of C_{ds}, C_{gd}, and R_{ON} as well as temperature-dependent non-linearity of R_{ON} of the transistor are considered simultaneously. Close agreement of theoretical, simulated and experimental results confirmed the validity of the proposed approach in taking into account these nonlinear effects. The paper investigated the effect of temperature variations on the characteristics of the inverter. Since both the output power and efficiency decrease with increasing temperature, a compensation circuit is proposed to keep them constant within a wide temperature range to enable its application as a reliable power source for medical implants in harsh environments. Simulations were performed and the results confirmed that the compensator enables significant improvements by maintaining the power and efficiency almost constant (8.46 ± 0.14 W and 90.4 ± 0.2%) within the temperature range of − 60 to 100 °C. Measurements performed at 25 °C and 80 °C with and without the compensation circuit were in good agreement with the theoretical and simulation results. The obtained measured output power and efficiency at 25 °C are equal to 7.42 W and 89.9%.

Today, wireless technology plays an important role in the development of Health informatics. The convenience of patients under treatment, diagnosing the disease with the least side effects and the accuracy of test results are important concerns of scientists in this field. Wireless technology is used in biomedical sensors, artificial organs, and remote monitoring of the patients' condition[1–3]. Figure 1 shows some examples of implants that integrate wireless technology for therapeutic applications. The illustrated implants work at different frequencies and are designed according to their function in different parts of the body[4–9]. Class-E Power Amplifier (PA) or inverter is the main component of WPT[11]. In design and analysis of Class-E power amplifier, the effects of input voltage waveforms[12], duty ratio[13], and parasitic linear and nonlinear capacitances[14] have been discussed. Also, comprehensive research projects have been conducted to improve the characteristics of PAs in different classes for biomedical industry[15] One of the important issues in the manufacture of biomedical implants is availability of reliable wireless power supplies and this paper is focused on this matter specially with regards to operation in harsh environments.

The Class-E inverter has been welcomed due to its high efficiency, circuit simplicity, and small size and therefore it has been the main element of practical circuits such as biomedical implants[16,17], inverters[18–20], WPT systems[21–26], oscillators[23,28], and light communication transmitter[29]. Due to these broad applications, a variety of techniques have also been used to design and optimize class E inverters for different WPT applications. As an example, in Inductive Power Transfer (IPT) WPT, due to the displacement of the transmitter and receiver coils, as well as the displacement of the alignment between them, the values of the output resistance and inductance of the inverter changes. To avoid the effects of these changes, frequency modulated control[24] and load independent class E inverter[25,26] have been presented. The load-independent Class-E inverter achieves constant output voltage,

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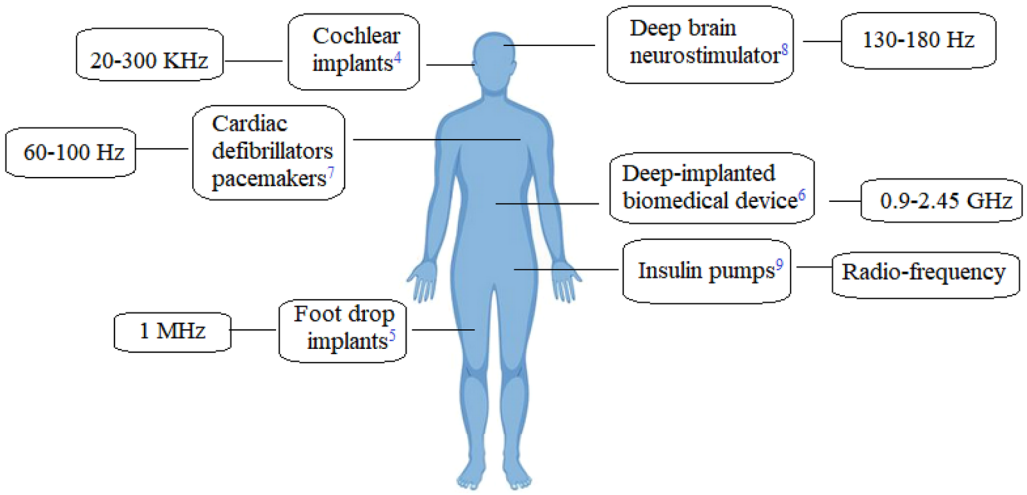

Figure 1. Some of the therapeutic implants which are supplied with WPT[10].

ZVS, and fixed phase shift between the driving signal and the output voltage at any load resistance without any control[24].

Another approach is to merge Class-E PAs with other classes, which results in mixed-mode PAs such as class D_{EM}[30] and class E_M/F_n[31]. The robust and efficient wireless power transfer and the floating bulk technique achieved by using a power-efficient Class-E power amplifier have also been investigated[32,33]. In one research[34], a study of the temperature effect on the MOSFET biased in the subthreshold region is presented. In another work two Class-E PAs with transmission line (TL), lumped elements[35], and a Class-E PA with two cascaded transistors[36] have been studied. The design of the Class-E PA considering the non-linear drain-source and linear gate-drain capacitances have also been studied[12,37,38] In a recent work[39], the temperature effect on the Class-E PA has been investigated where the effect of temperature has been compensated by DC gate-source voltage, despite its undesired influence on the transistor bias region, also only the drain-source resistor of the transistor is considered as a linear element and the effect of nonlinear capacitors is completely neglected. This is while, the need to consider these capacitors in the analysis has already been thoroughly proven[40]. Studying the effects of temperature changes on WPT transmitters while also considering the simultaneous effect of nonlinear capacitances and on-state resistance is a missing challenge of research, which is the main aim of this paper. We have then proceeded to propose a compensation circuit which does not adversely affect the bias of the MOSFET and aims to exceed the performance of the previous approach. This is done with the objective of maximizing the operating temperature range of the inverter as defined by its power level and efficiency. In this paper, it is shown that the output power and efficiency decrease with increasing temperature. The change in temperature also changes the drain-source voltage, which it may exceed the maximum withstand voltage of the transistor and as a result, the transistor can be damaged in the circuit. This condition would be worse if we had a MOSFET with a large R_{ON}. In medical implants, providing a reliable power source is one of the designers' issues. A compensation circuit is proposed in this paper to keep output power and efficiency constant within a wide temperature range in order to enable its application as a reliable power source for medical implants in harsh environments.

This paper is categorized as follows; discussion of the design block diagram and design specification, presentation of the proposed analysis for the Class E Inverter considering the voltage-dependent non-linearities of Cds, Cgd, and R_{ON} as well as temperature-dependent non-linearity of R_{ON} of the transistor and investigating temperature variation effects, introducing the class-E inverter with the proposed thermal compensation circuit, and finally presentation and discussion of the measurement results and a conclusion.

Proposed methodology

Design block diagram and design specification. The proposed block diagram of a WPT used in biomedical implants is shown in Fig. 2. Due to the high efficiency of switching inverters, they are used in the wireless power supply system in the power transmitter part. In wireless implants, the transmitter induces the required power into the implant circuit with an inductive couple that transmits the power through the coils. In the receiver part of the body, a rectifier and a regulator are utilized to create the required power. The presented circuit of a WPT is shown in Fig. 3.

Class E inverter is used in many WPTs due to its simplicity of structure and high efficiency at the operating frequency. The important elements of the Class E inverter circuit are the MOSFET, which acts as a switch, a resonant circuit at the desired operating frequency, and an external capacitor. In a class E inverter, the transistor is biased in the cut-off region, with a sufficient gate driving amplitude to make it to operate alternatively between the cut-off and the linear region. Nonlinear elements of the transistor include the drain-source capacitor and the gate-drain capacitor, which have a non-linear voltage dependence. The drain-source on-resistor has a nonlinear temperature dependence. The output series resonance circuit followed by a phase difference inductor is designed to produce the output signal at the operating frequency with the lowest power loss. A choke is used between the

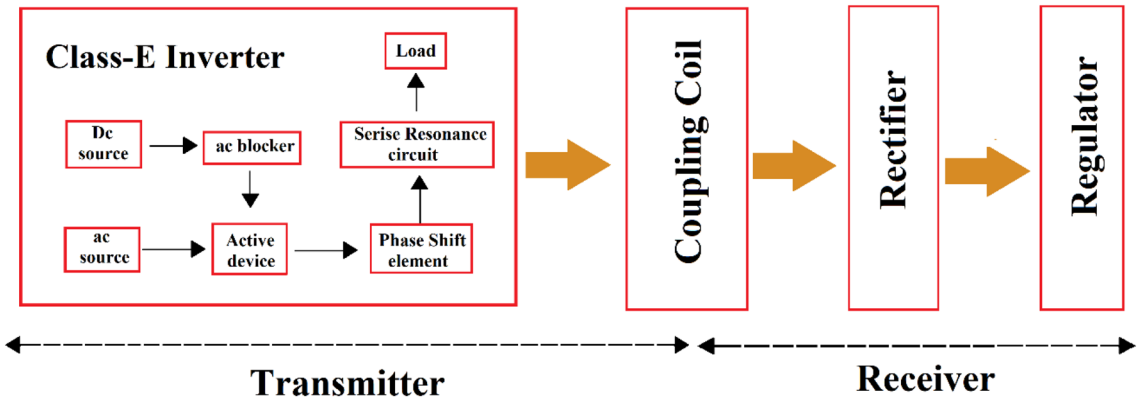

Figure 2. The proposed block diagram of a WPT in biomedical implants.

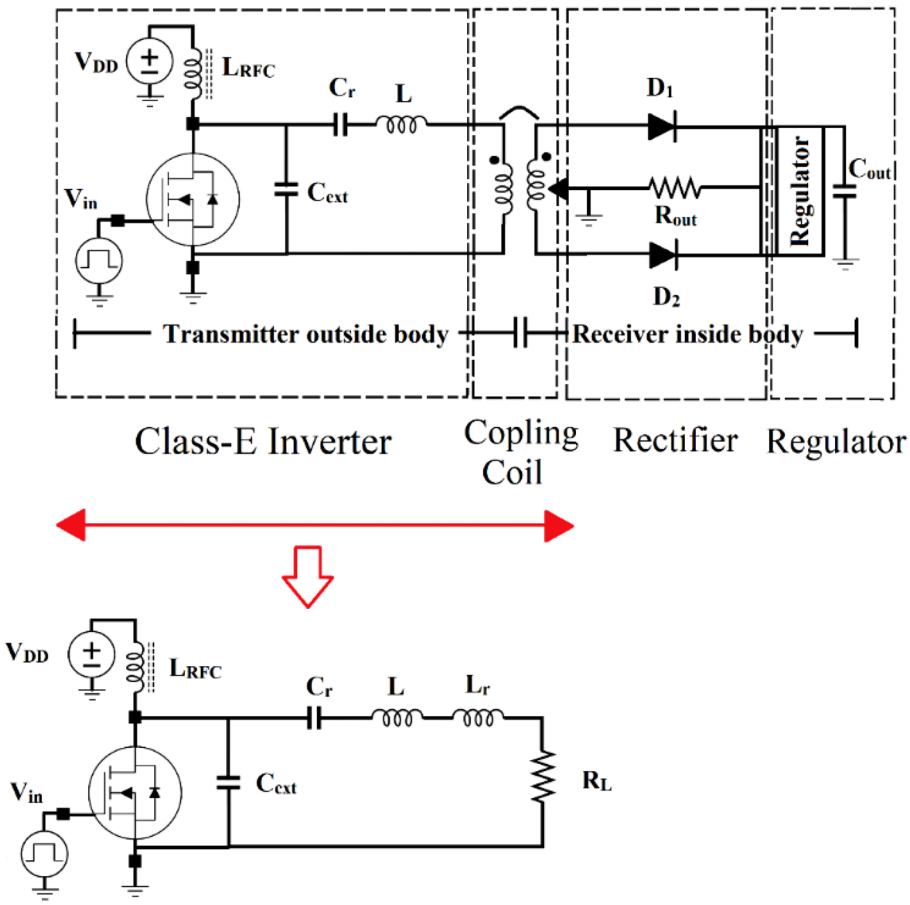

Figure 3. The presented circuit of a WPT is used in biomedical implants.

drain of the transistor and the power supply to create low-ripple DC current and isolate ac signals from DC. In most designs, the transistor is considered an ideal switch, which is modeled as a short circuit in the ON-state and as an open circuit in the OFF-state, but in the ON-state, the transistor has a resistance that depends on the transistor parameters.

Transistor temperature dependency. All passive and active elements have internal resistance, considering this resistance in the design process causes theoretical and fabricated responses to be in good agreement with each other. The most dependence of the transistor on the temperature is related to this resistance, which is tied to the drain-source. In switching inverters, the transistor operates in the triode region in the ON-state and operates in the cut-off region in the OFF-state. The relation of the transistor current in the triode region is defined as[41]:

$$i_T = \mu_n C_{ox} \frac{W}{L}\left[(V_{GS} - V_{th})V_{DS} - \frac{1}{2}V_{DS}^2\right] \tag{1}$$

In the deep triode region, $V_{DS} \leq 2(V_{GS} - V_{th})$, it can be obtained:

$$i_T \approx \mu_n C_{ox} \frac{W}{L}[(V_{GS} - V_{th})V_{DS}] \tag{2}$$

The relationship of the ON-state drain-source resistance can be presented as[41]:

$$R_{ON} = \frac{1}{\mu_n C_{ox} \frac{W}{L}[(V_{GS} - V_{th})]} \tag{3}$$

where i_T is the transistor current, V_{GS} is the gate-source voltage, V_{DS} is the drain-source voltage, μ_n is mobility, V_{th} is the threshold voltage, and C_{ox} is the oxide capacitor per unit area. W is 100u and L is 100u for IRF510. In (3), μ_n and V_{th} are temperature-dependent parameters that lead to the temperature dependence of ON-state drain-source resistance. Firstly, the effect of temperature variations on V_{th} is investigated. V_{th} is obtained as[42]:

$$V_{th} = 2\emptyset_F + \frac{\sqrt{2\varepsilon_{si} q N_a (2\emptyset_F)}}{C_{ox}} \tag{4}$$

where q is the electron charge and N_a is the acceptor doping density, ε_{si} is the dielectric constant of the semiconductor and $2\varnothing_F$ is twice the bulk potential. Where for the P substrate, the bulk potential is obtained as follows[42]:

$$\emptyset_F = V_T ln \frac{N_a}{n_i} \tag{5}$$

V_T is the thermal voltage and n_i is the intrinsic carrier density. The V_T and n_i depend on temperature and are described as follows[42]:

$$V_T = \frac{KT}{q} \tag{6}$$

$$n_i = \sqrt{N_C N_v} e^{-E_g/2KT} \tag{7}$$

N_C is the Effective density of states in the conduction band, N_v is the Effective density of states in the valence band, E_g is the semiconductor Energy bandgap, and K is Boltzmann's constant. The energy bandgap of a semiconductor is related to temperature and is expressed as follows[42]:

$$E_g(T) = -E_g(0) - \frac{\alpha T^2}{T + \beta} \tag{8}$$

By substituting (6), (7), and (8) in (5), the $\varnothing_F$ is obtained by[42]:

$$\emptyset_F = \frac{KT}{q} ln \frac{N_a}{\sqrt{N_C N_v} e^{-E_g(0) - \frac{\alpha T^2}{T+\beta}/2KT}} \tag{9}$$

Mobility is the second parameter that depends on the temperature. Mobility decreases with increasing temperature with coefficient $T^{-2.4}$ and is defined as below[42]:

$$\mu_n = \mu_{n0} T^{-2.4} \tag{10}$$

where μ_{n0} varies based on the amount of silicon impurity. By substituting all the parameters in (3), the equation of resistance based on temperature is obtained as:

$$R_{ON} = \frac{1}{\mu_{n0} T^{-2.4} C_{ox} \frac{W}{L}\left[\left(V_{GS} - 2\frac{KT}{q} ln \frac{N_a}{\sqrt{N_C N_v} e^{\left(-E_g(0) - \frac{\alpha T^2}{T+\beta}\right)/2KT}} + \frac{\sqrt{2\varepsilon_{si} q N_a 2\frac{KT}{q} ln \frac{N_a}{\sqrt{N_C N_v} e^{\left(-E_g(0) - \frac{\alpha T^2}{T+\beta}\right)/2KT}}}}{C_{ox}}\right)\right]} \tag{11}$$

The constant parameters for silicon in (11) are defined as below[42]:

$$\alpha = 0.473 \frac{\text{meV}}{\text{K}} \quad \beta = 636\,\text{K} \quad E_g(0) = 1.166\ \text{eV}$$

Temperature changes are caused by changes in ambient temperature and junction temperature, which causes power dissipation in the transistor. It can be seen from (11), R_{ON} is a function of V_{th} and mobility, which decreases with increasing temperature.

Figure 4 shows the dependence of V_{th} and mobility as a function of temperature for IRF510 transistor. The change of R_{ON} based on temperature variations when $V_{GS} = 5.2$ V is shown in Fig. 5. R_{ON} has an increasing trend with increasing temperature.

Presented analysis for the class E inverter. Figure 6 shows the equivalent of the simple class E (SCE) inverter circuit which consists of:

- The transistor considers the nonlinear capacitances (C_{ds} and C_{gd}).
- R_{ON} is the resistance of the transistor ON-state.
- C_{ext} is the fixed external capacitor.
- L_{RFC} is used as the ac blocker.
- R_{RFC} is the resistance of the $L_{RFC.}$
- L acts as a phase difference inductor.
- R_{L0} is the resistance of $L + Lr$.
- $C_r + L_r$ just passes the first harmonic and blocks other harmonics.

The element values and specifications of the class E inverter in − 60 °C ~ 180 °C temperature ranges are obtained by numerical solution according to ZVS and ZVDS conditions including nonlinear R_{ON}, C_{ds}, and C_{gd}. Figure 7 shows a block diagram of the design process and methodology that is used. In the design, the input parameters are operating frequency, peak output current I_m, external capacitances C_{ext}, and chock inductance L_{RFC}, which are known. Also, the output parameters are L, L_r, C_r, R_L, V_{DD}, efficiency, output power, V_{d-ON}, V_{d-ON}, and I_{DC}, which are obtained according to the temperature variation.

A square pulse with a duty cycle of 50% is applied to the gate transistor. When the transistor is OFF ($0 < \Theta < \pi$), the gate-source voltage is zero, leaving only the nonlinear capacitors of the transistor. The following relationship can be presented:

$$Transistor\ off \rightarrow -I_{DC} + \sum_{n=1}^{\infty} I_{mn} \sin(n\theta + \varphi_n) + \omega\left(C_{ext} + C_{ds} + C_{gd}\right)\frac{dV_{d-OFF}}{d\theta} = 0 \qquad (12)$$

In (12), V_{d-OFF} is the drain-source voltage in the OFF-state, I_{DC} is the DC current injected from V_{DD}, and because of L_{RFC} operation, this current has a very little ripple. I_{mn} is the nth harmonic peak of the output current. The nonlinearity of transistor capacitors (C_{ds} and C_{gd}) are considered for more accuracy in the design and their relationship is as follows[38]:

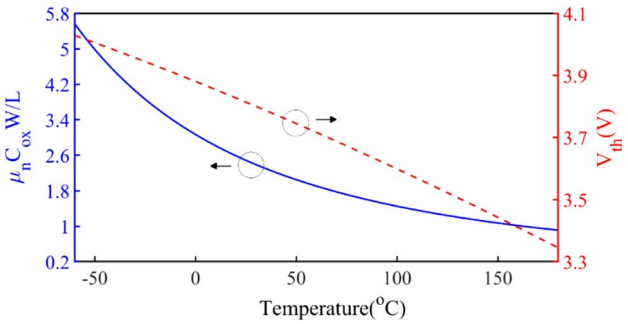

Figure 4. The dependence of V_{th} and mobility as a function of temperature for the IRF510 transistor.

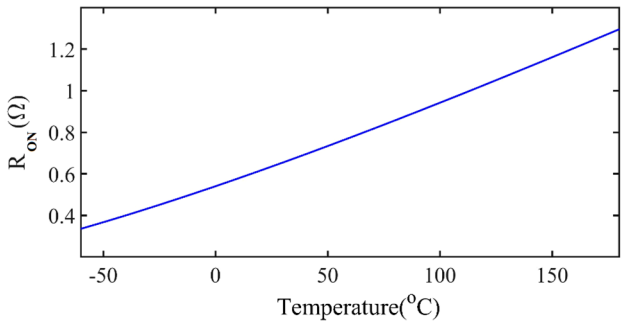

Figure 5. The dependence of R_{ON} as a function of temperature for the IRF510 transistor when VGS = 5.2 V.

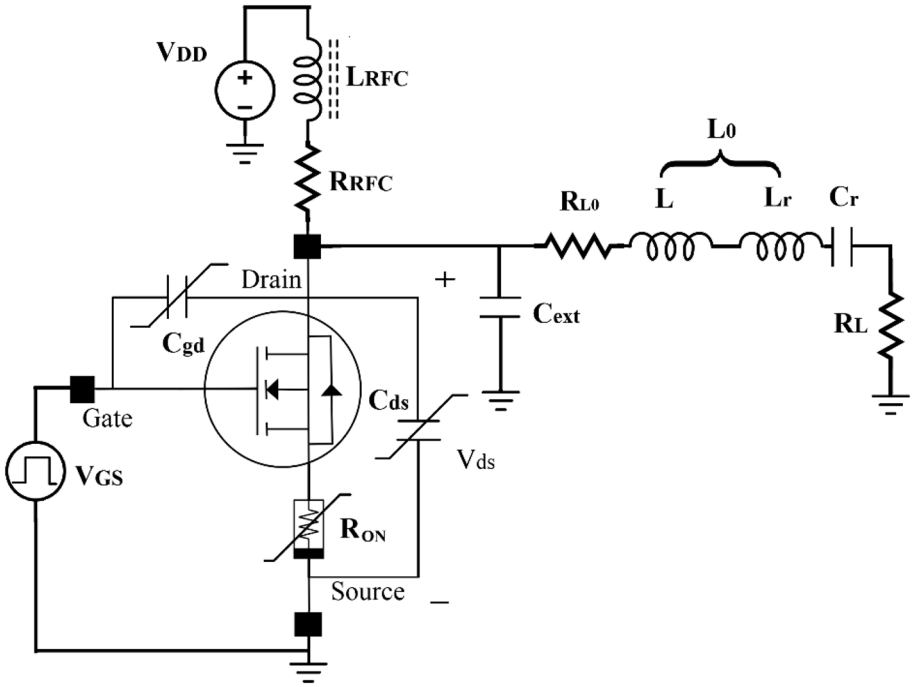

Figure 6. The equivalent circuit of the simple class E (SCE) inverter circuit.

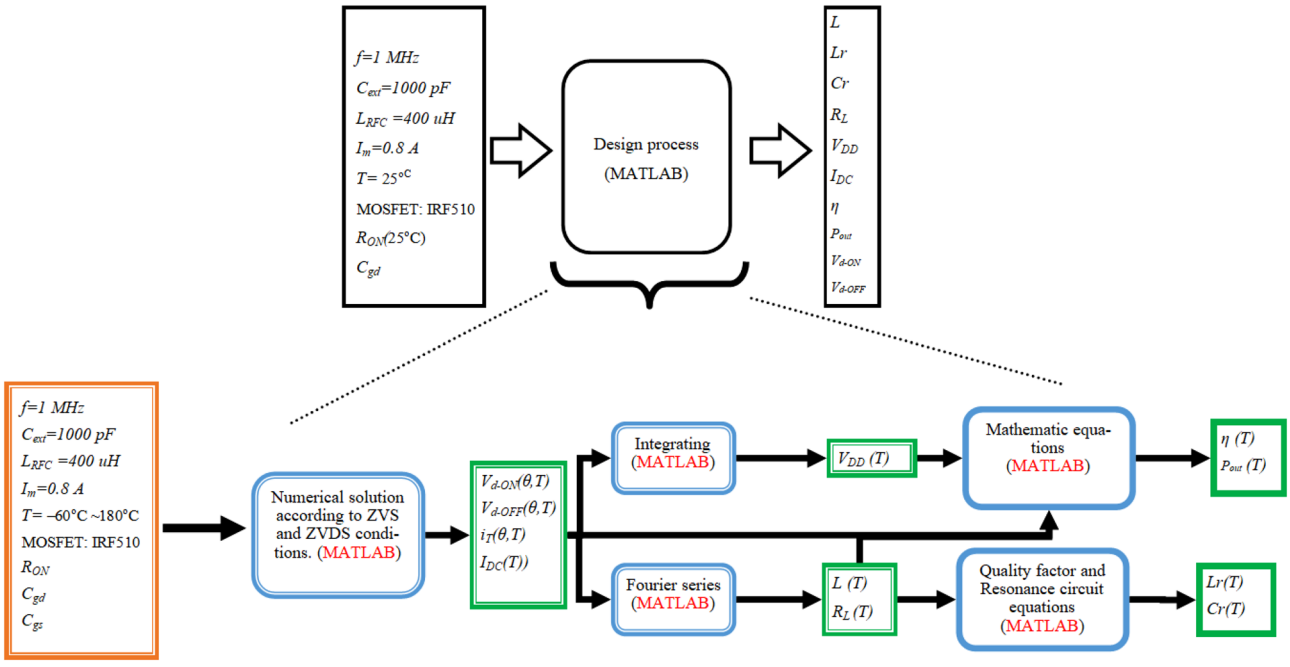

Figure 7. Block diagram of the Presented Analysis for the Class E Inverter.

$$C_{ds} = \frac{C_{j01}}{\left(1 + \frac{V_{d-OFF}}{V_{bi_1}}\right)^{m_1}},\ C_{gd} = \frac{C_{j02}}{\left(1 + \frac{V_{d-OFF}}{V_{bi_2}}\right)^{m_2}} \tag{13}$$

where V_{d-OFF} is the drain-to-source transistor voltage in the OFF-state, V_{bi1} and V_{bi2} are the built-in voltage of the pn junction, C_{j01} is the drain-to-source capacitance at V_{d-OFF}, C_{j02} is the gate-to-drain capacitance at V_{d-OFF}, m_1 is the grading coefficient for the nonlinear drain-to-source capacitance and m_2 is the grading coefficient for the nonlinear gate-to-drain capacitance. By substituting (13) in (12) and integrating from θ we have:

$$\frac{\omega C_{j01} V_{bi1}}{1-m_1}\left[\left(1+\frac{V_{d-OFF}}{V_{bi1}}\right)^{1-m_1}-1\right]+\frac{\omega C_{j02} V_{bi2}}{1-m_2}\left[\left(1+\frac{V_{d-OFF}}{V_{bi2}}\right)^{1-m2}-1\right]+\omega C_{ext} V_{d-OFF} = I_{DC}\theta+\sum_{n=1}^{\infty}\frac{I_{mn}}{n}[\cos(n\theta+\varphi_n)-\cos(\varphi_n)] \tag{14}$$

The parameters of IRF510 MOSFET are listed in Table 1[43].

When the transistor is ON ($\pi<\Theta<2\pi$), the gate-source voltage is high, R_{ON} impact is added to the structure. i_T is the current passing through the transistor. This current is considered zero when the transistor is in OFF-state due to the high resistance of the transistor. By utilizing the current division in the drain node, the below equation can be obtained:

$$i_T = I_{DC}-\sum_{n=1}^{\infty} I_{mn}\sin(n\theta+\varphi_n)\times\frac{Z_{C_{ds}} IIZ_{C_{gd}} IIZ_{C_{ext}}}{Z_{C_{ds}} IIZ_{C_{gd}} IIZ_{C_{ext}}+R_{ON}} \tag{15}$$

where 'Z' and 'II' mean impedance and parallel, respectively.

The ZVS and ZVDS conditions are applied to the transistor voltage to avoid overlap between voltage and current at π. These conditions create minimal consumption in the design. Applying these conditions to Eqs. (12) and (15):

$$ZVDS \rightarrow \frac{dV_{d-OFF}(\pi)}{d\theta}=0 \rightarrow -I_{DC}+\sum_{n=1}^{\infty}(-1)^n I_{mn}\sin(\varphi_n)=0 \tag{16}$$

$$ZVS=0 \rightarrow V_{d-OFF}(\pi)=0 \rightarrow I_{DC}\pi+\sum_{n=1}^{\infty}\frac{I_{mn}}{n}\left[(-1)^n-1\right]\cos(\varphi_n)=0 \tag{17}$$

The output resonance circuit of the transistor is designed with high-quality factor, so only the first harmonic is considered in the design and the rest of the harmonics are ignored. Therefore, according to (16) and (17), the amount of phase difference required to meet the conditions of ZVS and ZVDS is equal to $\varphi_n = -0.567$ rad. Figure 8 shows the drain voltage at 25 °C as well as determines the drain voltage peak value in the ON and OFF states. It can be seen that the drain voltage in the ON-state has a significant value, but it has been neglected in previous class E inverter designs.

The drain voltage in the ON-state according to R_{ON} can be obtained as below:

$$V_{d-ON} = i_T \times R_{ON} \tag{18}$$

where i_T is the current of the transistor in ON-state, which is presented in (15).

The voltage of the DC power supply according to the drain voltage can be obtained. 0 to π indicates the OFF-state, and π to 2π indicates the ON-state of the transistor, V_{DD} can be calculated as follows:

Parameters	C_{j01} (pF)	V_{bi1} (V)	m_1	C_{j02} (pF)	V_{bi2} (V)
Value	298	0.774	0.423	185	0.5
Parameters	m_2	V_{th} (V)	$\mu_n C_{ox}$	W (μm)	L (μm)
Value	0.651	3.82703	2.48457	100	100

Table 1. Parameters of the IRF510 MOSFET.

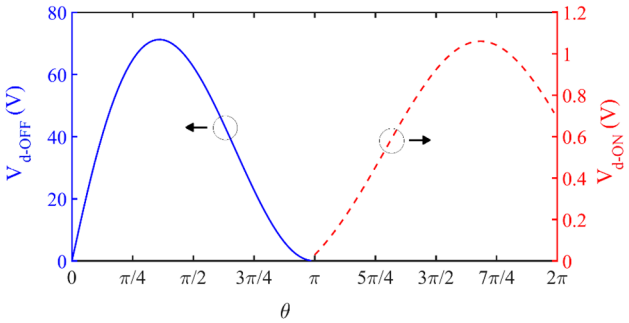

Figure 8. V_d in on and OFF-states versus Θ.

$$V_{DD} = \frac{1}{2\pi}\left[\int_0^{\pi} V_{d-OFF}(\theta)d\theta + \int_{\pi}^{2\pi} V_{d-ON}(\theta)d\theta\right] + R_{RFC}I_{DC} \tag{19}$$

To have a constant output current with ZVS and ZVDS conditions versus temperature changes, the circuit parameters like V_{DD}, L_r, C_r, L, and R_L must be changed. According to (19), V_{DD} versus temperature changes is obtained and shown in Fig. 9.

As temperature increases, V_{DD} should be increased to compensate for the drop in drain voltage in the OFF-state. Figure 10a shows the output resonant circuit. At the fundamental harmonic, which is considered to be 1 MHz, the resonant circuit is simplified, as shown in Fig. 10a. By employing KVL in the circuit:

$$-V_{d-OFF}H1 + V_{R_{L0}} + V_L + V_o = 0 \tag{20}$$

In (20), $V_{d-OFF}H1$ is the first harmonic of V_{d-OFF}, V_L is the phase difference inductor voltage, V_O is the output voltage, and $V_{R_{L0}}$ is the R_{L0} voltage. By substituting the first harmonic of the out current in (20):

$$-V_{d-OFF}H1 + R_{L0} \times I_{m1}\sin(\theta + \varphi_1) + 2\pi f \times L \times I_{m1}\cos(\theta + \varphi_1) + R_L \times I_{m1}\sin(\theta + \varphi_1) = 0 \tag{21}$$

By solving (21) we have:

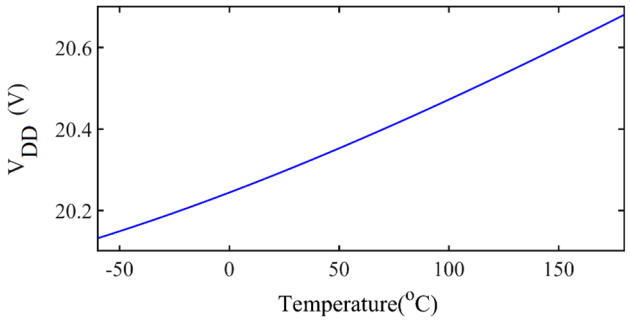

Figure 9. The value of V_{DD} based on temperature.

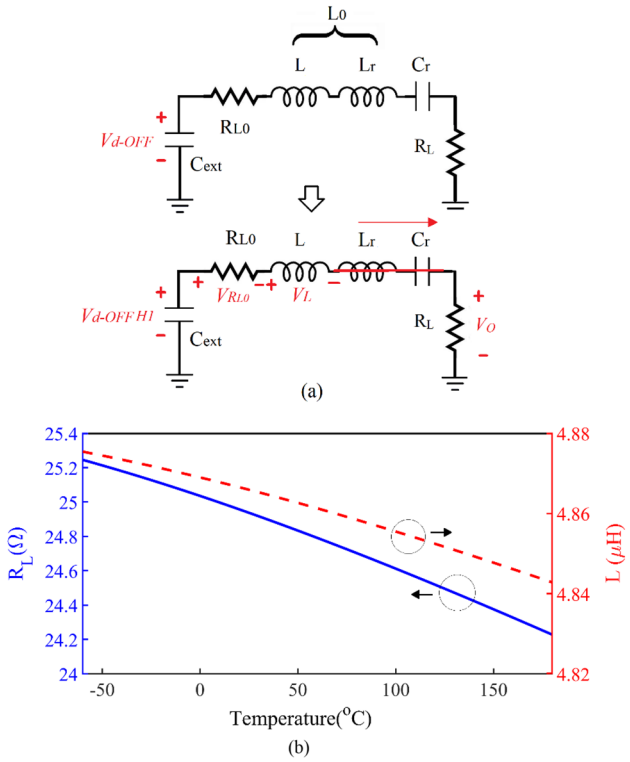

Figure 10. (**a**) The output resonant circuit in the main harmonic. (**b**) The R_L and L for establishing ZVS and ZVDS.

$$\left|V_{d-OFF}H1\right| = I_{m1}\sqrt{\left(2\pi f \times L\right)^2 + \left(R_L + R_{L0}\right)^2} \tag{22}$$

$$\varphi_{V_{d-OFF}H1} = \varphi_1 + tan^{-1}\left(\frac{2\pi f \times L}{R_L + R_{L0}}\right) \tag{23}$$

where $\left|V_{d-OFF}H1\right|$ and $\varphi_{V_{d-OFF}H1}$ are the absolute value and phase of the fundamental harmonic of V_{d-OFF}, respectively. By solving (22) and (23) the value of output resistance and phase difference inductor are calculated as follows:

$$R_L = \sqrt{\frac{\left|V_{d-OFF}H1\right|^2}{I_{m1}^2\left(1 + tan^2\left(\varphi_{V_{d-OFF}H1} - \varphi_1\right)\right)}} - R_{L0} \tag{24}$$

$$L = \frac{1}{2\pi f}\sqrt{\frac{\left|V_{d-OFF}H1\right|^2 \times tan^2\left(\varphi_{V_{d-OFF}H1} - \varphi_1\right)}{I_{m1}^2\left(1 + tan^2\left(\varphi_{V_{d-OFF}H1} - \varphi_1\right)\right)}} \tag{25}$$

By solving (24) and (25), the optimal load resistance values (R_L) and L that are suitable for creating ZVS and ZVDS conditions at different temperatures are calculated. The calculated R_L and L are shown in Fig. 10b. As the temperature increases, the value of these parameters should be reduced to achieve the conditions of ZVS and ZVDS and have a constant output current.

In this design, the quality factor in the resonant circuit is considered to be 10, so that the output current waveform is close to a pure sinusoid. According to (26) and (27), the value of the inductor and capacitor of the series resonant are obtained based on the temperature, as shown in Fig. 11. As the temperature increases, to access the ZVS and ZVDS conditions and constant output current, the inductor should be decreased and the capacitor should be increased.

$$Q = \frac{2\pi f L_r}{R_L} \rightarrow L_r = \frac{Q \times R_L}{2\pi f} \tag{26}$$

$$f = \frac{1}{2\pi\sqrt{L_r \times C_r}} \rightarrow C_r = \frac{1}{\left(2\pi f\right)^2 L_r} \tag{27}$$

In a real Class E inverter, the efficiency is not 100% due to the presence of parasitic elements. The efficiency can be calculated by dividing the power delivered to the load over the total power consumption in the circuit as follows:

$$\eta = \frac{P_O}{P_O + P_{loss}} \tag{28}$$

The total power consumption of the circuit is expressed as:

$$P_{loss} = P_{R_{RFC}} + P_{R_{LO}} + P_{R_{on}} \tag{29}$$

where $P_{R_{RFC}}$,$P_{R_{L0}}$, and $P_{R_{on}}$ are the dissipated power in R_{RFC}, R_{L0}, and R_{ON}, respectively. The efficiency is calculated as:

$$\eta = \frac{\frac{1}{2}R_L I_m^2}{\frac{1}{2}R_L I_{m1}^2 + R_{RFC}I_{DC}^2 + 0.5R_{L0}I_{m1}^2 + \frac{1}{2\pi}\int_0^{2\pi} R_{ON}I_{m1}\sin\left(\theta + \varphi_1\right)d\theta} \tag{30}$$

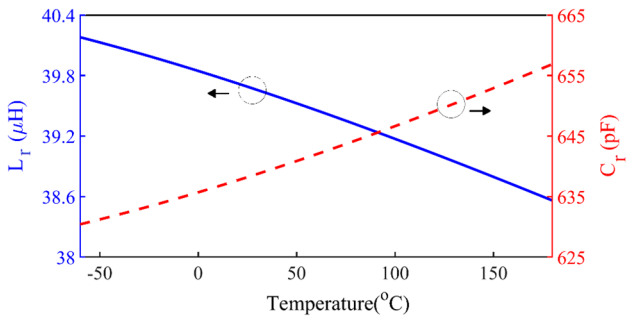

Figure 11. The L_r and C_r of the series resonance.

In order to have a constant output current and maintain the nominal conditions, the values of the circuit elements change according to the ambient and junction temperature. Figure 12 shows, that the efficiency and output power versus temperature variations when the values of the circuit elements change. As can be seen, the output power and the efficiency in the presented SCE inverter decrease with rising temperature.

Presented design for the class E inverter at 25 °C. In this section, a class E inverter at 25 °C is designed and the elements of the circuit are obtained according to previous analysis as listed in Table 2, then the effect of temperature variations on the specifications are investigated as shown by a block diagram in Fig. 13.

By solving (14) and (15), the dependence of the drain voltage is calculated according to temperature and Θ, as shown in Fig. 14a,b. In the ON-state, taking into account the rising $R_{ON,}$ the drain voltage rises, as shown in Fig. 14a. Due to the constant V_{DD}, as the temperature increases, the total area under the drain voltage curve from 0 to 2π should also remain constant. Therefore, to compensate for the increase in the drain voltage in the ON state, the peak value of drain voltage in the OFF-state is reduced as shown in Fig. 14b. The drain current is considered

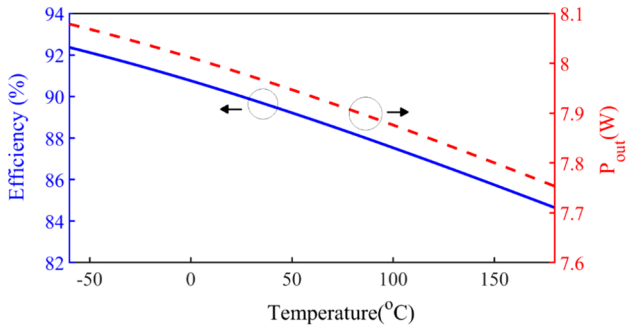

Figure 12. The output power and efficiency.

Element	Values
L (μH) + L_r(μH)	4.86 + 39.6
C_r (pF)	638.7
R_L (Ω)	24.9
V_{DD} (V)	20.31
L_{RFC} (μH)	400
R_{RFC}(Ω)	0.3
C_{ext} (pF)	1000

Table 2. The element's value of the presented class E inverter at 25 °C.

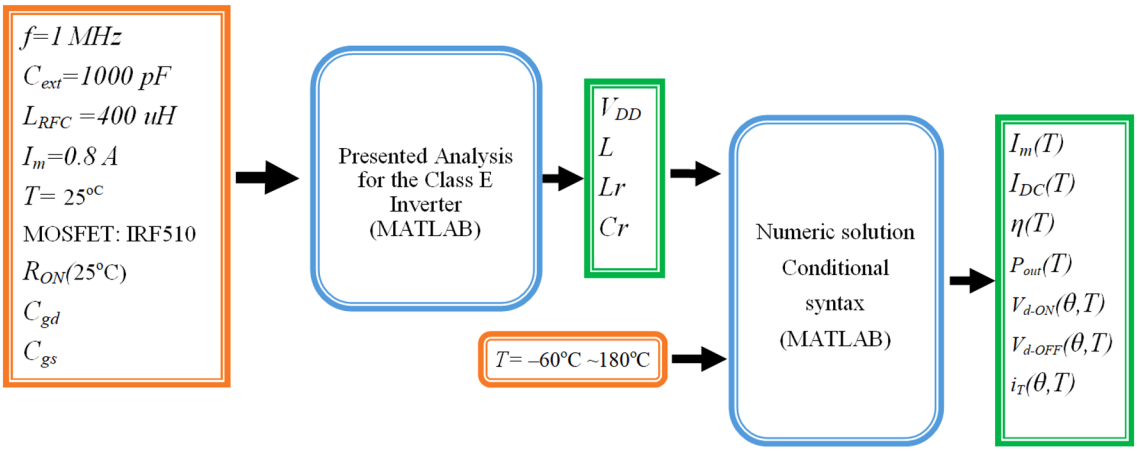

Figure 13. Block diagram of the Presented Design for the Class E Inverter at 25 °C.

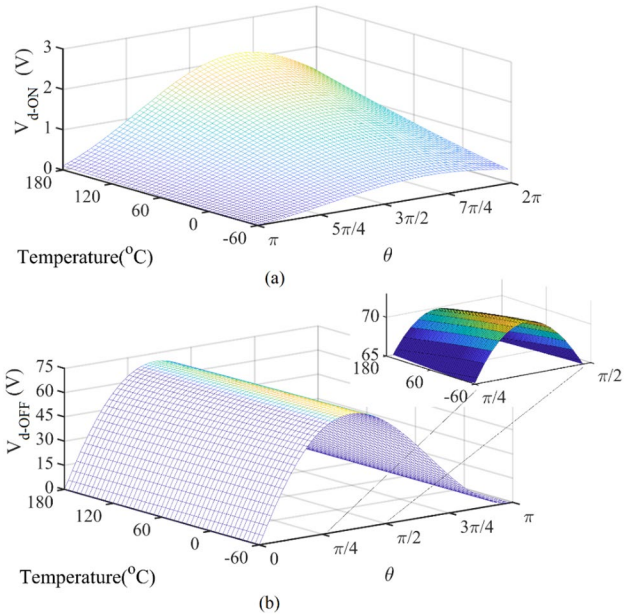

Figure 14. V_d versus temperature and Θ (**a**) in the ON-state ($\pi < \Theta < 2\pi$), (**b**) in the OFF-state ($0 < \Theta < \pi$).

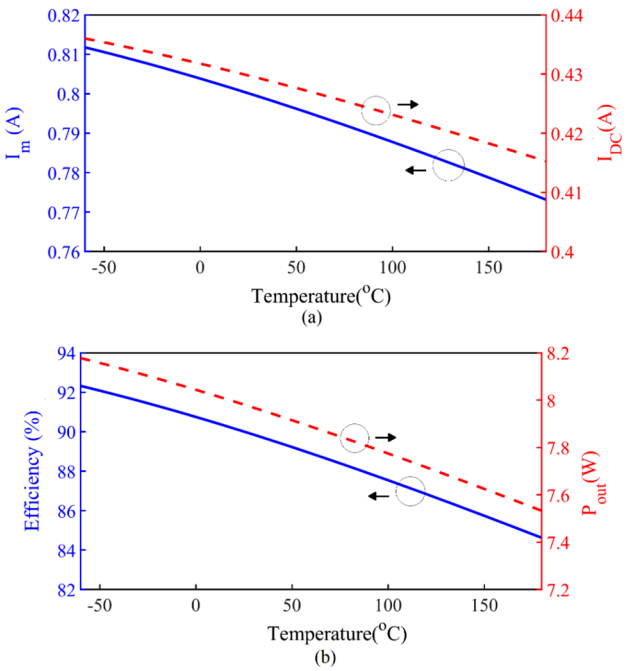

Figure 15. (**a**) I_m and I_{DC} versus temperature. (**b**) Efficiency and P_{out} versus temperature.

zero in the range of 0 to π and the transistor resistance is assumed infinite. One of the important factors in the design is to consider the maximum voltage that can be tolerated for the transistor according to its model. If the drain voltage changes caused by temperature fluctuations are not controlled, they can damage the transistor.

A change in temperature causes a change in resistance, and then the amount of output current and efficiency and output power change. Figure 15a,b show the reduction of these parameters based on temperature increment. As it is clear, these changes are significant and should be considered in the design.

Design of the presented thermal compensation unit. In this section, a thermal compensation unit (TCU) is provided for the SCE. According to (11), R_{ON} has inversely related to the gate-source voltage applied to the transistor. R_{ON} versus V_{GS} and temperature is shown in Fig. 16.

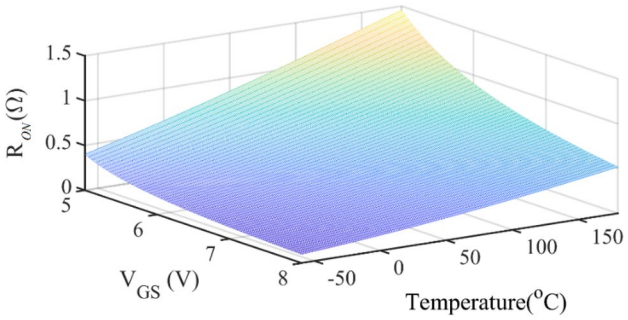

Figure 16. R_{ON} versus VGS and temperature.

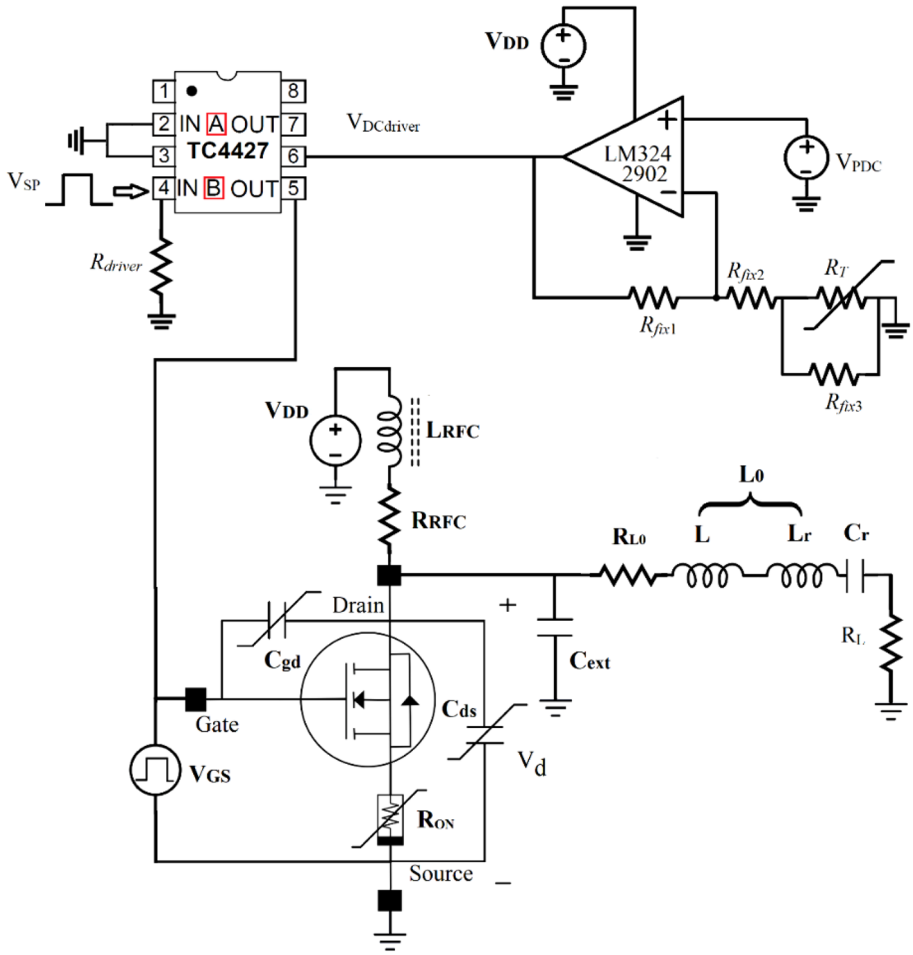

Figure 17. The equivalent circuit of the thermal compensated class E (TCCE) inverter.

To achieve a constant R_{ON} with temperature variations, the amount of V_{GS} in the circuit should be changed. To generate V_{GS} according to temperature changes, a compensation circuit is designed, as shown in Fig. 17.

The TCU includes:

- An OP-AMP is formed in a non-inverter state.
- Three constant resistors (R_{fix1}, R_{fix2}, R_{fix3}).
- R_T is a 10KΩ negative temperature control (NTC) resistor with 3435 part-number.
- V_{PDC} has applied voltage to the op-amp.
- TC4427 is used as the driver.

R_T has a nonlinear decreasing behavior with increasing temperature. The model of this resistor is 3435. The resistance value versus temperature is shown in Fig. 18.

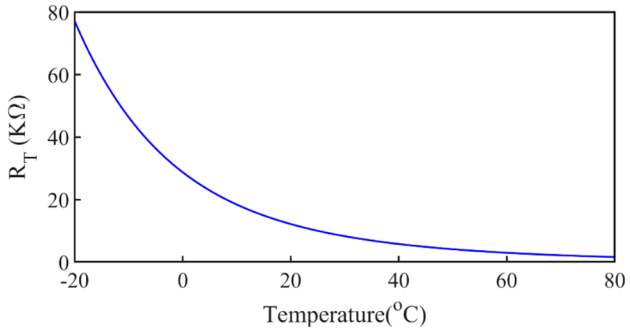

Figure 18. R_T versus temperature.

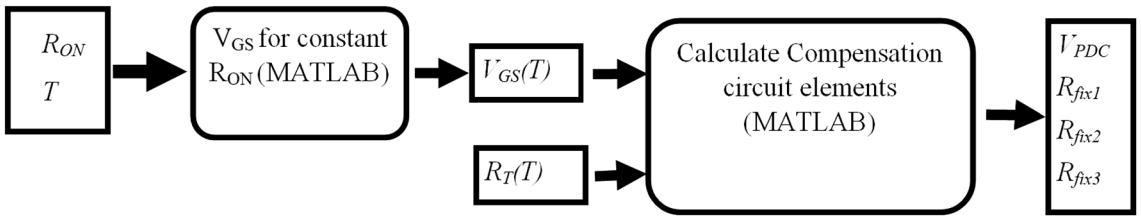

Figure 19. Block diagram of the TCU design flow.

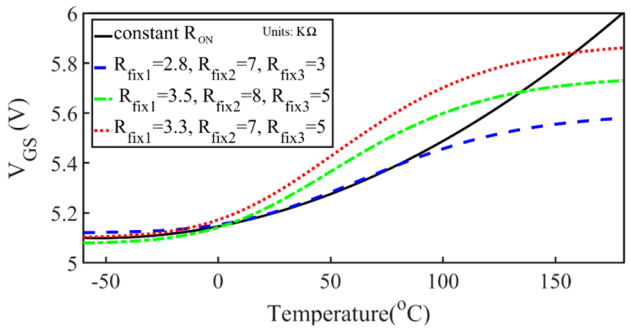

Figure 20. V_{GS} versus temperature for different values of R_{fix1}, R_{fix2}, and R_{fix3} and the constant resistance at 25 °C.

The block diagram of the TCU design process is shown in Fig. 19. The values of V_{GS} versus temperature that creates constant R_{ON} are obtained from Fig. 16 in MATLAB and plotted in Fig. 20 with a continuous-black-line. The elements value of the compensation circuit as shown in Fig. 17 are calculated in MATLAB with respect to V_{GS} and R_T (3435 NTC resistor) values. Figure 20 shows the created V_{GS} versus temperature with different values of R_{fix1}, R_{fix2}, and R_{fix3}.

$V_{DCdriver}$ determines the value of the pulse signal applied to the gate and is calculated from the following equation:

$$V_{DCdriver} = V_{PDC}\left(1 + \frac{R_{fix1}}{R_{fix2} + R_T||R_{fix3}}\right) \tag{31}$$

Figure 20 shows, V_{GS} versus temperature for constant R_{ON} in a continuous black line. The elements of the compensation circuit, which are R_{fix1}, R_{fix2}, R_{fix3}, and V_{PDC} should be adjusted so that the compensation circuit produces this pattern for V_{GS}. The blue dashed lines with $R_{fix1} = 2.8$, $R_{fix2} = 7$, and $R_{fix3} = 3$ KΩ provide the best agreement between − 60 and 100 °C. The SCE is investigated with and without the compensation circuit. When the TCU is in the design, it prevents the effect of temperature variations on the inverter parameters. The changes in efficiency and output power based on the temperature in the SCE and the TCCE inverter are shown in Fig. 21, simultaneously. The compensator enables significant improvements by maintaining the simulation power and efficiency almost constant (8.46 ± 0.14 W and 90.4 ± 0.2%) within the temperature range of − 60 to 100 °C. From the comparison of efficiency and output power in the TCCE inverter and the SCE inverter, it is becoming clear

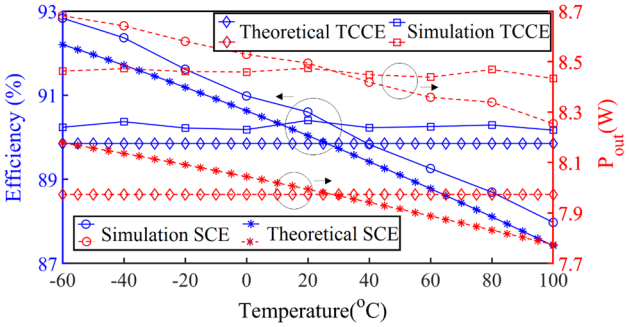

Figure 21. The changes in efficiency and output power of the SCE and TCCE.

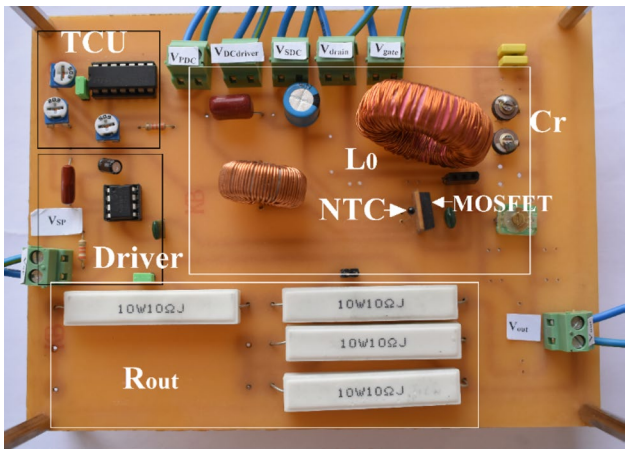

Figure 22. The fabricated inverter.

that the TCU provides constant output power and efficiency versus temperature variations, which is very desirable for telecommunication circuits.

Performance analysis result

The presented TCCE inverter is fabricated and shown in Fig. 22. The input signal has a duty ratio of 0.5. The operation frequency is 1 MHz. As can be seen, the negative temperature control resistor is placed next to the IRF510 to sense the ambient and junction temperature simultaneously. The TCU can be isolated from the SCE inverter with a jumper so that it can be tested with and without the compensation circuit. The load resistance is made by ceramic resistors with a tolerance of 10 watts. All capacitors used are able to withstand high power.

Comparison of theoretical, simulation, and experimental results. Table 3 shows the values of the elements used in the TCCE inverter. Table 4 shows the theoretical, simulated, and measured results of the presented TCCE inverter at 25 °C. As can be seen, the simulation and measurement results are very close to the theoretical results. This precision in the results is due to the consideration of all the parasitic elements of the transistor as well as the resistance of the transistor in the ON-state. Figure 23a shows the output driver voltage applied to the gate of the transistor. The value of V_{GS} is 5.2 V. The driver output capacitor causes a slow slope in the measured V_{GS}. In Fig. 23b, the drain voltage for simulation, theoretical and fabrication results are shown. The output current is considered pure sinusoidal in the theoretical analysis, but in the measurement and simulation results, the output current has more harmonics, which increases the drain voltage level for simulation and measurement.

Figure 24c shows the output voltage. The difference between the results is due to the increase of the resistance in the resonance path in the manufacturing process and considering the output current as a pure sinusoid. Figure 24a shows the applied gate voltage for the SCE inverter at 25 °C and 80 °C and also for the TCCE inverter at 80 °C. At a temperature of 80 °C, the value of gate voltage increases due to the operation of the compensating circuit and prevents changes in the drain voltage. As can be seen in Fig. 24b, the drain voltage in the SCE inverter at 25 °C is almost the same as the drain voltage in the TCCE inverter at 80 °C. Due to the operation of the TCU, the peak of the drain voltage remains constant. Figure 24c shows that at 80 °C in the SCE inverter, the output voltage is affected by the decreased in the drain voltage. Table 5 compares the values of the parameters measured with SCE at 25 °C and 80 °C and the parameters measured with TCCE at 80 °C. In the SCE inverter at 80 °C,

Element	Theoretical	Simulated	Measured
R_{fix1} (kΩ)	2.8	2.8	2.8
R_{fix2} (kΩ)	7	7	7
R_{fix3} (kΩ)	3	3	3
R_T (kΩ) (3435)	10	10	10
L_{RFC} (μH)	400	400	400
R_{RFC}(Ω)	0.3	0.3	0.3
C_{ext} (pF)	1000	1000	1000
R_{L0} (Ω)	1.2	1.2	1.5
R_{driver} (KΩ)	33	33	33
C_{driver} (pF)	500	500	500
L (μH) + L_r(μH)	4.86 + 39.6	4.86 + 39.6	45
C_r (pF)	638.7	638.7	639
R_L (Ω)	24.9	24.9	25

Table 3. The elements value of the inverter and compensation circuit.

Parameter	Theoretical	Simulated	Measured
V_{DD} (V)	20.31	20.31	20.3
I_{DC} (A)	0.4297	0.461	0.407
I_{m1} (A)	0.8	0.824	0.77
V_{PDC} (V)	4	4	4
P_{out} (W)	7.97	8.46	7.42
η (%)	89.85	90.4	89.9

Table 4. The important parameters of the inverter at 25 °C.

the output power is 2.7% lower than the SCE inverter at 25 °C. By applying the TCCE inverter, this difference reaches 0.13%, which is very favorable. In the SCE inverter, the efficiency at 25 °C is 89.9%, which decreases to 88.1% when the temperature increases to 80 °C. As the temperature increases in the TCCE inverter, the efficiency remains constant. It is concluded that the TCU has a very positive effect on the inverter parameters. Important parameters of the class E inverter for comparing the TCCE inverter with other references are presented in Table 6. The output power and efficiency of the proposed circuit are 7.42 W and 89.9%. Output power and efficiency are in conflict with each other, in some references, despite high efficiency, they have provided lower output power. C_{gd} and C_{ds} have a non-linear relationship with the drain-source voltage and their consideration confirms the theoretical answer. None of the references consider these capacitances as nonlinear elements in design process, nor do all references consider the nonlinear effects of R_{ON}.

Conclusion

In this paper, a class E inverter with a thermal compensation unit has been presented. In the WPT, the class E inverter is more affected by temperature due to the presence of the active elements. The temperature variation effect has been considered in the class E inverter design including nonlinear C_{ds}, C_{gd} and R_{ON} and it has been compensated to achieve a reliable power source in the biomedical implant. It has been found that temperature changes significantly affect inverter characteristics such as output power and efficiency. Therefore, a compensation circuit was proposed and added to the simple class E inverter. Simulations were performed and the results confirmed that the compensator enables significant improvements by maintaining almost constant power and efficiency (8.46 ± 0.14 W and 90.4 ± 0.2%) in the temperature range of − 60 to 100 °C. The thermal compensation class E inverter has been fabricated, and the simulation and theoretical results are validated with the measured results. The tested circuit results are in good and acceptable agreement with the simulation results. The obtained output power is 7.42 W with an efficiency of 89.9% at 25 °C.

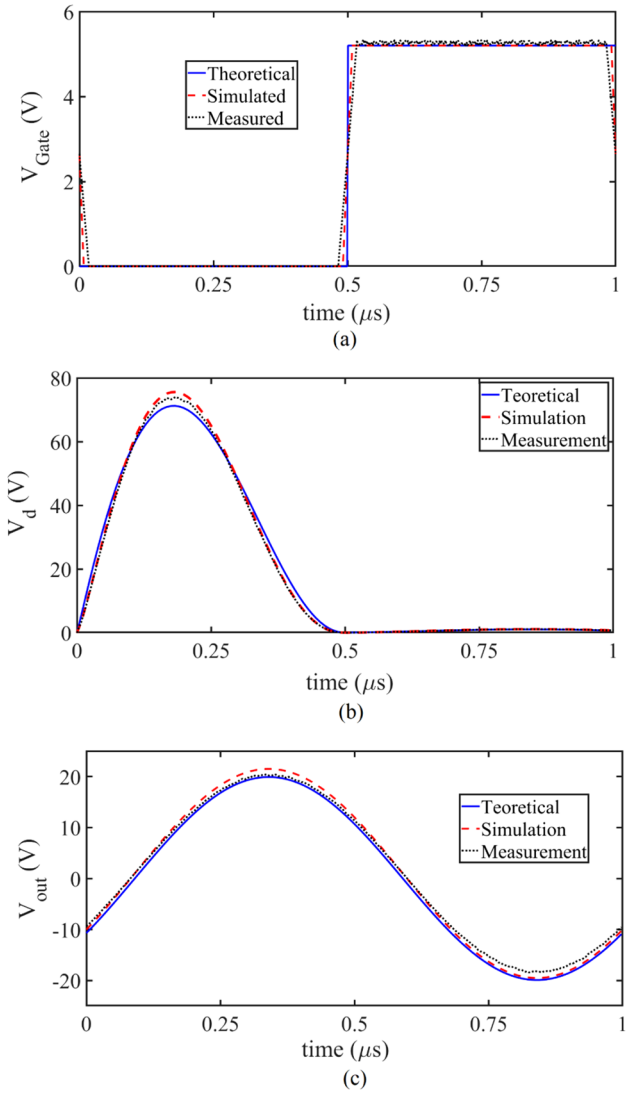

Figure 23. (**a**) The output driver voltage is applied to the transistor gate. (**b**) V_d and (**c**) the output voltage for the simulation, theoretical, and fabrication at 25 °C.

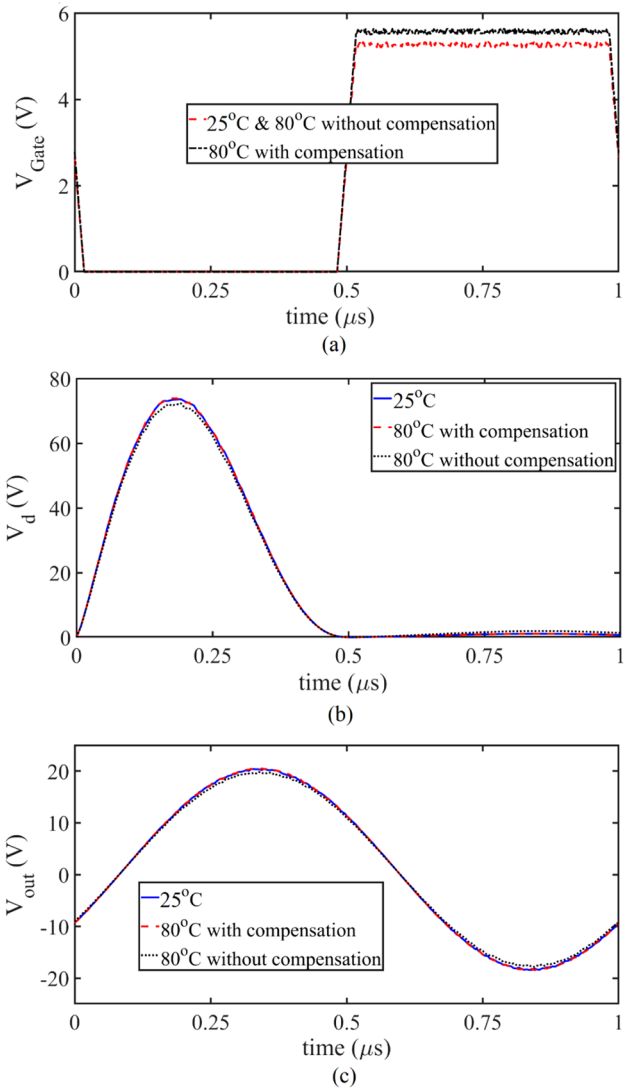

Figure 24. (**a**) The SCE and TCCE output driver voltage is applied to the transistor gate. (**b**) The SCE and TCCE waveform of V_d and (**c**) The SCE and TCCE output voltage for the simulation, theoretical, and fabrication at 25 °C and 80 °C.

Parameter	Measured				
Temperature (°C)	25	80			
	SCE	TCCE		SCE	
Compensation	Value	Value	Difference %	Value	Difference %
V_{DD} (V)	20.3	20.3	0	20.3	0
I_{DC} (A)	0.407	0.407	0	0.404	− 0.74
I_{m1} (A)	0.77	0.771	+ 0.13	0.759	− 1.43
P_{out} (W)	7.42	7.43	+ 0.13	7.22	− 2.7
η (%)	89.9	89.9	0	88.1	− 2

Table 5. The values of the measured parameters in the state with and without compensation circuit at 80 °C.

Ref	MOSFET	F (MHz)	P_{out}(w)	Efficiency	V_{GS}	V_{DD}	C_{gd}	C_{ds}	R_{ON}	TC*
[2]	IPP530N15N3G	1	10	37.7–89.3	10	10	–	Constant	–	NO
[3]	IRFR120Z	1	4.76	93.2	NA	19.5	–	Constant	–	NO
[8]	RQ6E045BN	0.8	1.02	92	5	4.5	–	Constant	–	NO
[9]	FQT13n06	0.8	0.96	89	6	4.5	–	Constant	–	NO
[12]	–	1800	17	83	4.4	28	–	Constant	–	NO
[14]	–	1370	9.5	90.2	8.8	28	–	Constant	–	NO
[19]	0.18 µm CMOS	477	1.5	NA	NA	3.3	–	–	Linear	YES
This Work	IRF510	1	7.42	89.9	5.2	20.3	Nonlinear	Nonlinear	Nonlinear	YES

Table 6. The comparison between the presented inverter and other works. *TC refers to thermal compensation.

Data availability

The calculated results during the current study are available from the corresponding author on reasonable request.

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Author contributions

Design, analysis, investigation, and writing—original draft preparation M.K., suggestions, writing—review and editing: M.H. and H.A. All authors discussed the results and contributed to the final manuscript.

Competing interests

The authors declare no competing interests.

Additional information

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