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Analog and RF performance optimization for gate all around tunnel FET using broken-gap material

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Many times, the fabricated cylindrical gate-all-around tunnel FET (GAA TFET) has an uneven radius due to several etching and deposition processes involved while fabricating the device, which show notable variations in the performance of the device. In this report, III–V uneven GAA TFET is studied by considering the uneven radius as elliptical in shape for all possible variations, which shows a significant impact on analog and RF figure of merits (FOMs). The performance of the optimized devices is compared with their circular structure and with their maximum deviation in elliptical geometry for all possible variations in device channel and gate oxide. The variations in its device channel and gate oxide have shown a significant impact on the performance of the device. The analog and RF FOMs are studied, including the transconductance generation factor (g_m/I_{DS}), intrinsic gain (g_mR_O), capacitances (C_{GS}, C_{GD}), cut-off frequency (f_T), and gate delay (τ_m).

Aggressive transistor scaling with the aim of boosting on-die capabilities has led to an adverse effect on power dissipation. Due to increasing insistence on power dissipation, low voltage requirements, energy conservation, and maximising on-die capabilities has led the devices having the prospect of acquiring sub-threshold swing (SS) surpassing the thermionic limit of 60 mV/dec has earned extensive attention[1–3]. Tunnel field-effect transistors (TFETs) have unique carrier injection mechanisms and inversion layer formation when compared to conventional MOSFETs. These lead to substantial improvement of SS, I_{ON}/I_{OFF} ratio, and, as such, TFET devices have been one of the prominent contenders for replacing conventional MOSFETs[4,5]. However, TFETs have encountered severe ambipolar leakage current (I_{AMB}), low ON-state current (I_{ON}), and gradual shifting between ON and OFF states[6]. With continuous scaling of devices, the reduction of power dissipation remains a primary requisite along with the enhancement of device performance as far as system-on-chip based CMOS integrated circuits are concerned. In addition, the gate-all-around (GAA) architecture has demonstrated enhanced electrostatic control, tunneling efficiency, off-state leakage current, and current drivability, thereby, resulting in the improvement of analog and RF performances[7–9].

The steps involved in the fabrication of the vertical GAA structure involve several etching, deposition, and growing processes, which generally form an uneven radius rather than the ideal circular GAA structure[10,11]. Because of this uneven radius, predicting the performance of fabricated GAA device structures is difficult[12,13], and only a few reports for its acceptable variations[14–17] are available. Most of the reports only address one type of geometry and are of mostly MOSFET devices, as the report[12] shows the impact of hydrogen annealing on the device diameter of GAA MOSFET devices, which led to the elliptical circumference having an ON current of 825 μA/μm, report[13] shows the fabricated GAA MOSFET device having an elliptical shape (i.e., EOEC geometry) having ON current of 976 μA/μm, report[15] demonstrate the impact of varying channel length on fabricated elliptical GAA MOSFETs, report[14] demonstrates numerical analysis on three different types of variations such as t_{si} fluctuation, elliptical shape fluctuations (i.e., EOEC fluctuations), and corner rounding fluctuations where the acceptable tolerance for RF IC design is analyzed as $\Delta t_{si} < 1$ nm and $r/R > 75\%$, and the report[16] mathematically analyzed the short-channel-effects of elliptical GAA MOSFET (i.e., EOEC structure) by varying its effective radius. The experimental[18,19] and numerical analyses[20] suggest that incorporating III-V broken-bandgap semiconductor material in TFET devices shows improved tunnelling efficiency, leading to enhanced device performance[21,22].

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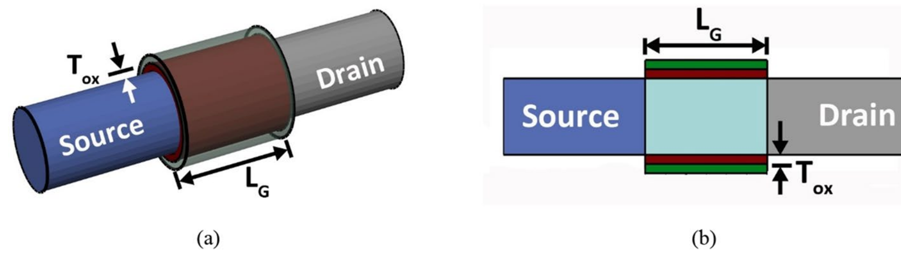

Figure 1. EOEC eGAA TFET structure: (**a**) 3D view, (**b**) cross-sectional view.

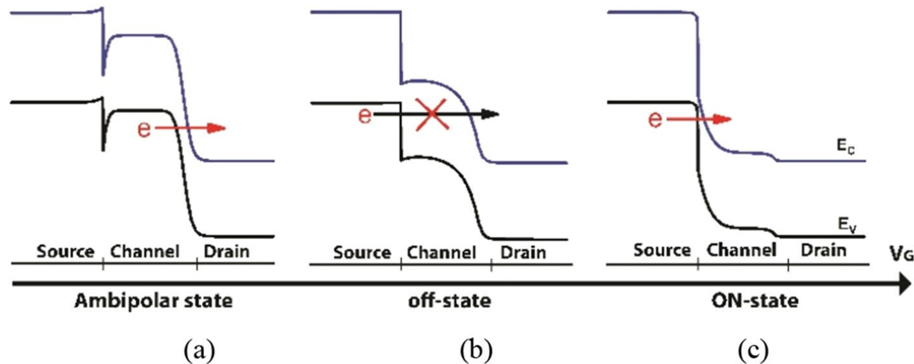

Figure 2. Band diagram of COCC structure: (**a**) ambipolar-state, (**b**) off-state, (**c**) ON-state.

Parameter	Predicted value for year 2021	Obtained value
V_{DD} for III–V material, (V)	0.59	0.3
C_{GG} for III–V material, (fF/μm)	0.59	0.0385
Mobility, (cm^2/V-s)	300	15,509.8
I_{OFF} (pA/μm)	20	6.7

Table 1. ITRS 2013 (predicted LP technology requirements of multi-gate (MG) FET devices for year 2021).

The ternary compound material of type-II heterostructure such as GaSb/InGaAs gained importance due to its tunable band alignment, direct bandgap, and effective bandgap by varying the mole fraction[23–25]. There are some challenges while fabricating III–V semiconductor TFETs, such as a lack of dielectric material, which causes thermodynamically unstable interface states, thereby leading to fermi level pinning at the interface. Moreover, uncontrolled oxidation on III–V material results in a higher density of bandgap traps at the interface. However, these challenges are encountered by using the interface control (i.e., passivation) layer at the interface[26].

In this report, the issues related to fabricating vertical GAA TFET are considered where the most unlikely uneven radius is considered to be elliptical in shape for all possible GAA fabrication defects. In addition, a broken-gap type-II heterojunction of GaSb/InGaAs material has been introduced[23], which further boosts the device performance. The objective of this paper is to design and optimize III–V elliptical gate-all-around TFET (III–V eGAA TFET) by varying the minor diameter (MD) and gate dielectric thickness (T_{OX}) of the channel region to get the optimized MD and T_{OX} of the elliptical structure. The optimization process is carried out by considering the higher I_{ON}, lower I_{AMB}, low parasitic capacitance, minimum gate delay (τ_m), and higher mobility. Finally, the optimal structure is investigated for analog and RF performance.

Device structure and simulation methodology. The 3D and cross-sectional schematics of the simulated III–V eGAA TFET structure for elliptical oxide–elliptical channel (EOEC) is shown in Fig. 1, and its corresponding band diagram for circular oxide–circular channel (COCC) for ambipolar, off, and ON state conditions are depicted in Fig. 2. The device under simulation incorporates type-II heterojunction material such as GaSb/InGaAs[23]. In addition, the uneven radius of the fabricated device is considered elliptical in nature, having a major diameter of 20 nm, and the optimal value of the minor diameter (MD) is calibrated by varying it from 10 to 20 nm. The device also incorporates the source doping (N_A) of 10^{20} cm^{-3}, intrinsic channel doping (N_I) of 10^{15} cm^{-3}, drain doping (N_D) of 5×10^{19} cm^{-3}, gate length (L_G) of 30 nm, and maximum gate oxide thickness (T_{OX}) of 2 nm. The inset of our simulation is in agreement with ITRS[27] and the targeted value considered in our simulation is tabulated in Table 1, where the work function of the metal and supply voltage (V_{DD}) are

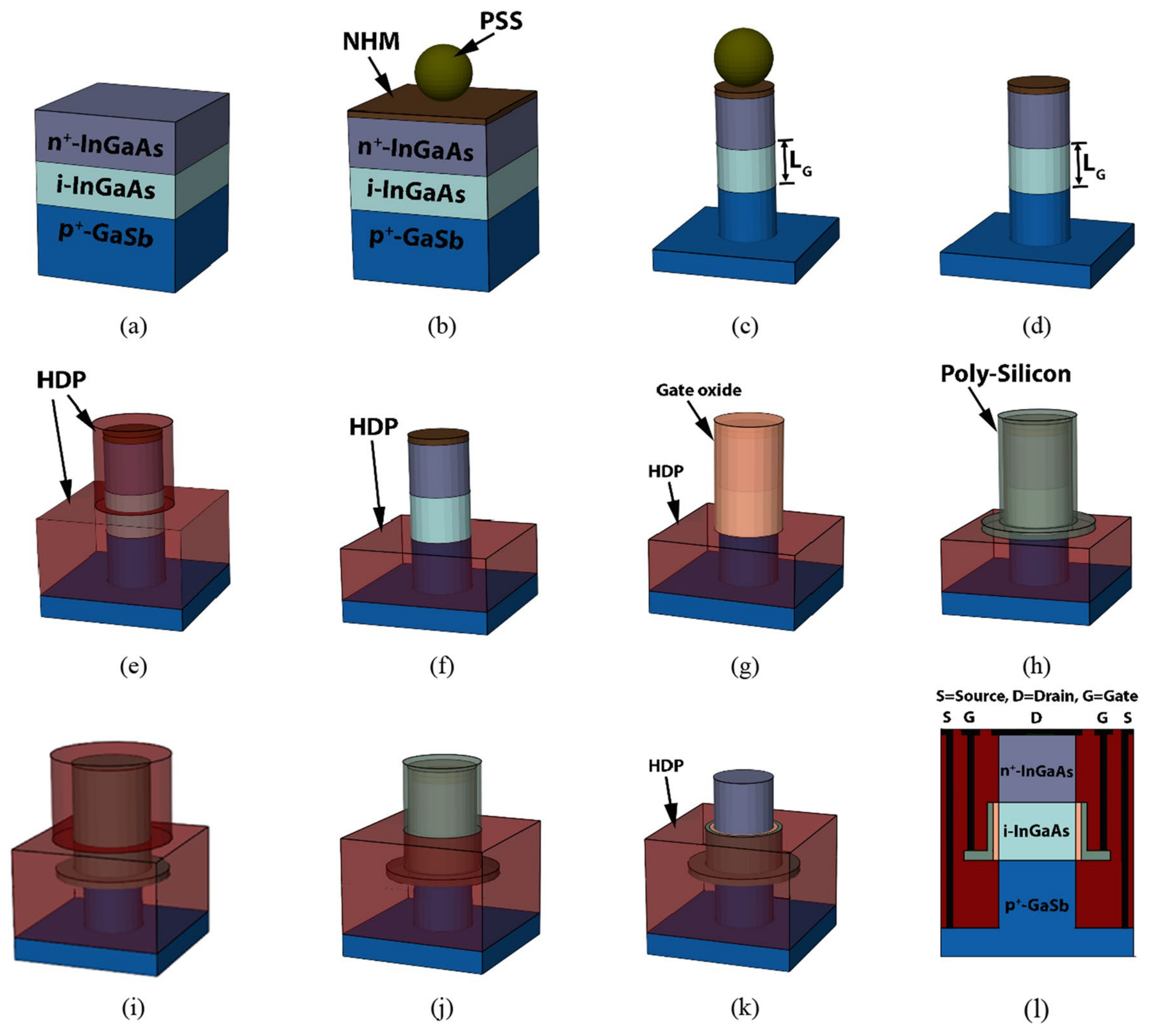

Figure 3. Schematic of III–V eGAA TFET fabrication steps: (**a**) III–V material deposition, (**b**) PSS placement, (**c**) RIE on PSS to get 20 nm sphere followed by NHM deposition, (**d**) deep RIE etching process, (**e**) PSS of 20 nm diameter and NHM etched away, (**f**) SiO_2 deposition, (**g**) PSS of 24 nm diameter and NHM deposition, (**h**) DHF etch-back up to the source-channel junction, (**i**) PolySilicon deposition, (**j**) SiO_2 deposition, (**k**) contact tip implantation followed by contact formation.

set at 5.01 eV (i.e., nickel) and 0.3 V, respectively. The simulations are carried out by the *3D* numerical device simulator TCAD Sentaurus[28] with an optimized meshing strategy as discussed in[29]. The non-local band-to-band tunnelling (BTBT) model has been employed in our simulation. Apart from this, carrier scattering due to the presence of charged impurity ions and velocity saturation at high-field is activated by considering concentration-dependent and high-electric field-dependent mobility models. The mobility degradation model at interfaces is also included to compute the transverse field, and the old Slotboom model is incorporated to compute the doping-induced bandgap narrowing of the material. Moreover, the effect of the strain through deformation in the lattice structure, causing shifts in the conduction and valance bands, is captured by the piezo deformation potential model. Finally, the quantum correction model is incorporated to take into account the change in the effective bandgap of the device due to the variation in MD from 10 to 20 nm. The non-local BTBT parameters of Sentaurus TCAD for InGaAs and GaSb are used as described in[30].

Proposed fabrication steps. The process steps for fabricating III–V eGAA TFETs are proposed in Fig. 3. The sequential process steps which can be employed for the fabrication are: (i) Layers of GaSb (p-type, Be ~ 10^{20} cm^{-3}), 30 nm of InGaAs (intrinsic, Si ~ 10^{15} cm^{-3}), and 35 nm of InGaAs (n-type, Si ~ 5×10^{19} cm^{-3}) need to be deposited layer-by-layer as shown in Fig. 3a. Such a deposition can be carried out by molecular beam epitaxy (MBE). Then, a nitride hard mask (NHM) is deposited on top of the surface followed by a spreading polystyrene sphere (PSS) to self-assemble on top of the surface (Fig. 3b). To reduce the PSS diameter, the reactive ion etching (RIE) process can be used, which forms colloidal particle nanodots that are no longer closely packed (i.e., space is created for gate oxide and contact pad deposition) for getting the GAA structure. (ii) Tetramethylammonium hydroxide (TMAH) based wet etch process needs to be carried out to remove the material

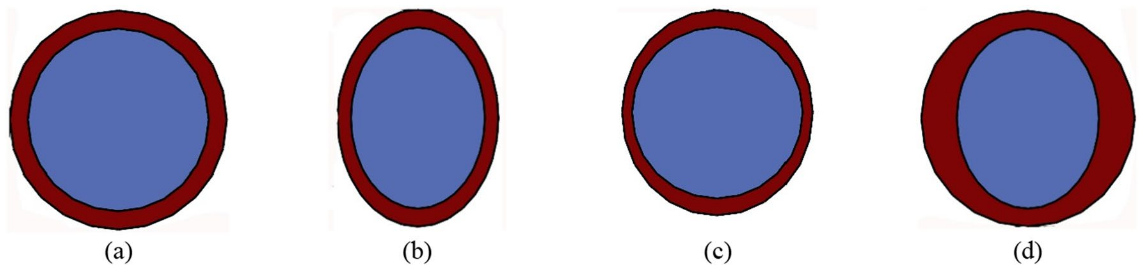

Figure 4. Schematic representation of possible cross-sectional variations of GAA structure due to fabrication imperfections: (**a**) circular oxide—circular channel (COCC), (**b**) elliptical oxide—elliptical channel (EOEC), (**c**) elliptical oxide—circular channel (EOCC), (**d**) circular oxide—elliptical channel (COEC).

underneath the NHM patterned by PSS (Fig. 3c). The next step involves etching away the PSS with the dissolution of $CHCl_3$ (Fig. 3d).

Further, a non-conformal high-density plasma (HDP) oxide is deposited (Fig. 3e), followed by dilute hydrofluoric acid (DHF) etch-back to get HDP up to the source-channel junction (Fig. 3f). (iii) To grow gate oxide high-density plasma chemical vapor deposition (HDPCVD) technique can be used (Fig. 3g), followed by the deposition of poly-silicon (Fig. 3h). (iv) Again, non-conformal HDP oxide is deposited (Fig. 3i) and DHF etch-back to get HDP up to the channel-drain junction (Fig. 3j). Further, etch-back the poly-silicon, gate oxide, and NHM to expose the drain region (Fig. 3k). Finally, non-conformal HDP oxide is deposited again and patterned to form the contact pads (Fig. 3l).

We have considered that the RIE process is involved in reducing the PSS and the grown gate oxide, which accounts for the uneven channel radius and T_{OX} variation induced in the fabricated device. The worst-case scenario of structural variations involved in the fabrication process is considered elliptical in shape as depicted in Fig. 4, where, Fig. 4a shows the ideal circular GAA structure having a circular oxide-circular channel (COCC). Figure 4b to Fig. 3d represent elliptical oxide—elliptical channel (EOEC), elliptical oxide—circular channel (EOCC), and circular oxide—elliptical channel (COEC), respectively.

Structural optimization. Device optimization for EOEC and COEC structure is carried out by evaluating optimal channel MD by varying it from 10 to 20 nm. For the EOCC structure, optimization is done by varying T_{OX} from 1 to 2 nm along the minor axis (MA).

For optimization of the EOEC structure, the major diameter of the channel region is fixed at 20 nm, while the MD is decreased from 20 nm (which represents a circular GAA TFET) to 10 nm (eGAA TFET), simultaneously maintaining the same gate oxide thickness of 2 nm throughout the entire elliptical periphery. The results of our simulation are depicted in Fig. 5a. Starting from 20 nm, as the channel, MD is reduced, the band bending between the drain-channel and source-channel region gradually increases as depicted in Fig. 6a. The former increases the inflow of carriers from drain to channel, increasing I_{AMB} of the device; the latter increases the inflow of carriers from source to channel, increasing J_{DS} of the device. As the channel MD is reduced, the area of the device decreases gradually, which consequently decreases C_{par} followed by a decrease in its τ_m. For EOEC structure optimization, the point at which the structure has maximum J_{DS} and μ_{carr}, and the minimum possible I_{AMB}, C_{par}, and τ_m is considered to be the optimized geometry. In this report, an EOEC structure having a MD of 14 nm is considered to be the optimized device.

For EOCC structural optimization, the channel region is fixed at 20 nm in diameter from all sides, while the T_{OX} is reduced from 2 nm (which represents circular GAA TFET) to 1 nm (eGAA TFET) along MA, while keeping a fixed T_{OX} of 2 nm along the major axis. The results of our simulation are depicted in Fig. 5b. Starting from 2 nm, as the T_{OX} along MA is reduced, the vertical electric field penetrates more into the substrate along MA, which consequently increases $J_{DS,}$ and the same is verified from the energy band diagram depicted in Fig. 6b where tunneling width becomes narrow with reducing T_{OX} along MA. As the vertical electric field is penetrating more into the substrate causes a narrowing of depletion width at the drain to the channel region. The reduced depletion width at the drain to channel region gives rise to the inflow of carriers from drain to channel, which leads to an increase in I_{AMB}, followed by an increase in its C_{par}. However, τ_m depends on J_{DS} and the total gate capacitance of the device, where J_{DS} shows the dominant factor which leads to a decrease in its τ_m. For EOCC structure optimization, the point at which the structure has maximum J_{DS} and μ_{carr}, and the minimum possible I_{AMB}, C_{par}, and τ_m is considered to be the optimized geometry. In this report, the EOCC structure having a T_{OX} of 1.4 nm along MA is considered to be the optimized device.

Finally, for COEC structural optimization, the outer diameter (both channel and T_{OX} together) is fixed at 24 nm from all sides, while with a decrease in channel MD from 20 to 10 nm (all are having an outer diameter of 24 nm) lead to virtual increment of T_{OX} from 2 to 7 nm along MD of the device as depicted in Fig. 4d. Result of our simulation depicted in Fig. 5c does not explicitly show the effect of variation of neither channel MD nor T_{OX} characteristics as obtained in Fig. 5a,b. For COEC characteristics, the impact of channel MD is observed up to certain channel MD, thereafter the impact of T_{OX} plays a significant role as depicted in Fig. 5c. Starting from 20 nm, as the channel, MD is reduced, the J_{DS} decreases up to 14 nm considering the same reason stated for Fig. 5a, thereafter J_{DS} increases due to the impact of T_{OX} which becomes more dominant than the impact of channel MD and follows the same reason stated for Fig. 5b[31]. The variation in current density is also verified by the

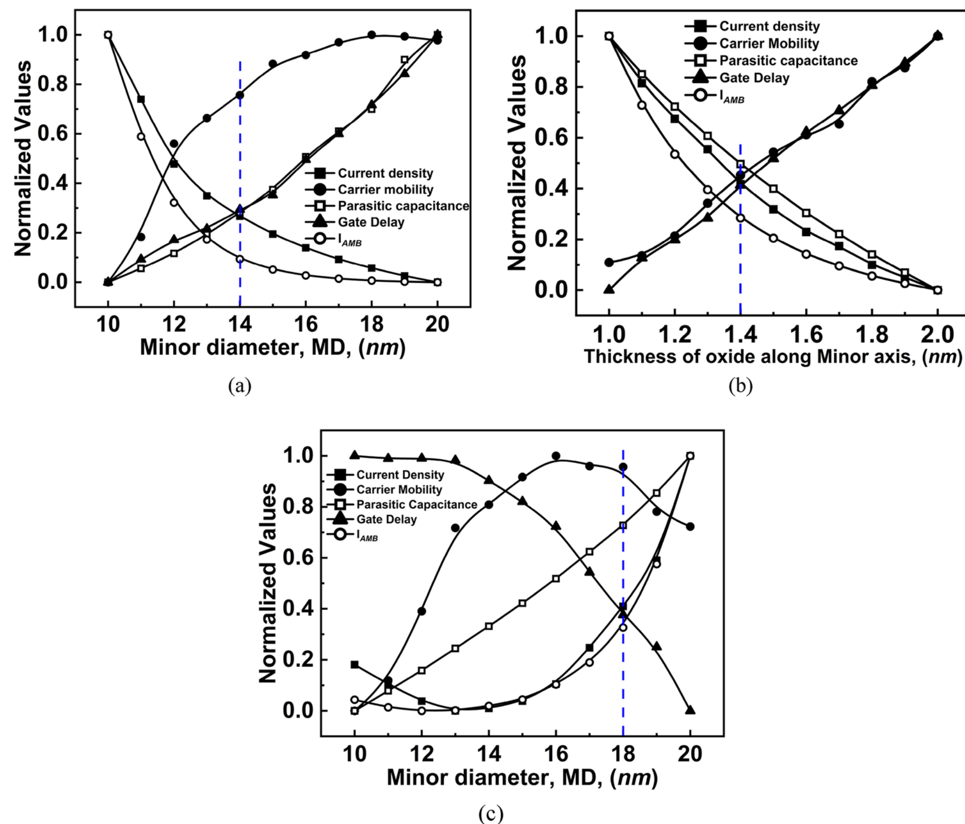

Figure 5. Normalized values for different eGAA TFET along: (**a**) MD for EOEC optimization, (**b**) MA of EOCC structure for gate oxide thickness optimization, (**c**) MD for COEC optimization.

energy band diagram depicted in Fig. 6c. For COEC structure optimization, the point at which the structure has maximum J_{DS} and μ_{carr}, and the minimum possible I_{AMB}, C_{par}, and τ_m is considered to be the optimized geometry. In this report, a COEC structure having a channel MD of 18 nm is considered to be the optimized device. It is observed that the channel MD of 14 nm and 18 nm for EOEC and COEC and T_{OX} of 1.4 nm for EOCC exhibit optimized device performance.

Further, the impact of mechanical strain generated during the fabrication process, specifically at the junctions due to lattice mismatches, has been considered in the analysis. These lattice mismatches cause variation in the band structure and carrier mobility of the device, which affects the drain current, as shown in Fig. 7a. To encounter these variations, piezo deformation potential (PDP) has been invoked to get closely matched fabricated device characteristics. It is observed from Fig. 7 that, when PDP is included, then the J_{DS} shows an increment of ~ 3.5%, ~ 3%, ~ 0.5%, and ~ 0.4% for COCC, COEC, EOCC, and EOEC, respectively, when compared to the device which does not have PDP involved in its numerical simulation analysis. Finally, the impact of structural deformation on threshold voltage and ON-state drain current of the device is depicted in Fig. 7b. It is observed that when the channel area is large and the oxide width is comparatively thinner for the EOCC structure, then ON-state drain current is high whereas threshold voltage is comparatively low. The impact is clearly visualized when we compare EOEC and COCC structures, where oxide width is constant and channel area reduces, which causes an increase in ON-state drain current and a decrease in the threshold voltage of the device because channel area is the dominating factor which reduces current density with a reduction in the channel area. On the other hand, the impact of oxide is visualized when we compare EOCC and COEC structures, where oxide width along the minor axis is significantly high. This high oxide width causes a decrease in the device's ON-state drain current and a significant increase in the device's threshold voltage, as shown in Fig. 7b. The detailed discussion of different optimized geometries due to varying channel area and oxide width on analog and RF performance is analyzed in the result and discussion section.

Results and discussion

This section presents the analog and RF performances of III-V eGAA TFET considering the channel MD of 14 nm and 18 nm for EOEC and COEC structures whereas T_{OX} of 1.4 nm for EOCC structures to get the better device performance at 300 °K.

Effect of process variation on analog performance parameter. The impact of channel MD and T_{OX} on the analog performance parameters such as transconductance (g_m), output conductance (g_D), transconductance generation factor (g_m/I_{DS}), and intrinsic gain (g_mR_O) for III-V eGAA TFET structure are analyzed in this

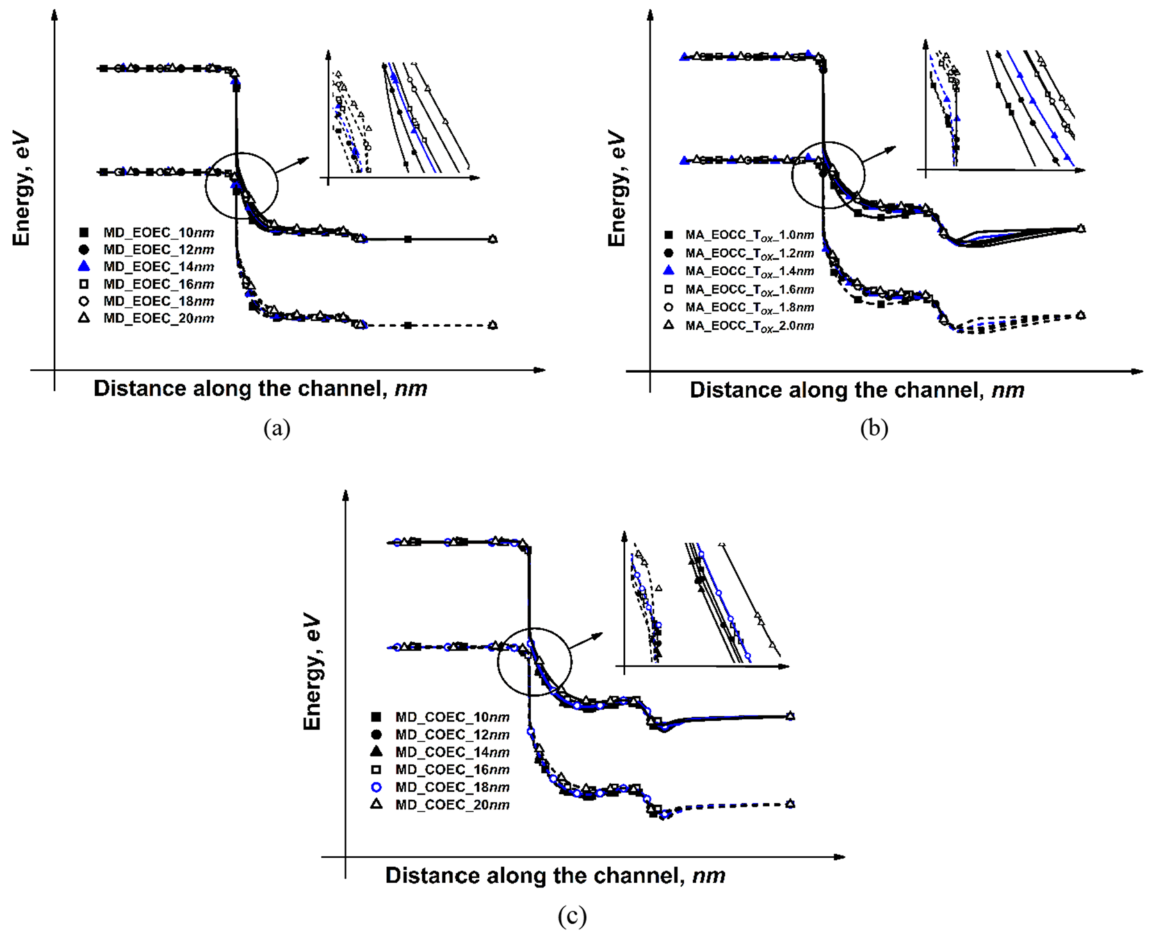

Figure 6. Band diagram for different eGAA TFET along: (**a**) MD for EOEC optimization, (**b**) MA of EOCC structure for gate oxide thickness optimization, (**c**) MD for COEC optimization.

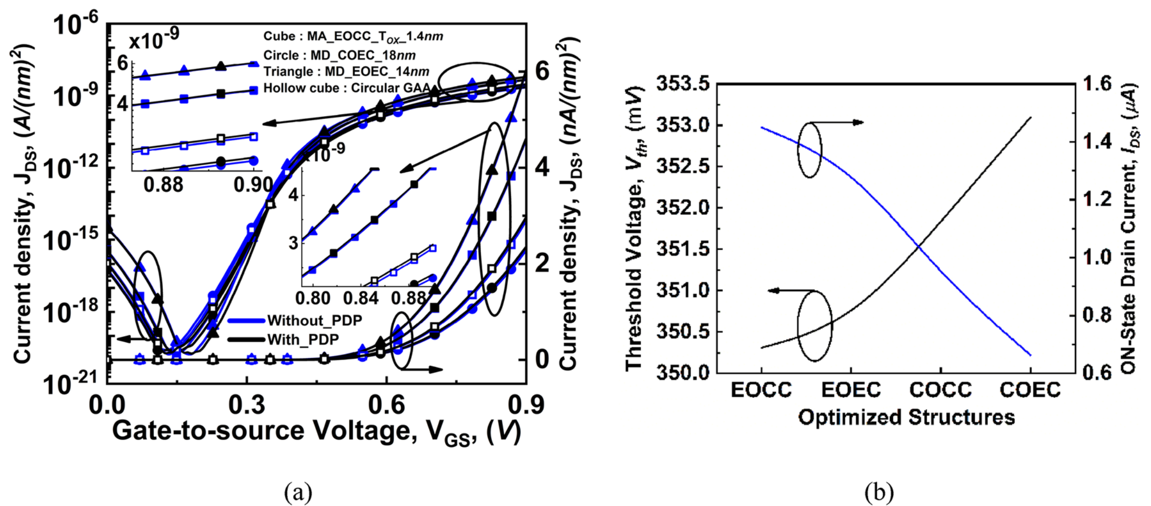

Figure 7. (**a**) Comparison of variation of drain current density (J_{DS}) as a function of gate-to-source voltage at $V_{DS} = 0.3$ V for all possible optimized structures when PDP is invoked, and (**b**) variation in threshold voltage and ON-state drain current as a function of deformation in device structures.

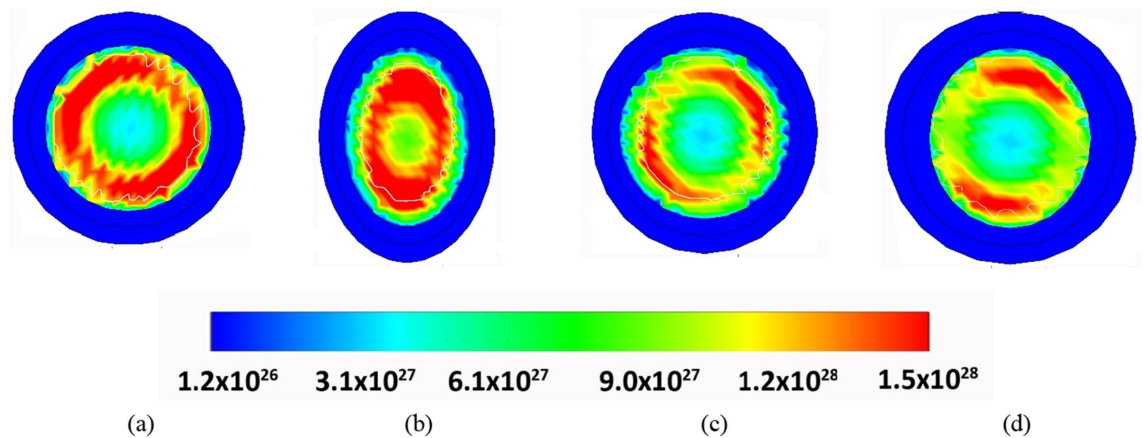

Figure 8. Band generation rate of carriers for (**a**) COCC, (**b**) EOEC, (**c**) EOCC, and (**d**) COEC.

section. It is observed from Fig. 8a that the COCC structure has an accumulation of band-to-band generated tunneling carriers from all sides of the gate in a circular fashion and are generally present near the semiconductor-dielectric interface. Whereas, due to the vertical electric field of EOEC structure penetrating more at the center of the device as depicted in Fig. 8b, which results in tunneling of the carrier at the center of the device rather than near the semiconductor-dielectric interface[32]. As a result, the carrier density increases at the center of the device which narrows the tunneling width at the source-channel junction as depicted in Fig. 6b[33]. Therefore, the band-to-band generated tunneling carriers take the shape of the elliptical channel and the accumulated carriers shift from the semiconductor-dielectric interface to the center of the device[34].

For EOCC structure depicted in Fig. 8c shows that the vertical electric field penetrated more into the region where T_{OX} is minimum causing carriers to accumulate at the region where T_{OX} is minimum. Finally, for COEC structure depicted in Fig. 8d, band-to-band generated carriers follow the same phenomenon stated for Fig. 8b,c considering the dominancy of either channel MD of EOEC structure or T_{OX} of EOCC structures. However, the device having channel MD of 18 nm of COEC structure shows that the carriers are accumulating below the major axis where T_{OX} is fixed at 2 nm[17,32]. The vertical electric field penetrates more with decreasing channel MD of EOEC structure resulting in an increase in its carrier density[33] as depicted in Fig. 9a. As electron density increases cause more carriers to tunnel from the valence band of the source to the conduction band of the channel, which enhances the tunneling probability of carrier at the source to channel junction[35]. The insertion in Fig. 9a shows the increment in drain current density of optimized EOEC from ~ 3 nA/(nm)^2 to ~ 6 nA/(nm)^2 from its circular counterpart.

In the case of varying T_{OX} keeping fixed channel MD of 20 nm of EOCC structure causes faster accumulation of the carrier density near the semiconductor-dielectric interface where T_{OX} is minimum as depicted in Fig. 9b. However, the gradual increase in the electrostatic control of the EOCC structure shows an increment in its drain current density with a decrease in T_{OX} of the device along MA. The insertion in Fig. 9b shows the increase in the drain current density from ~ 3 nA/(nm)^2 to ~ 5 nA/(nm)^2 when compared to COCC structure.

On the contrary, the COEC structure shows an unpredictable trend even after keeping the outer diameter fixed at 24 nm. It is evident from Fig. 8d that, varying channel MD causes virtual variation in T_{OX} of the device which leads to accumulation of carrier density depending on the dominancy of either channel MD or T_{OX} of the device. Result of our simulation shown in Fig. 9c shows that when channel MD is 10 nm then T_{OX} along the channel MD is maximum and has a drain current density of ~ 2.2 nA/(nm)^2 whereas with the gradual increase in channel MD from 10 to 14 nm shows the effect of T_{OX} on the device is relatively higher than the variation of MD of the channel on the device. As a result, drain current density decreases from ~ 2.2 to ~ 1.9 nA/(nm)^2 from channel MD of 10 nm to 14 nm. However, when channel MD increases beyond 14 nm, the impact of variation of channel MD is more in the device when compared to the virtual variation of T_{OX} along MA. The enlarged view under Fig. 8c depicts that, the drain current density increases beyond 14 nm whereas the optimized COEC structure shows a drain current density of ~ 2.4 nA/(nm)^2.

For the evaluation of the transconductance (g_m) and the drain conductance (g_D) of the III-V eGAA-TFETs, the following expressions are used,

$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}}, \tag{1}$$

$$g_D = \frac{\partial I_{DS}}{\partial V_{DS}} \tag{2}$$

The g_m and g_D expressions depend on the change in I_{DS} with changing applied port biasing of TFET[33]. However, the dependency on I_{DS} further led to a dependency on the tunneling probability of the carriers at the source-to-channel junction, effective mobility (μ_{eff})(μ_{eff}), tunneling barrier width, or average tunneling thickness (λ)(λ) of the device.

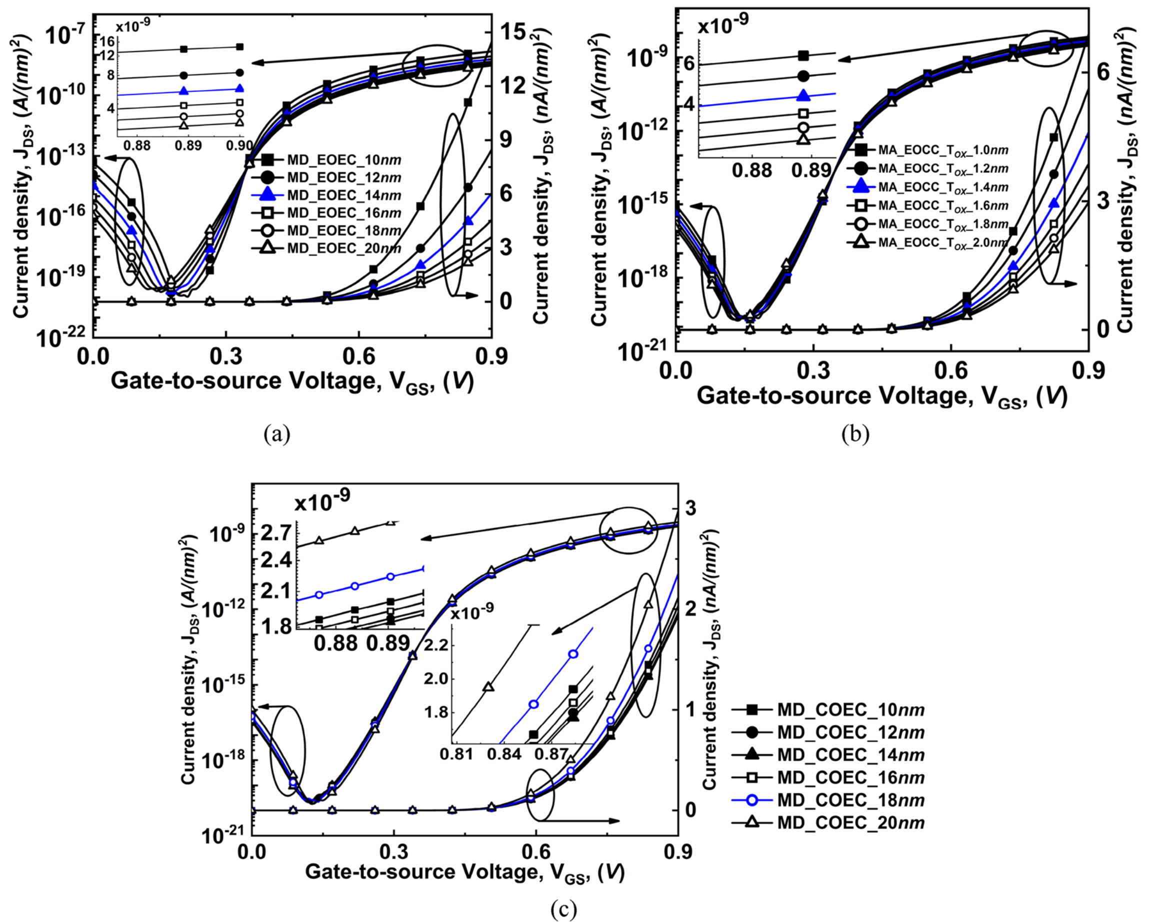

Figure 9. Comparison of variation of drain current density (J_{DS}) as a function of gate-to-source voltage at V_{DS} = 0.3 V of COCC structure with (a) EOEC, (b) EOCC, and (c) COEC structure.

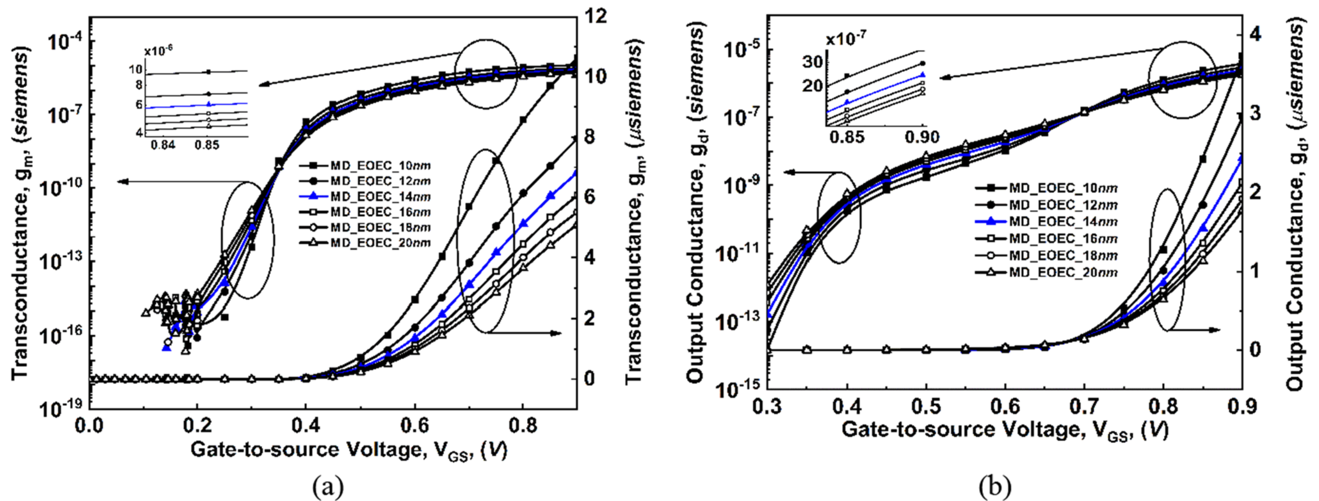

Figure 10. Comparison of variation of transconductance (g_m) and output conductance (g_d) as a function of gate voltage at V_{DS} = 0.3 V for EOEC devices: (a) g_m, and (b) g_d.

For EOEC and EOCC structures, their tunneling barrier width becomes narrower which increases the tunneling probability, thereby, g_m and g_D show a rapid increase with V_{GS} as shown in Fig. 10 and Fig. 11. On the other hand, for COEC structure, their tunneling barrier width depends on both the variations (channel MD and T_{OX}) which result in a decrease in g_m and g_D till 14 nm than a gradual increase beyond 14 nm along channel MD of the device as shown in Fig. 12.

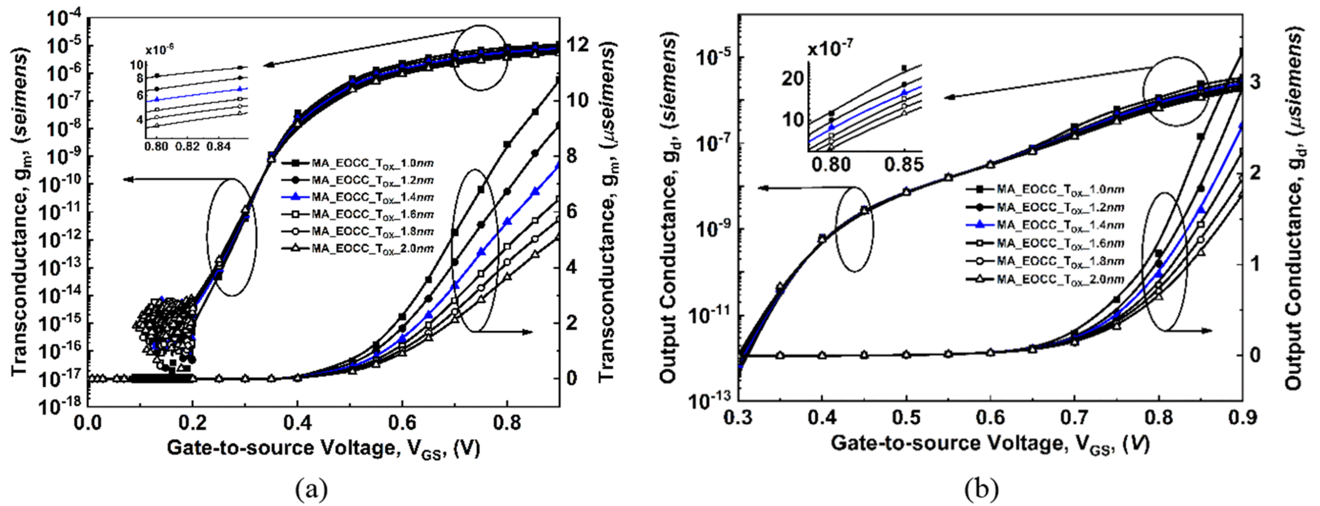

Figure 11. Comparison of variation of transconductance (g_m) and output conductance (g_d) as a function of gate voltage at $V_{DS} = 0.3$ V for EOCC devices: (**a**) g_m, and (**b**) g_d.

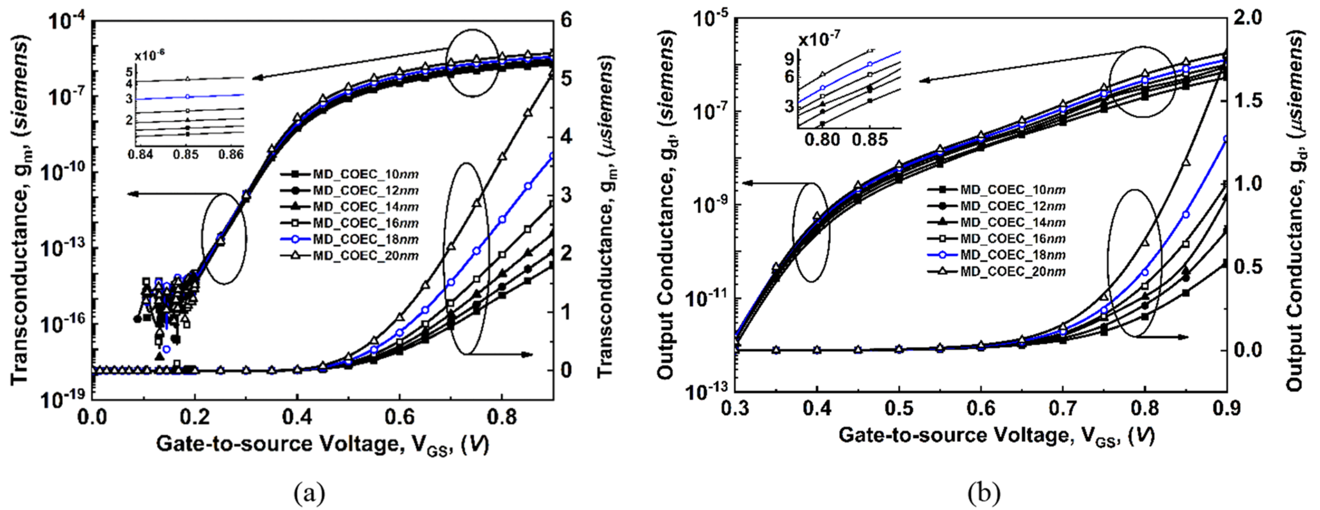

Figure 12. Comparison of variation of transconductance (g_m) and output conductance (g_d) as a function of gate voltage at $V_{DS} = 0.3$ V for COEC devices: (**a**) g_m, and (**b**) g_d.

The performance parameters of available gain per unit value of power dissipation, quality factor (g_m/I_{DS})[35], and intrinsic gain (g_mR_O)[30] of the device as a function of V_{GS} at $V_{DS} = 0.3$ V are shown in Fig. 13. Since, g_m and g_D increase with increasing V_{GS}, therefore with a decrease in channel MD and T_{OX} of EOEC and EOCC structures show a significant increase in g_m/I_{DS} and g_mR_O characteristics. On the other hand, g_m and g_D of COEC structure decreases when channel MD decreases from 14 to 10 nm whereas when channel MD decreases from 20 to 14 nm causes an increase in g_m and g_D of COEC structure therefore, g_m/I_{DS} and g_mR_O first decrease from 20 to 14 nm channel MD then it increases from 14 to 10 nm channel MD for COEC structure.

For g_m/I_{DS} in the subthreshold region, the transconductance and the drain currents for both variations are negligible. However, the peak of the g_m depicts the threshold voltage of the device. From Eq. (2), the drain conductance of the device depends on the tunneling current of TFET[33]. Therefore, increasing the tunneling carrier at the source-to-channel junction causes g_D of the device to increase, which consequently leads to the reduction of output resistance (R_O) of the device. It is observed from Fig. 13a that the optimized EOEC structure shows an increment in g_m/I_{DS} from ~ 86 V^{-1} to ~ 117 V^{-1} and an increment in g_mR_o from ~ 33 to ~ 90 respectively when compared to COCC structure. Moreover, Fig. 13b depicts, the increment in g_m/I_{DS} of optimized EOCC from ~ 86 to ~ 96 V^{-1} and increment in g_mR_o from ~ 33 to ~ 79 respectively when compared to COCC structure. Finally, Fig. 13c depicts the COEC structure where g_m/I_{DS} and g_mR_o first decreases from ~ 86 V^{-1} and ~ 33 (MD = 20 nm) to ~ 78 V^{-1} and ~ 21 (MD = 14 nm) then g_m/I_{DS} and g_mR_o increases to ~ 79 V^{-1} and ~ 24 respectively. The insertion in Fig. 13c shows the optimized COEC structure having g_m/I_{DS} and g_mR_o as ~ 81 V^{-1} and ~ 27 respectively.

Effect of process variation on RF performance parameter. The comparison of variations on EOEC, EOCC, and COEC from its equivalent COCC structure has substantially boosted the RF performance param-

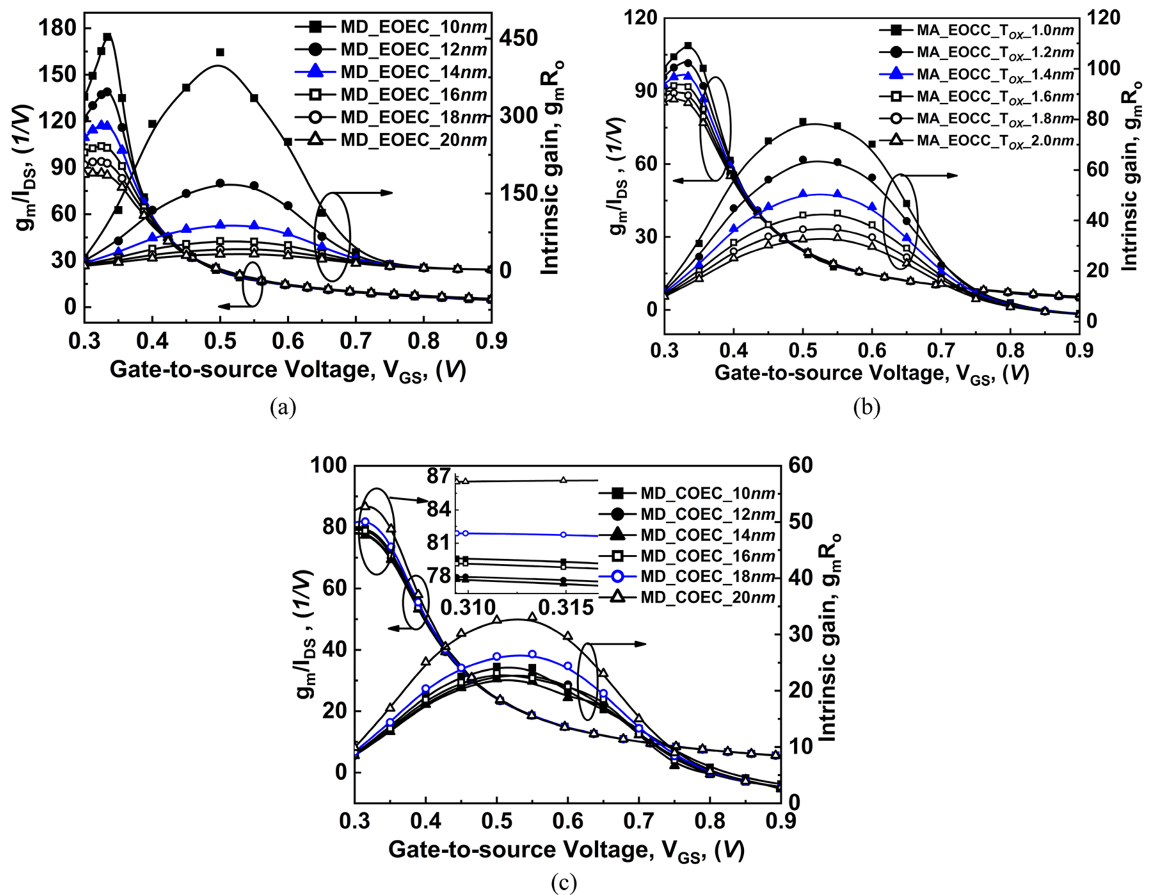

Figure 13. Comparison of variation of transconductance generation factor and intrinsic gain as a function of gate voltage at $V_{DS} = 0.3$ V of COCC structure with: (**a**) EOEC, (**b**) EOCC, and (**c**) COEC structures.

eters. The performance variation of C_{GD}, C_{GS}, and C_{GG}, along with cut-off frequency (f_T) and gate delay (τ_m) is analyzed in this section.

For a fixed V_{DS}, the depletion region at the source-to-channel region is formed due to reverse biasing of the source-to-channel junction, which gives rise to C_{GS}[36]. However, at low V_{GS}, the depletion charge near the drain side decreases with a decrease in the area of the channel, which causes a decrease in C_{GD}. When high V_{GS} is applied, the channel area decreases, causing a negligible change in inversion charge at the source end. As a result, C_{GS} decreases with a decrease in the area of the channel. Whereas, the inversion charge increases with a decrease in the area of the channel at high V_{GS}. Therefore, C_{GD} increases with a decrease in the area of the channel[37].

The variation of C_{GS} along with C_{GD} as a function of V_{GS} for EOEC, EOCC, and COEC structures is plotted in Fig. 14. For a fixed V_{DS}, when channel MD of the EOEC structure decreases from 20 to 10 nm, it causes a decrease in the area of the GAA structure, which consequently reduces the depletion charge at the source-to-channel junction at low V_{GS}. Whereas, at high V_{GS}, a decrease in channel MD shows negligible variation in the inversion charge at the source end. As a result, C_{GS} decreases with the decrease in channel MD of the EOEC structure. The optimized EOEC structure shows a decrease in C_{GS} from ~ 4.5 to ~ 3.5 aF when compared to the COCC structure. On the other hand, a decrease in channel MD of the EOEC structure at low V_{GS} causes a negligible change in depletion charge at the drain-to-channel region. Therefore, C_{GD} follows the same trend with a decrease in channel MD of the EOEC structure. However, at high V_{GS}, inversion charge experiences a sudden increase therefore, C_{GD} experiences cross-over and increases with a decrease in channel MD of EOEC structure from ~ 34 to ~ 37 aF when compared to COCC structure as depicted in Fig. 14a.

For the EOCC structure, at low V_{GS}, decreasing the T_{OX} along MA shows a negligible change in its inversion charge at the source end. As a result, C_{GS} shows negligible variation at low V_{GS}. On the other hand, at high V_{GS}, decreasing T_{OX} causes a gradual increment in the electric field which subsequently increases the inversion charge near the drain end. Thus, C_{GD} increases with decreasing T_{OX} for EOCC structure which leads to an increase in C_{GD} from ~ 34 to ~ 43 aF when compared to its COCC structure as depicted in Fig. 14b.

On the contrary, unlike the analog performance parameter, the RF performance of COEC follows the predictable trend due to its dependency on the area and T_{OX} of the GAA structure. As the reason stated, the source side depletion charge at low V_{GS} increases with decreasing channel MD of COEC structure, however it experiences slight reduction with virtual increment in T_{OX} where depletion charge at source end is dominated by the variation of channel MD of COEC structure. Furthermore, at high V_{GS}, the inversion charge experiences a slight increment at the source side with decreasing channel MD. Therefore, C_{GS} is dominated and decreases with decreasing

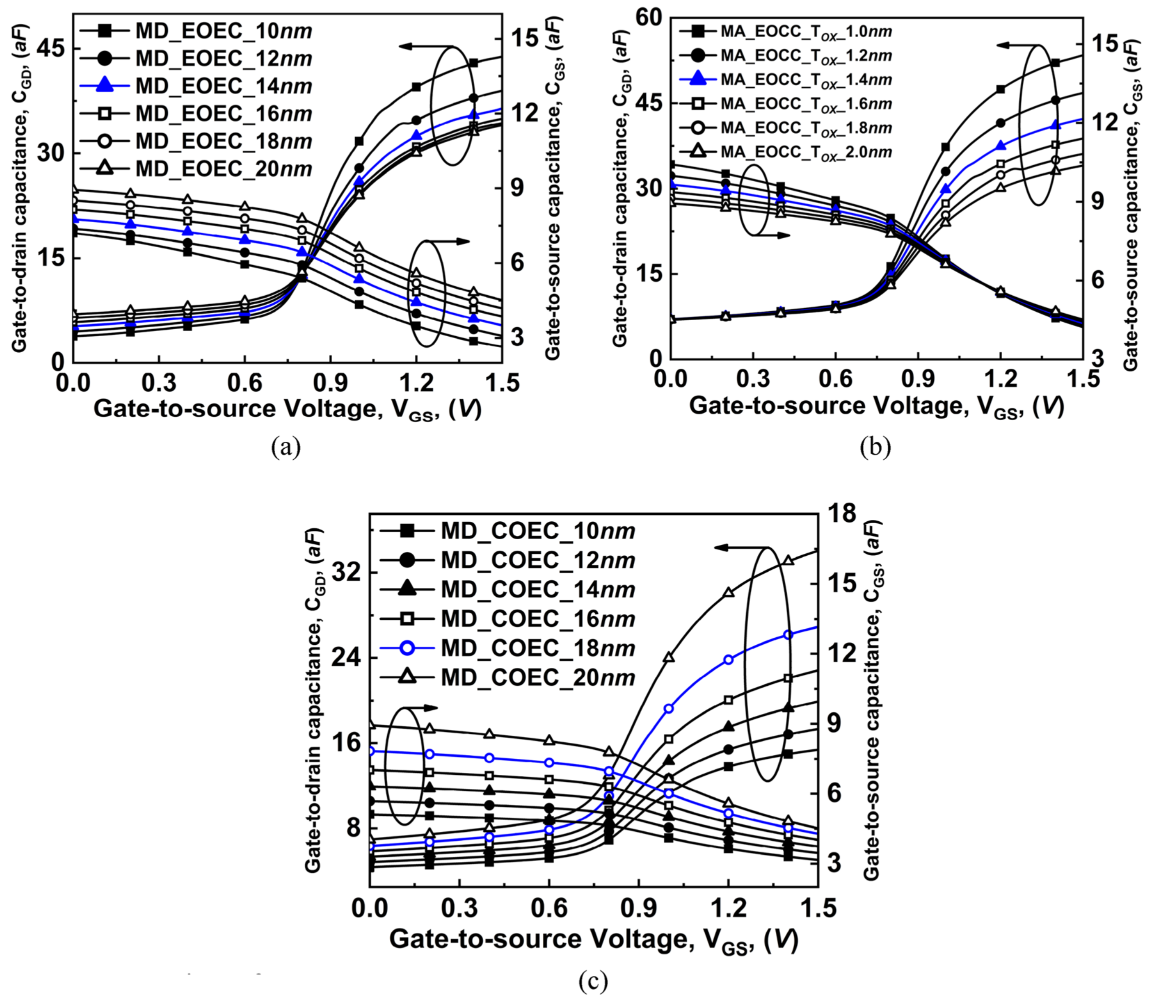

Figure 14. Comparison of variation of gate-to-source capacitances and gate-to-drain capacitances as a function of gate voltage at $V_{DS} = 0.3$ V of COCC structure with (**a**) EOEC, (**b**) EOCC, and (**c**) COEC structures.

channel MD of COEC structure. The optimized COEC structure shows a decrement in C_{GS} from ~ 4.5 to ~ 4.2 aF when compared to COCC structure. As channel MD of COEC is dominated by virtual variation of $T_{OX,}$ therefore, at high V_{GS}, C_{GD} experiences sudden decrement in inversion charge when compared to its circular structure with a decrease in C_{GD} from ~ 34 to ~ 27 aF from COCC structure as depicted in Fig. 14c.

The total capacitance $C_{GG} = C_{GS} + C_{GD}$ ($C_{GG} = C_{GS} + C_{GD}$) is plotted in Fig. 15 which follows the variation in C_{GD} as depicted in Fig. 14. It is evident from Fig. 15 that, C_{GG} follows the C_{GD} graph which is the dominant contributor to total gate capacitance for any variation in COCC, EOEC, EOCC, and COEC structures. At high V_{GS}, C_{GG} is almost the same as C_{GD} whereas, at low V_{GS}, C_{GG} shows the same trend as C_{GS} which is higher in magnitude at low V_{GS}.

The cutoff frequency (f_T) and the gate delay (τ_m) are other parameters for the analysis of RF performances. The cutoff frequency and the gate delay are defined by

$$f_T = \frac{g_m}{2\pi(C_{GS} + C_{GD})} \tag{3}$$

$$\tau_m = \frac{C_{GG} V_{DD}}{I_{ON}} \tag{4}$$

From the f_T expression (3), it is evident that it depends on the transconductance (g_m) and the total capacitance $C_{GG} = C_{GS} + C_{GD}$ values, which is a function of V_{GS}[38]. The characteristics of f_T are explained explicitly for the subthreshold and superthreshold regions for all device structures. It is observed from Fig. 15 that in the weak inversion region, for each variation, the value of the intrinsic capacitance is low. However, the value of g_m increases rapidly in the weak inversion region for variation in any device structure. Therefore, the value of f_T at a low V_{GS} value is dominated by the value of g_m as shown in Fig. 16. Whereas, in the strong inversion region, the intrinsic capacitance value shows a rapid increase with V_{GS}. However, the g_m of the device is almost invariable at the strong inversion region. Thus, in strong inversion, the f_T parameter is dominated by the value of intrinsic

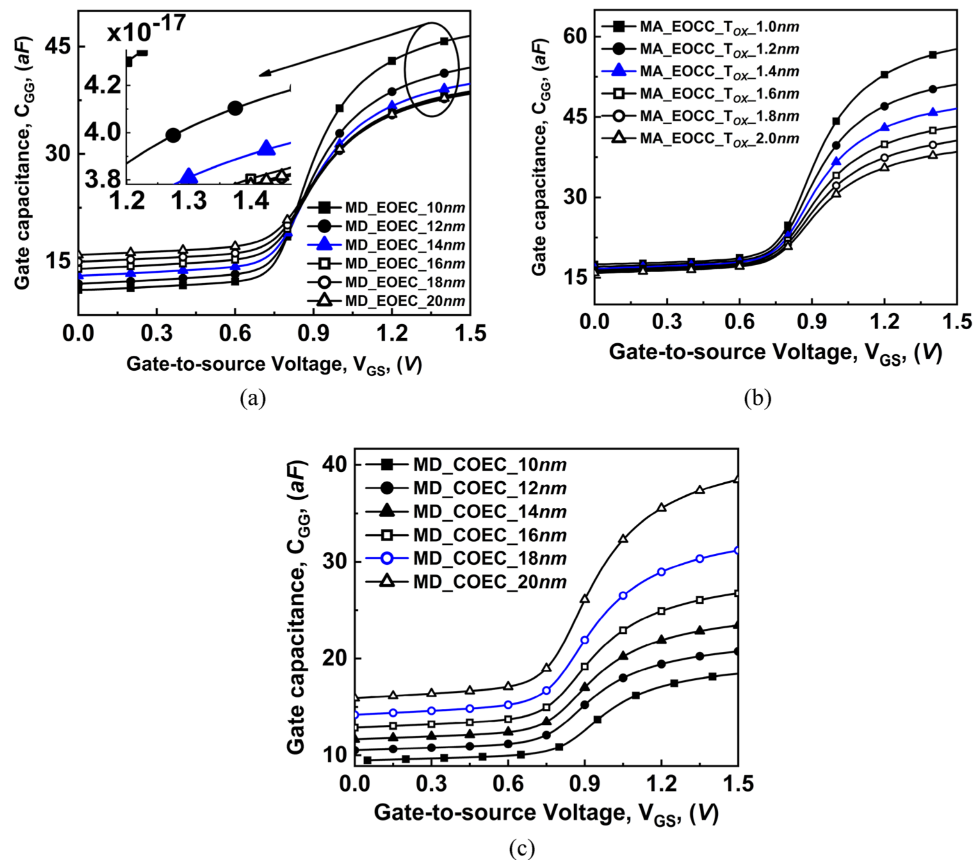

Figure 15. Comparison of variation of total gate capacitance as a function of gate voltage at $V_{DS} = 0.3$ V of COCC structure with: (**a**) EOEC, (**b**) EOCC, and (**c**) COEC structures.

capacitance. Results of the simulation depicted in Fig. 16a that, with the decrease in the channel MD of the EOEC structure, the f_T of the device increases where the optimized EOEC structure shows increment from ~31 to ~43 GHz cutoff frequency and increment from ~31 to ~40 GHz cutoff frequency on EOCC structure when compared to COCC structure. On the other hand, for the COEC structure, intrinsic capacitance is relatively higher. Therefore, the value of f_T at a low V_{GS} value has an impact on both the intrinsic capacitance and the g_m of the device. As a result, the decrease in MD of the COEC structure causes a decrease in f_T of the device where the optimized COEC structure shows a decrement from ~31 to ~26 GHz when compared to its circular structure as shown in Fig. 16c.

The variation of gate delay (τ_m) as a function of V_{GS} is also plotted in Fig. 16. The gate delay expression (4) stated earlier has supply voltage (V_{DD}), gate capacitance (C_{GG}), and ON-state current (I_{ON}) dependence.

It is observed from Fig. 15a that, with a decrease in channel MD of EOEC structure causes C_{GG} and drain current to increase following the reason stated in analog performance. The rate of increase of drain current is dominated by the increase in C_{GG} of the device, which consequently reduces the τ_m. The insertion in Fig. 16a depicts the decrease in the τ_m of optimized EOEC structure from ~8.5 to ~5.5 psec when compared to COCC structure. For EOCC structure, shows an increment in both C_{GG} as well as drain current with decreasing T_{OX} of the device. Likewise, considering the case of EOEC, the drain current of the EOCC structure shows dominating parameter when compared to the C_{GG} of the device followed by a reduction in τ_m as depicted in Fig. 16b. The enlarged view under Fig. 16b shows the reduction of optimized gate delay from ~8.5 to ~6.3 psec when compared to its circular structure. Finally, for the COEC structure, variation in channel MD causes virtual variation in T_{OX} which in turn reduces C_{GG} and drain current of the device. Likewise, the drain current shows dominating nature when compared to C_{GG} which further led to an increase in τ_m of the device as depicted in Fig. 16c. The insertion in Fig. 16c shows the optimized COEC gate delay from ~8.5 to ~10 psec when compared to the COCC structure.

Benchmarking of proposed EOEC and COCC structures against several GAA MOSFETs and TFETs reports. This section presents a status map of numerous reports available on elliptical or circular GAA MOSFETs and TFETs against the analyzed EOEC and COCC structures as tabulated in Table 2. The status map shows that there is a drastic decrease in I_{ON} for GAA TFET when compared to its GAA MOSFET counterpart. This drastic decrease is due to different carrier injection mechanisms as well as comparatively lower V_{DS} applied to the device. On the other hand, the device under consideration also has a lower I_{ON} when compared to its TFET counterpart. This lower I_{ON} is due to the lower V_{DS} applied to the device under consideration. However, the device shows significantly reduced gate capacitance, which is the crucial parameter for any device's perfor-

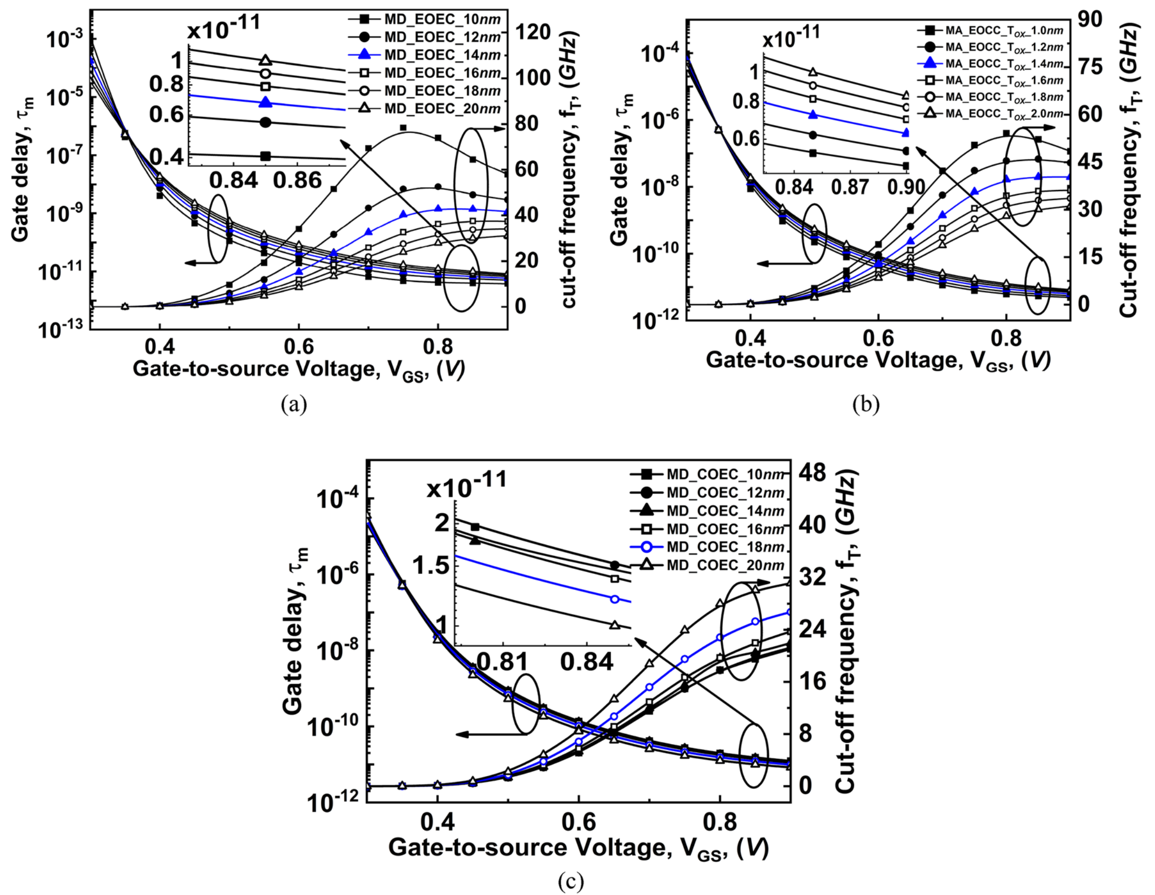

Figure 16. Comparison of variation of cut-off frequency and gate delay as a function of gate voltage at $V_{DS} = 0.3$ V of COCC structure with: (**a**) EOEC, (**b**) EOCC, and (**c**) COEC structures.

	This work		Ref.[12]	Ref.[13]	Ref.[15]	Ref.[14]	Ref.[9]	Ref.[39]	Ref.[40]
Geometry	**COCC TFET**	**EOEC TFET**	**EOEC MOSFET**	**EOEC MOSFET**	**EOEC MOSFET**	**COCC MOSFET**	**COCC TFET**	**DG TFET**	**COCC TFET**
Diameter (nm)	20	14	~20.4	~12.8	~13.9	~3	10	–	20
L_G (nm)	30	30	~35	~25	~25	10	20	100	50
EOT or T_{OX} (nm)	2	2	1.5	~1.12	~1.4	1	2	2	2
V_{DS} (V)	0.3	0.3	1	1	1	0.4	1	1	1
I_{ON} (μA/μm)	~32	~44	825	976	600	~1180	244	148	200
I_{ON}/I_{OFF}	3.4×10^{13}	1.9×10^{11}	2×10^{5}	9.7×10^{5}	6×10^{7}	1.4×10^{5}	1.3×10^{8}	1.8×10^{11}	7.12×10^{12}
g_m (mS)	~0.051	~0.069	–	–	–	–	–	0.1	0.55
C_{GG} (fF)	0.041	0.037	–	–	–	–	–	1.1	2.5
f_T (GHz)	32	44	–	–	–	–	–	–	40

Table 2. Details of proposed EOEC and COCC structures against several GAA MOSFETs and TFETs.

mance. Besides the lower I_{ON}, the device under consideration shows a drastic increase in the I_{ON}/I_{OFF} ratio. This high I_{ON}/I_{OFF} determines the switching speed of the device."

Conclusion

The optimization of the structure and the comparative analysis of analog and RF FOMs for the III-V eGAA TFET with its EOEC, EOCC, and COEC structures are performed. Further optimization and comparative analysis of the analog and RF FOMs of the device is done for various EOEC, EOCC, and COEC structures. The device shows comparatively higher mobility, lower parasitic capacitances, and a minimum possible gate delay of the optimized geometries. When compared to their circular structures, the optimised EOEC and EOCC devices show a 64% and 59% increase in intrinsic gain, respectively, and a 28% and 23% increase in cut-off frequency. On the other hand, the optimized COEC structure shows a reduction in its intrinsic gain and its cut-off frequency.

However, the physics behind the extracted output characteristics depends upon the dominancy of T_{OX} and MD of the COEC structure. Owing to the higher gain and cut-off frequency of the EOEC and EOCC structures, the proposed optimized device can be an alternative structure that meets the need for higher performance for analog RF CMOS circuit applications. To summarize, the advantage of the undesired fabrication issue up to a certain level (MD up to 30% for EOEC, T_{OX} up to 30% for EOCC, and MD up to 10% for COEC structures), which enhances the analog and RF FOMs, can be passed on to the circuit design where high gain, higher drive current, and higher gain bandwidth product are desired, and thus, the unintentional elliptical device structure proves to be the promising choice for analog/RF application.

Data availability

The datasets generated and/or analyzed during the current study are available from the author Pankaj Kumar (iitdhn.pankaj@gmail.com) upon reasonable request.

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Author contributions
P.K. and K.K. conceived the idea and reviewed and edited the manuscript. P.K. performed device simulations and wrote the initial draft of the manuscript. P.K., K.K. and B.C.M. analyzed the data and figure generation. A.M. and S.K. reviewed and edited the manuscript with the help of all co-authors.

Competing interests
The authors declare no competing interests.

Additional information
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