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# Logic and memory functions of an inverter comprising reconfigurable double gated feedback field effect transistors

Juhee Jeon, Sola Woo, Kyoungah Cho &amp; Sangsig Kim✉

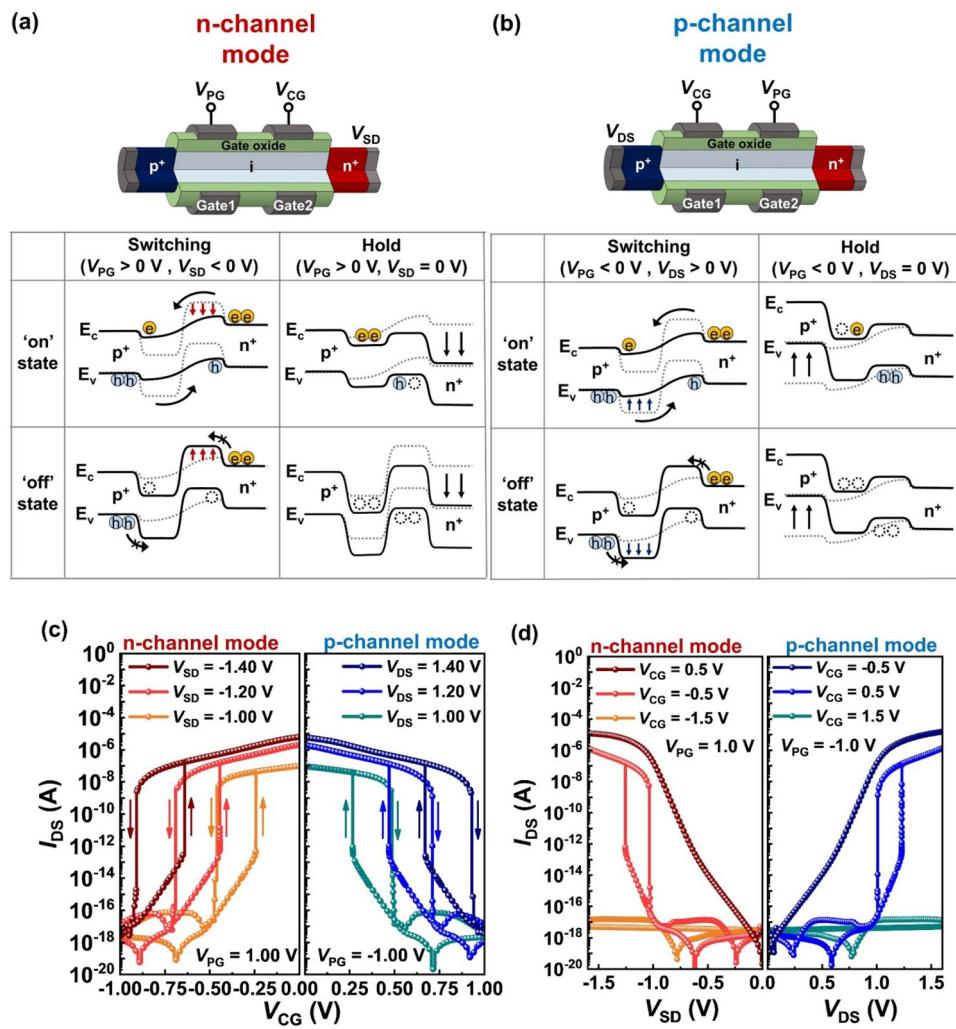
In this study, we propose an inverter consisting of reconfigurable double-gated (DG) feedback field-effect transistors (FBFETs) and examine its logic and memory operations through a mixed-mode technology computer-aided design simulation. The DG FBFETs can be reconfigured to n- or p-channel modes, and these modes exhibit an on/off current ratio of  $\sim 10^{12}$  and a subthreshold swing (SS) of  $\sim 0.4$  mV/dec. Our study suggests the solution to the output voltage loss, a common problem in FBFET-based inverters; the proposed inverter exhibits the same output logic voltage as the supply voltage in gigahertz frequencies by applying a reset operation between the logic operations. The inverter retains the output logic '1' and '0' states for  $\sim 21$  s without the supply voltage. The proposed inverter demonstrates the promising potential for logic-in-memory application.

Recently, researchers have researched logic-in-memory (LIM) architectures using reconfigurable field-effect transistors (RFETs) combined with ferroelectric materials<sup>1,2</sup>. The use of ferroelectric materials has allowed RFETs to possess memory characteristics while maintaining reconfigure behavior which switches n- and p-channel operation modes at transistor level<sup>3–6</sup>. As the reconfigurable behavior reduces the number of component transistors required for logic functionality in LIM architecture<sup>7–10</sup>, it enhances the logic functionality per circuit and enables various circuit topologies of LIM architecture<sup>1</sup>.

More recently, single-gated (SG) feedback field-effect transistors (FBFETs) operating in positive feedback mechanism have been researched to develop LIM architecture<sup>11</sup>. SG FBFETs have exhibited extremely low SS<sup>12,13</sup>, and the positive feedback mechanism enables SG FBFETs to perform logic and memory operations in LIM architecture comprising these transistors<sup>11,14</sup>. However, SG FBFETs have not exhibited desired reconfigurable behavior. Thus, in this study, we propose reconfigurable double-gated (DG) FBFETs and LIM operation of an inverter comprising these transistors. The DG FBFETs can be fabricated by CMOS-compatible top-down technology<sup>19</sup>. To demonstrate the LIM operation, transient simulations are performed through mixed-mode technology computer-aided design (TCAD) simulation. Moreover, by applying a reset operation, the inverter exhibits the LIM operation without the output voltage loss, a common problem in the FBFET-based inverters<sup>12,15</sup>.

**Simulation method.** Our simulation was carried out with a two-dimensional structure using a commercial device simulator, Synopsys Sentaurus (O\_2018.06)<sup>16</sup>. A DG FBFET had a p-i-n silicon nanowire (SiNW) structure with two gate electrodes (for details, see supplementary information). We used the thin layer mobility, the Lombardi, Philips unified mobility, and the high-field saturation model for considering the doping and field dependences of carrier mobility. Fermi statistics was applied to perform an accurate simulation. We also considered bandgap narrowing (default model), Shockley–Read–Hall (SRH) recombination with concentration-dependent lifetimes, Surface SRH recombination, and Auger recombination. Furthermore, the area factor of 12 nm was specified in the simulation for assuming the width of the transistor. In this study, we excluded the band-to-band-tunneling (BTBT) model because the BTBT is negligible in the DG FBFETs (for details, see supplementary information). In addition, the quantum confinement model was not considered because the dimension of the device is larger than the Fermi wavelength<sup>20</sup>.

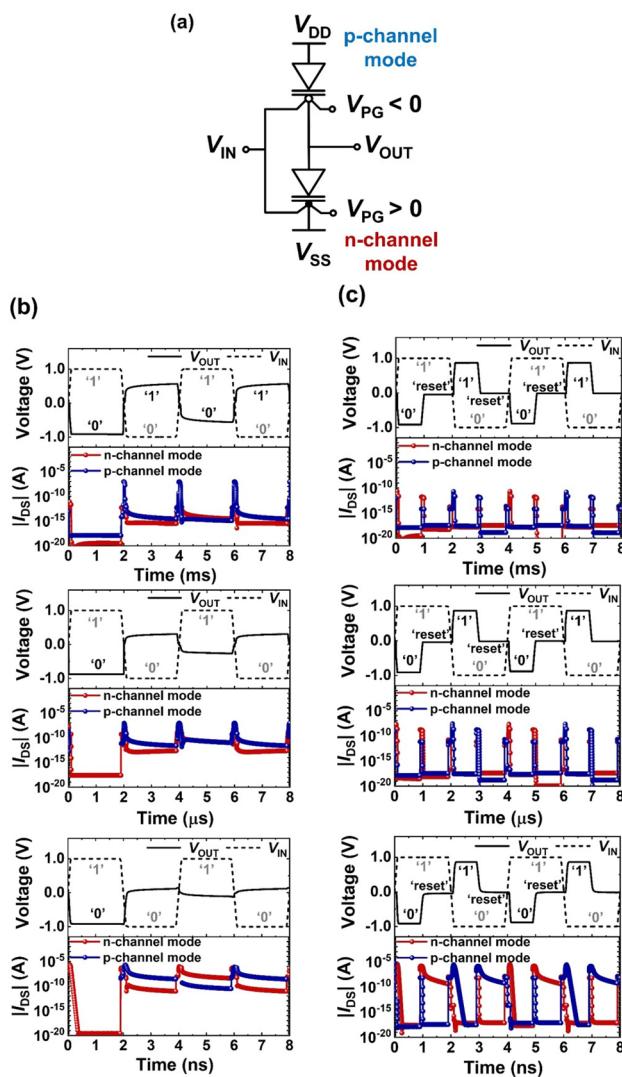
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**Figure 1.** The operation mechanism of the reconfigurable double-gated feedback field-effect transistor (DG FBFFET). The schematic illustration of the reconfigurable switching and holding operations in the (a) n- and (b) p-channel modes. (c) Transfer and (d) output characteristics for the n- and p-channel modes.

## Results and discussion

**Switching and holding mechanisms of reconfigurable double-gated feedback field-effect transistors.** Figures 1a and b show the schematics and band diagrams of the reconfigurable DG FBFFETs during the switching and hold operations in the n- and p-channel modes. In the n-channel mode (Fig. 1a), gate1 operates as the program gate, whereas gate2 operates as the control gate. The positive bias of the program gate induces the virtual n-doped region in the intrinsic channel to block the hole injection from the drain. When a control-gate voltage ( $V_{CG}$ ) is positively swept with the negative source-to-drain voltage ( $V_{SD}$ ), electrons in the source are injected into the channel owing to the lowering of the potential barrier in the control-gated channel. The accumulation of electrons lowers the potential barrier in the program-gated channel, allowing the hole injection. As the potential barrier suddenly decreases due to the positive feedback loop, the transistor switches to the 'on' state with the latch-up phenomenon. However, when  $V_{CG}$  is negatively swept, the potential barrier suddenly rises with the elimination of the positive feedback loop. As a result, the transistor switches to the 'off' state with the latch-down phenomenon. During the 'on' state, excess charge carriers are accumulated in the potential well in the channel. When  $V_{SD}$  and  $V_{CG}$  are varied to 0 V, some holes release from the control-gated channel, but electrons remain in the program-gated channel because of the constant positive  $V_{PG}$  bias. Thus, the potential barrier in the program-gated channel is low enough to trigger the positive feedback loop. During the 'off' state, excess charge carriers are removed from the potential well in the channel. Thus, the potential barrier of the channel region is high enough to prevent the positive feedback loop at  $V_{SD} = V_{CG} = 0 \text{ V}$ . In the p-channel mode (Fig. 1b), the position and polarity of the program- and control-gate are reversed. The negative  $V_{PG}$  (gate2) induces the virtual p-doped region that impedes the electron injection from the source. When a  $V_{CG}$  is negatively swept with the positive drain-to-source voltage ( $V_{DS}$ ), holes in the drain are injected into the channel, and then the transistor switches to the 'on' state with the latch-up phenomenon. Conversely, a positively swept  $V_{CG}$  leads to the switching 'off' operation with the latch-down phenomenon. When  $V_{SD}$  and  $V_{CG}$  are varied to 0 V in the 'on'

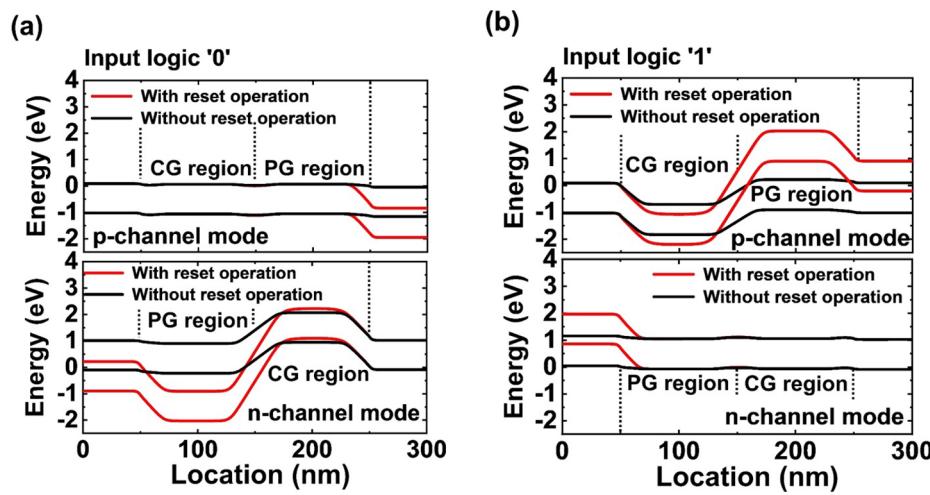


**Figure 2.** (a) Schematic of the inverter comprising the reconfigurable DG FBFETs. (b) Timing diagrams of the non-full swing inverting logic operation with ms,  $\mu$ s, and ns time steps under static conditions (a  $V_{DD}$  of 1.0 V, a  $V_{SS}$  of -1.0 V, and a  $|V_{PG}|$  of 1.0 V). (c) Timing diagrams of the full swing inverting logic and reset operations with ms,  $\mu$ s, and ns time steps. The reset operation between the logic operations is carried out to eliminate the accumulated charge carriers; the reset operation takes place with  $V_{IN} = 1.0$  V and  $V_{PG} = V_{DD} = V_{SS} = 0.0$  V for the output logic '0', and  $V_{IN} = -1.0$  V and  $V_{PG} = V_{DD} = V_{SS} = 0.0$  V for the output logic '1'.

state, the stored excess holes remain in the program-gated channel, lowering the potential barrier height enough to trigger the positive feedback loop. By contrast, for the 'off' state, the absence of excess charge carriers leads to a high potential barrier enough to prevent the positive feedback loop at  $V_{SD} = V_{CG} = 0$  V.

Figure 1c shows the transfer characteristics of the reconfigurable DG FBFETs in the n- and p-channel modes. In the n-channel mode ( $V_{PG} = 1.0$  V), as a  $V_{SD}$  varies from -1.00 to -1.40 V, the 'switching on' voltage ( $V_{on}$ ) shifts from -0.24 to -0.64 V. Contrary, in the p-channel mode ( $V_{PG} = -1.0$  V), as a  $V_{DS}$  varies from 1.00 to 1.40 V,  $V_{on}$  shifts from 0.27 to 0.67 V. The shift of  $V_{on}$  is owing to the decrease in the potential barrier height between the drain (or source) and program-gated region. Moreover, for both channel modes, the transistor exhibits a constant memory window of  $\sim 0.25$  V regardless of  $V_{DS}$  (or  $V_{SD}$ ). The transistor also exhibits an on/off current ratio of  $\sim 10^{12}$  and a subthreshold swing (SS) of  $\sim 0.4$  mV/dec at a  $V_{DS}$  ( $|V_{SD}|$ ) of 1.00 V for the p-channel (n-channel) mode. The output characteristics in the n- and p-channel modes are shown in Fig. 1d. When a  $V_{CG}$  of 0.5 V for the n-channel mode and -0.5 V for the p-channel mode is applied, the output characteristics are similar to the current–voltage characteristics of a p-n diode. However, when a  $V_{CG}$  of -0.5 V for the n-channel mode and 0.5 V for the p-channel mode are applied, the transistor exhibits the latch-up and -down phenomena. Moreover, the transistor is in the 'off' state when  $V_{CG}$  is -1.5 V for the n-channel mode and 1.5 V for the p-channel mode.

**Reset operation in the logic inverter comprising reconfigurable DG FBFETs.** Figure 2a shows a circuit of the inverter comprising the reconfigurable DG FBFETs. In the proposed inverter, the top transistor



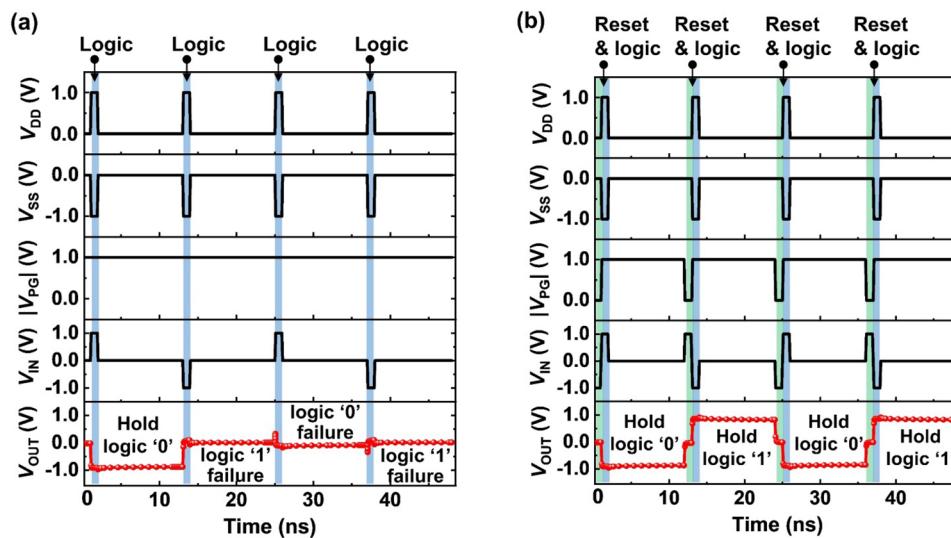
**Figure 3.** Energy band diagrams of the DG FBFETs in the n- and p-channel modes during the (a) input logic '0' and (b) input logic '1'. The reset operation modulates the height of the potential barrier in the channel region. The data were extracted from the timing diagrams of the ns time step in Fig. 2(b) and (c).

operates in the p-channel mode for the pull-up operation, whereas the bottom transistor operates in the n-channel mode for the pull-down operation. The inverter is biased with supply voltages  $V_{DD}$  and  $V_{SS}$  corresponding to the drain voltage of the DG FBFETs in the p-channel mode and the source voltage of the DG FBFETs in the n-channel mode, respectively. The calculated output parasitic capacitance is 18 aF.

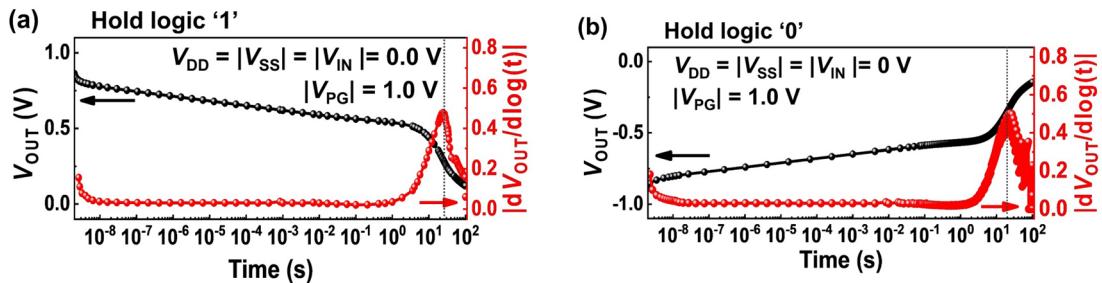
The transient responses of the inverting logic operation with ms,  $\mu$ s, and ns time steps are depicted in Fig. 2b. Under static voltage conditions (a  $V_{DD}$  of 1.0 V, a  $V_{SS}$  of -1.0 V, and a  $|V_{PG}|$  of 1.0 V), input voltages ( $V_{IN}$ ) of 1.0 and -1.0 V are applied for the input logic '1' and '0', respectively. The inverter exhibits a  $V_{SS}$  level at the first output logic '0' state, but an output voltage loss for the subsequent logic '1'. As the time step decreases from milliseconds to nanoseconds, the voltage level of the subsequent logic '1' decreases from 0.6 to 0.1 V. Thus, the output voltage loss increases as the operating frequency increases. This non-full swing characteristic is attributed to the 'data-retaining' behavior that stores charge carriers in the channel of the DG FBFETs. During the pull-down operation at the first input logic '1', charge carriers are accumulated and lower the potential barrier of the DG FBFETs in the n-channel mode. The faster the logic transition speed is, the more difficult it is to remove the accumulated charge carriers. Accordingly, at the subsequent input logic '0', the off-current level of the DG FBFETs in the n-channel mode increases from  $\sim 10^{-15}$  to  $\sim 10^{-11}$  A as the time step decreases from milliseconds to nanoseconds. The situation is similar to the subsequent input logic '1'. However, the output voltage is settled at an intermediate voltage under the millisecond speed since it is hard to remove the accumulated charge carriers even at low frequencies. Hence, in order to resolve the output voltage loss, we use the reset pulse that plays a role in eliminating the accumulated charge carriers between the logic operations.

Figure 2c shows the transient responses of the inverting logic and reset operations with ms,  $\mu$ s, and ns time steps. The reset operation takes place with  $V_{IN} = 1.0$  V and  $V_{PG} = V_{DD} = V_{SS} = 0.0$  V for the output logic '0' state, and  $V_{IN} = -1.0$  V and  $V_{PG} = V_{DD} = V_{SS} = 0.0$  V for the output logic '1' state. During the reset operation, applying a  $V_{PG}$  of 0 V causes the emission of the residual charge carriers. Also, the removed supply voltage prevents unintended charge carrier injection, and an electric field formed in the channel region by  $V_{IN}$  removes the residual charge carriers. This charge carrier emission results in an off-current level of  $10^{-10}$  A in the n-channel (p-channel) transistor during the resetting the output logic '0' ('1') state under the speed of nanosecond order. For the input logic '0' ('1'), the off-current level of the n-channel (p-channel) transistor is  $\sim 10^{-18}$  A after the reset operation, thereby the inverter exhibits a  $V_{DD}$  ( $V_{SS}$ ) level regardless of the operating frequency. Since the output voltage ( $V_{OUT}$ ) at the reset operation is distinctive with the output logic '1' and '0' states, the inverter exhibits three logic states of '1', '0', and 'reset'.

To verify the effect of the reset operation, we analyze the energy band diagrams of the DG FBFETs in the p- and n-channel modes during logic operation under the speed of nanosecond order. For the input logic '0' (Fig. 3a), the DG FBFETs in the p-channel mode is in the 'on' state while the DG FBFETs in the n-channel mode is in the 'off' state. In the DG FBFETs in the n-channel mode, the lowered potential barrier of the program-gated channel indicates that the residual electrons are mainly in the program-gated channel. Thus, resetting the residual electrons leads to the high potential barrier of the DG FBFETs in the n-channel mode enough to suppress the leakage current. Conversely, for the input logic '1' (Fig. 3b), the DG FBFETs in the p-channel mode is in the 'off' state while the DG FBFETs in the n-channel mode is in the 'on' state. Without the reset operation, the presence of the residual holes lowers the potential barrier of the program-gated channel in the DG FBFETs in the p-channel mode. By resetting the residual holes, the DG FBFETs in the p-channel mode exhibits a high potential barrier even at the speed of nanosecond order.



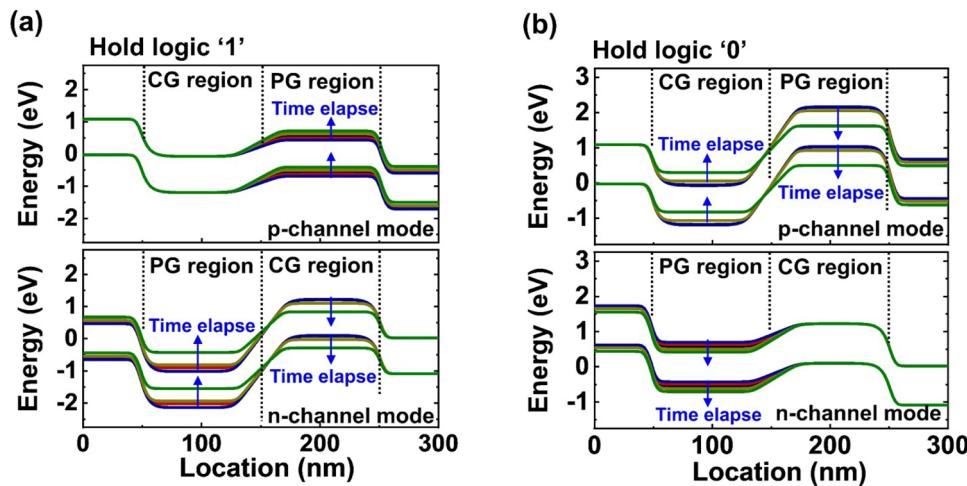
**Figure 4.** (a) Timing diagrams of consecutive logic and hold operations: hold logical data failure. (b) Timing diagrams of consecutive reset, logic and hold operations. The pulses of the drain, source, program-gate, input, and output voltages ( $V_{DD}$ ,  $V_{SS}$ ,  $|V_{PG}|$ ,  $V_{IN}$ , and  $V_{OUT}$ ) are applied with a logic (reset) pulse width of 1 ns and a hold pulse width of 10 ns.



**Figure 5.**  $V_{OUT}$  and  $|dV_{OUT}/d\log(t)|$  for holding the output logic (a) '1' and (b) '0' states. The time to reach maximum  $|dV_{OUT}/d\log(t)|$  represents the retention time.

**Logic and memory operation of the logic inverter.** The presence of the residual charge carriers, which is an obstacle for logical calculation, enables the inverter to store its logical state without the supply voltage. Figure 4 shows the timing diagrams for analyzing the memory ability of the inverter. The blue and green columns indicate the input logic and reset operations, respectively, and both have a pulse width of 1 ns. For the hold operation, the biases of  $V_{IN} = V_{DD} = V_{SS} = 0.0 \text{ V}$  and  $|V_{PG}| = 1.0 \text{ V}$  are applied for 10 ns. When input logic '1' is applied at a  $V_{DD}$  of 1.0 V, a  $V_{SS}$  of -1.0 V, and a  $|V_{PG}|$  of 1.0 V (Fig. 4a), the inverter exhibits a  $V_{SS}$  level as the output logic '0' state. Further, when input and supply voltages are removed,  $V_{OUT}$  consistently retained a  $V_{SS}$  level as the output logic '0' state without any voltage drops. However, when input logic '1' is applied, the following output logic state is indistinguishable because of the output voltage loss. Therefore, the inverter needs a reset operation between the hold and logic operations to perform the memory function properly without failure. When a reset pulse is applied after the hold logic '0' (Fig. 4b)), the output logic transitions from '0' to 'reset' state. Then, applying a  $V_{IN}$  of -1.0 V (with a  $V_{DD}$  of 1.0 V, a  $V_{SS}$  of -1.0 V, and a  $|V_{PG}|$  of 1.0 V) changes the output logic state from 'reset' to '1' for 1 ns without the output voltage loss. Further, the inverter exhibits a  $V_{DD}$  level as the output logic '1' state during the hold operation. After the subsequent reset and input logic '1' pulses,  $V_{OUT}$  retains a constant  $V_{DD}$  level for holding the output logic '1' state.

Figure 5 shows the  $V_{OUT}$  during the holding operation as the semi-log plot. As time increases to 100 s,  $V_{OUT}$  of logic '1' and '0' states reaches 0 V. We consider the time to reach the maximum  $|dV_{OUT}/d\log(t)|$ , i.e., inflection point, as the retention time of the stored logic states; The retention time of the logic '1' and '0' states is the same as ~ 21 s. For the logic '1' ('0'), a slope of  $V_{OUT}$  decrease (increase) is constant until ~ 1 s, and then it increases. The change of the slope is related to the potential barrier collapse of the 'off' state transistor. During holding logic '1' (Fig. 6a), the stored holes leak out slowly from the program-gated region of the DG FBFETs in the p-channel mode until the high potential barrier of the DG FBFETs in the n-channel mode is maintained. However, owing to the continued charge carrier injection, the potential barrier of the DG FBFETs in the n-channel mode decreases rapidly after 1 s, and the  $V_{OUT}$  decrease accelerates. For the holding logic '0' (Fig. 6b), the stored electrons leak out slowly from the DG FBFETs in the n-channel mode because of the high potential barrier the DG FBFETs in



**Figure 6.** Energy band diagrams of the DG FBFETs in the n- and p-channel modes while holding the output logic (a) ‘1’ and (b) ‘0’ states.

the p-channel mode is maintained. As the potential barrier of the DG FBFETs in the p-channel mode decreases rapidly after 1 s, the  $V_{\text{OUT}}$  increase accelerates.

We demonstrate that the proposed inverter can perform the logic operation and store the output. We also investigate the non-full swing characteristic that could be attributed to the ‘data-retaining’ behavior or the high latch-up/down voltage of the DG FBFETs. Moreover, by resetting the accumulated charge carriers, the inverter exhibits the  $V_{\text{DD}}$  or  $V_{\text{SS}}$  level at the output logic under gigahertz frequency. The equal voltage level between supply and logic signal facilitates the application of the inverter in a cascaded circuit. On the other hand, the reset operation with removing the supply voltages could be an issue when applying to an extended LIM system. Hence, further research is needed on the pulse schemes capable of resetting the accumulated charge carriers without removing the supply voltages to overcome the issue. Furthermore, the presence of the three distinct logic states of ‘1’, ‘0’, and ‘reset’ implies that the proposed inverter can be applied in ternary logic-in-memory systems<sup>17,18</sup>.

## Conclusion

In this study, we demonstrate the logic and memory functions of the inverter comprising the reconfigurable DG FBFETs. In the inverter based on the positive feedback mechanism, the output voltage loss arises from the residual charge carriers in the channel region during the logic operation. We apply the reset operation of removing the residual charge carriers with a program-gate, allowing the full pull-up and -down operations. As a result, the inverter exhibits the  $V_{\text{DD}}$  or  $V_{\text{SS}}$  level of the output logic state under a switching speed of nanoseconds order. Moreover, the output logic level of ‘1’ and ‘0’ is retained for ~ 21 s without the supply voltages. The results verify the possibility of application of the proposed inverter in LIM architecture.

## Data availability

All data generated during this study are included in this published article (and its Supplementary Information files).

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## Author contributions

J.J., S.W. and S.K. provided conceptualization and methodology; J.J. and K.C. verified and investigated; J.J. and S.K. analyzed the results and wrote the manuscript; S.K. supervised the research. All authors edited the manuscript and have given approval to the final version of the manuscript.

## Competing interests

The authors declare no competing interests.

## Additional information

**Supplementary Information** The online version contains supplementary material available at <https://doi.org/10.1038/s41598-022-16796-x>.

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