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Selectively biased tri-terminal vertically-integrated memristor configuration

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Memristors, when utilized as electronic components in circuits, can offer opportunities for the implementation of novel reconfigurable electronics. While they have been used in large arrays, studies in ensembles of devices are comparatively limited. Here we propose a vertically stacked memristor configuration with a shared middle electrode. We study the compound resistive states presented by the combined in-series devices and we alter them either by controlling each device separately, or by altering the full configuration, which depends on selective usage of the middle floating electrode. The shared middle electrode enables a rare look into the combined system, which is not normally available in vertically stacked devices. In the course of this study, it was found that separate switching of individual devices carries over its effects to the Complete device (albeit non-linearly), enabling increased resistive state range, which leads to a larger number of distinguishable states (above SNR variance limits) and hence enhanced device memory. Additionally, by applying a switching stimulus to the external electrodes it is possible to switch both devices simultaneously, making the entire configuration a voltage divider with individual memristive components. Through usage of this type of configuration and by taking advantage of the voltage division, it is possible to surge-protect fragile devices, while it was also found that simultaneous reset of stacked devices is possible, significantly reducing the required reset time in larger arrays.

Since their conception[1] and eventual fabrication[2] memristive devices have been extensively studied in an effort to incorporate them in circuit designs[3], in novel neuromoprhic computing setups[4], as artificial electronic synapses in an attempt to replicate synaptic functions normally only available to biological brain structures[5] and as electronic nociceptors for artificial skin applications[6]. Increased integration density, which resulted from incorporation in circuits, uncovered issues which impede nominal device operation, such as sneak path currents. A popular mitigation strategy has been the usage of new topologies, such as complementary resistive switching (CRS)[7], 1 selector 1 memristor (1S1M)[8], 1 diode 1 memristor (1D1M)[9] configurations. Other theoretical propositions include using a complementary memristor array composed by two anti-serially connected memristors[10]. At the same time, these technologies also protect from unwanted switching or destructive breakdown of fragile devices, by enforcing a (soft) compliance current through the multiple layers used to fabricate them.

On a separate front, efforts are being directed towards increased range in tuneability of devices[11], especially in settings of neuromorphic computing, where synaptic weight management is of vital importance. By using memristors as standalone components, analogue reconfigurable circuits[12] and threshold logic gates[3] can be fabricated, among other possible circuitry. One commonly referenced "device ensemble" is the memristive fuse[13,14], which elaborates on the expected behaviour of two memristors in series. Specifically, it has been previously pointed out[15] that memristive fuse is the natural extension of complementary switching when states in both devices exhibit analogue behaviour. In all of these "hardwired ensemble" cases it is not possible to gain insight into the workings of the separate layers of the ensemble, and fine tuning of states is a critical issue which has not yet been resolved.

Here, we propose a three-terminal device, 1M1M topology, which consists of two memristors fabricated vertically, with an interleaved, but accessible common middle electrode. The case for three terminal connected devices has already been theoretically made where this configuration is used to propose neuromorphic or conventional circuits[10,16]. This configuration allows probing of the whole stack, while the ability to tune both memristors separately allows fine tuning of the compound stack's resistive state. Other expectations from this type of configuration include increased tuneability, simultaneous switching of both devices and an inherent surge protection of devices due to the stack functioning as a voltage divider, improving resilience. With regards to fine tuneability, "super-resolution" memristive ensembles represent an idea that has been explored theoretically,

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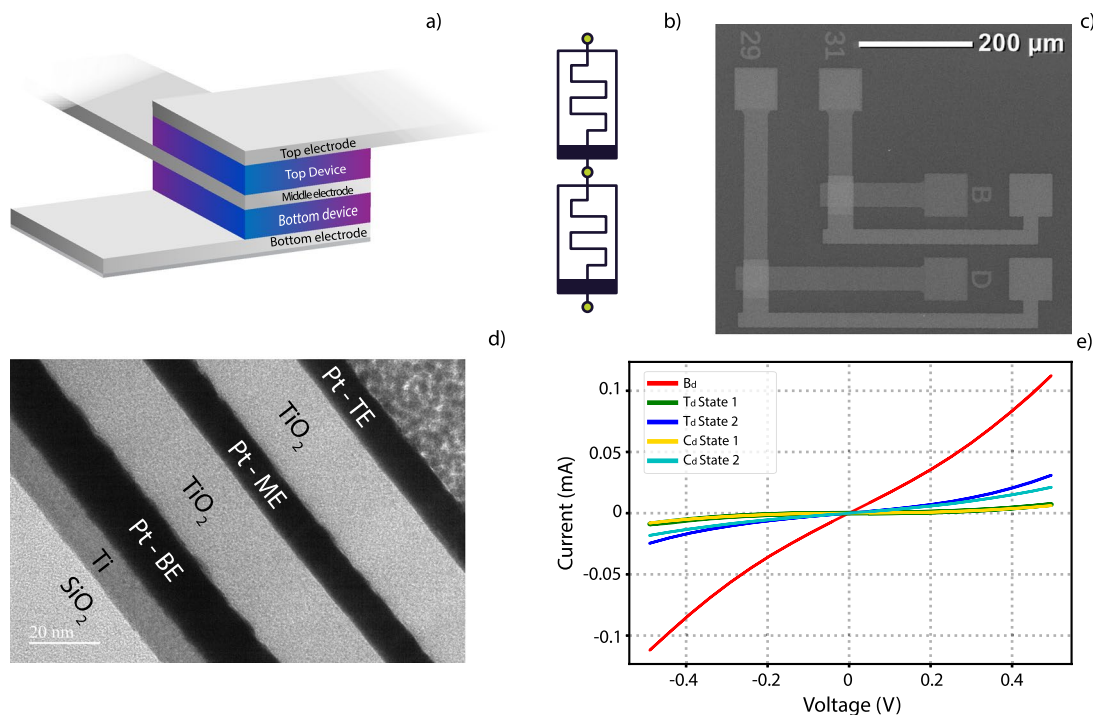
Figure 1. Physical and electrical characteristics of MIMIM devices. (**a**) Graphical depiction of device topology, while (**b**) electrical equivalent model ('serial' connection). (**c**) SEM image of the fabricated devices, illustrating the 3 electrodes and their overlap areas which constitute the devices. (**d**) TEM image of the overlap area, showing the vertical stacking of the fabricated devices. (**e**) non-switching IVs of a stack, whereby the IV of the Complete device is dependent on the IVs of the top (T_d) and Bottom devices (B_d), and the resulting voltage division between the two. In this case, two distinct states for the Top device (T_d State 1 and T_d State 2) were registered and the switching impact on the Complete device (Cd) has been recorded, as depicted in C_d State 1 and C_d State 2.

with cells consisting of two memristors connected in parallel[17], while here we are implementing it in a serial connection topology. This configuration allows both higher resolution and higher memory density per unit area. Both are achieved via manipulation of individual devices with different switching ranges, enabling the set-up of a coarsely-set resistive state originating from one device plus fine resistive tuning around that state by utilizing the second device. Notably, even for devices with similar resistive ranges and tuning tolerances, independent control of resistive states of two devices can achieve better control of the aggregate resistive state. Finally, the superposition of resistive states across both devices, broadens the overall tuning range of the aggregate state, providing further memory density (more available states). For simplicity we shall refer to these effects simply as "super-resolution" in the rest of the paper. Control of forming[18] and/or device manufacture can lead to both "serially" and "anti-serially" connected devices which can exhibit distinct computational behaviours. The difference being that in a "serial" stack, application of voltage of some chosen polarity will elicit the same response from both devices in the stack (both will either increase or decrease resistance).

Sample preparation

The type of devices selected to use as building blocks for this work were TiO_x based devices, which have been extensively studied during the last decade. TiO_x devices, fabricated and used in previous publications of our group, have had different aspects of their electrical behaviour assessed, such as, their conduction mechanisms at distinct resistive levels[19], the electrical characteristics of interfacial barriers at the metal-TiO_2 contact[20] and phenomena of interface asymmetry induced by symmetrical electrodes in these devices have also been studied[21]. Also, different capping layers have been tested to produce devices with better multibit capabilities[11], out of which we make use of the most advantageous configuration (TiO_x/Al_2O_3 active layer) in this current work. Final device structure can be summarized as a metal–insulator-metal–insulator-metal (M-I-M-I-M). The two fabricated prototypes were: Pt(BE)/TiO_x(AL1)/Pt(ME)/TiO_x(AL2)/Pt(TE) and Pt(BE)/[TiO_x/Al_2O_3](AL1)/Pt(ME)/TiO_x(AL2)/Pt(TE). Abbreviations in the parentheses denote the function of each layer within the device stack (Bottom, Middle, Top Electrodes and Active layers 1 & 2). A complete SEM image of all three electrodes, their access pads and the overlap area can be seen in Fig. 1c, while a visual representation of the cross-sectional area is available in Fig. 1a. Finally, Fig. 1b is a depiction of the electronic circuit which this configuration offers, with each of the three access points depicted as green circles. A TEM image of the cross-sectional area (Fig. 1d) depicts the internal composition of the devices ensuring film uniformity and quality.

Memristive devices are initially fabricated as M-I-M capacitors, and they transition into memristors after an electroforming step. This electorforming step is carried out independently for each memristive device in

the stack, by making use of the ME. Electroforming and measurements are carried out by using the ArC One platform , previously developed for memristor characterization[22]. This enables the use of highly controllable pulsing schemes for gentle and controllable electroforming, as well as controllable and gradual state switching, by utilizing pulse trains instead of IVs. All testing in this work is current-compliance free. The electroforming procedure comprises of 4 repeated steps to ensure successful device activation and has been covered extensively as part of a larger testing procedure in a previous publication[23]. Initially an IV sweep is carried out to ensure good connection to the device and to observe typical rectifying behaviour of unformed devices. Afterwards, the electroforming step takes place, in which a pulse train of steadily increasing voltage is sent to the device, until a sharp drop in resistance (to below a specified threshold) triggers the stop condition of the pulsing algorithm (Supplementary Figure S1). A new IV curve of the device is then obtained, which must be pinched, and resistive switching must be observed, for it to be considered as formed. Finally, a retention step is carried out to ensure non-volatile behaviour.

The forming procedure was applied *individually* for both top and Bottom devices. After forming, the possible measurement combinations available are Top device (Td), Bottom device (Bd) and the Complete device (Cd). Measurements of each configuration were carried out by positioning the probing needles on only two electrode pads at a time. Possible electrode combinations were the TE and ME (which correspond to the Top Device (T_d)), ME and BE (which correspond to the Bottom Device (B_d)) and TE and BE electrodes (which correspond to the Complete Device (C_d)). The third, unused, electrode was not engaged (floating terminal), to avoid any impact on measurement. Figure 1e displays non-switching IVs of Complete device and its two constituent devices. In this figure, 2 separate Top device states are included,(T_d State 1 and T_d State 2) which in turn impact the Complete device IV, leading to C_d State 1 and C_d State 2, respectively.

Here, two types of measurements were carried out which will be analysed in detail. The first type assesses switching impact on the Complete device due to only one individual device switching. To assess initial resistive state of all devices a resistive readout at 0.5 V was recorded from each individual device, by positioning the probes in all three of the previously mentioned electrode configurations, corresponding to the three device configurations (T_d, B_d, C_d). Switching is accomplished by using a pulsing process, which is a gentler approach to switching than IV switching and also enables more accurate state selection in multi-bit devices[11]. Pulse width was kept at 1 ms and inter-pulse time was set at 10 ms. Once a suitable switching voltage was found for each device, ranging from 1.5 to 3 V, a desired state would be set as a threshold and pulsing would be applied until that threshold was achieved or surpassed. This process was followed by a subsequent resistive read-out of all devices, by re-setting probes in all three configurations. This was repeated for all resistive states depicted in individual switching mode. For the second type of measurements, concerning the switching of the Complete device, pulsing was applied across the Top and Bottom electrodes, corresponding to the Complete device configuration, which could lead to switching in both layers or only one of them. After each switching event a resistive readout was obtained from all three devices. Due to the inherent non-linearity of memristive device IVs and to ensure consistency and comparability between measurements, whenever a resistive state value is quoted, this refers to static resistance under 0.5 V read-out voltage unless otherwise specified.

Characterization

Device characterization has been initially carried out by switching one of the two memristors and observing the effect on the Complete device and then switching the Complete device as a whole and observing the effect this had on the two devices it was composed of. As expected, full-stack resistance changes when either of the devices switches. This can be seen from the non-switching IVs recorded in Fig. 1e, where a state change in the top device led to a corresponding state change in the Complete device. However, the Complete device operates as a voltage divider and due to: a) the redistribution of voltage within the divider due to generally unequal switching between constituent devices and b) the inherent non-linearity in device IVs, the final resistance of the Complete device is dependent on, but not equal to, the sum of resistances of each individual device.

Switching in single layer. Individual switching was carried out independently on both of the devices comprising a Complete device, as shown in Fig. 2. Figure 2a,e indicates which part of the device is switching in each set of measurements. In each case the non-switching device was completely unaffected, as seen in Fig. 2b,f, confirming our ability to control devices independently. On the other hand, state switching of a device is transmitted to the complete device, as seen in Fig. 2c,g, when compared with Fig. 2d,h respectively. As a result of this behaviour we can achieve high tuneability range of resistive states by finely tuning each one of the two separate devices, which will result in a combined range and potentially increased density/resolution of controllably achievable states in the final stack, increasing state resolution.

A convenient way of exploiting this behaviour would be setting the aggregate stack state by using a device with large resistive state range and inter-state gaps for coarse tuning and a corresponding small range/gap device for fine tuning. To illustrate this, we utilize a multistate seeking protocol, which has been described at length in previous publications[11,24]. In brief, the protocol returns the number of statistically distinguishable resistive states that a target device can achieve. The protocol is applied separately to both the top and Bottom devices in the same stack, returning the states illustrated in Fig. 3a,b. The former depicts short retention runs for all stable states (62) that have been found in the Bottom device, spanning a 2-order-of-magnitude (500kΩ) resistive state window, while the latter shows stable states found in the Top device (45), spanning a narrower resistive range (10 kΩ). For this experiment we consider two adjacent resistive states to be distinguishable if they are separated by 1σ deviation.

The 3-D map in Fig. 3c illustrates all states that could be obtained in the complete device, resulting from the sum of states in the two separately tested devices, which can be achieved by separately controlling each individual
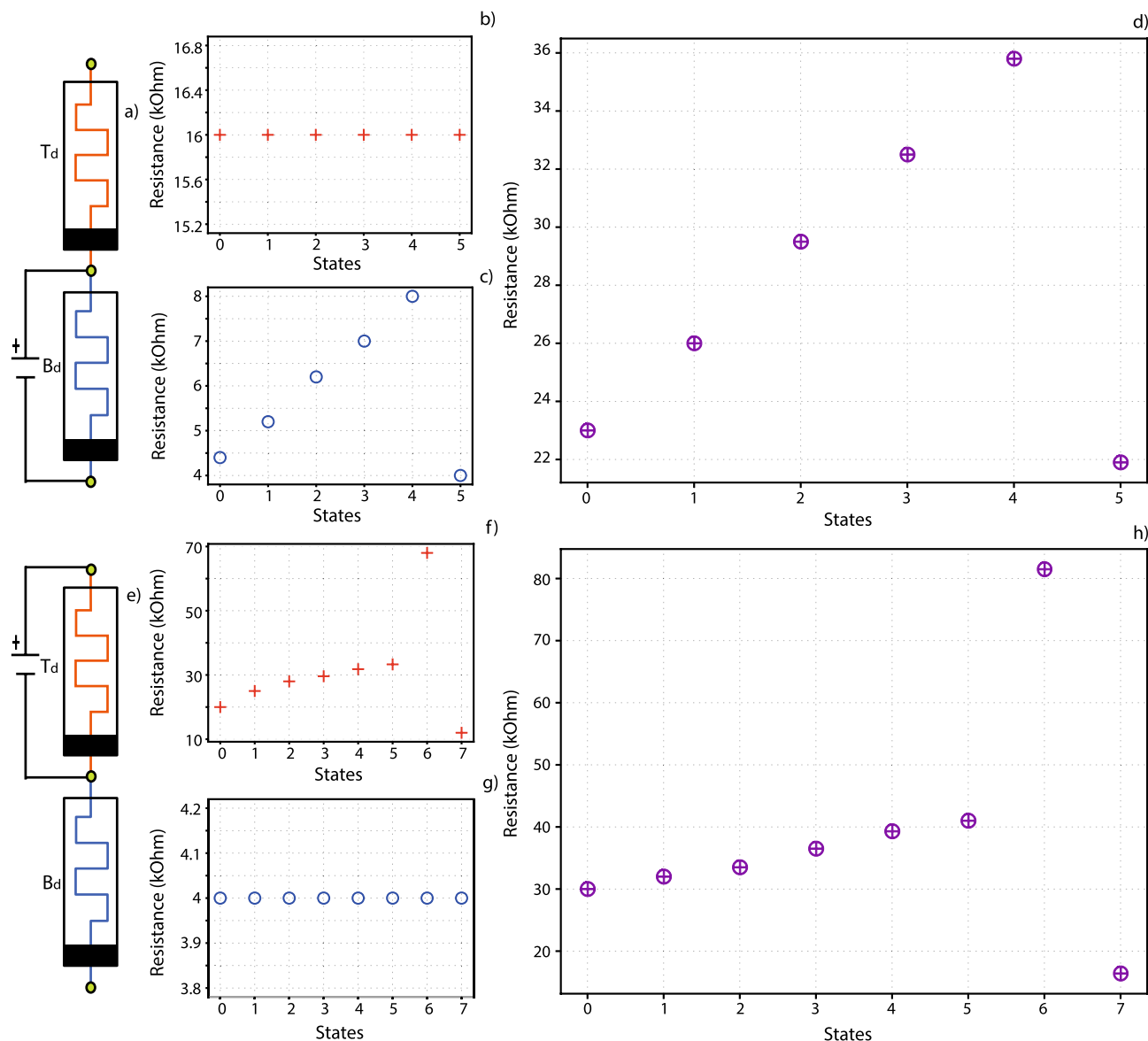
Figure 2. Complete device switching when the Bottom device is switched (**a**–**d**) and when the Top device (Td) is switched (**e**–**h**). Subfigures (**a**,**e**) depict the equivalent circuit during programming, where the switching and non-switching components can be distinguished. Subfigures (**b**,**c**,**f**,**g**) show the corresponding states of the devices in each step of the experiment, with (**b**,**c**) corresponding to the Top and Bottom devices of subfigure (**a**), while (**f**,**g**) correspond to the respective devices in subfigure (**e**). Evidence from (**b**,**g**) shows that the secondary device remains stable, while the switching device is being programmed in (**c**,**f**) respectively. Subfigures (**d**,**h**) result from measuring the resistive state of the Complete devices (**a**,**e**). In both cases it is evident that Complete device resistive states follow the curve set by the switching device, but the relation is not simply additive, due to the Complete device functioning as a voltage divider, thus slightly offsetting the effective voltage received by individual devices. (in both cases a change of $X\Omega$ in the switching device leads to a change $Y > X\Omega$ at the output).

device. Due to inherent non-linearity and voltage division of devices, the actual resistive values would, understandably, deviate from the calculated values, but the number of states would remain unaltered, as would the expected stack behaviour, due to selection of devices with different resistive ranges. This illustrates the point of a finely controlled super-resolution memristor. In this case, the individual devices have their states spread out in different patterns. The Bottom device has a large number of states spread out over a range of 500 kΩ, while the Top device has all its states within the boundaries of 10 kΩ. This in effect allows for the usage of the Top device as a fine-tuning mechanism, as can be seen in the rightmost 2-D projection of the 3-D map in Fig. 3c.

While many of the states presented here are duplicates, it is obvious that the combination of these two devices results in a state resolution which could not be achieved individually by any of the two devices.

Simultaneous switching. This section covers simultaneous switching of devices by using the top and bottom electrodes, TE and BE. This in effect enables the entire stack to work as a single device, but with the added

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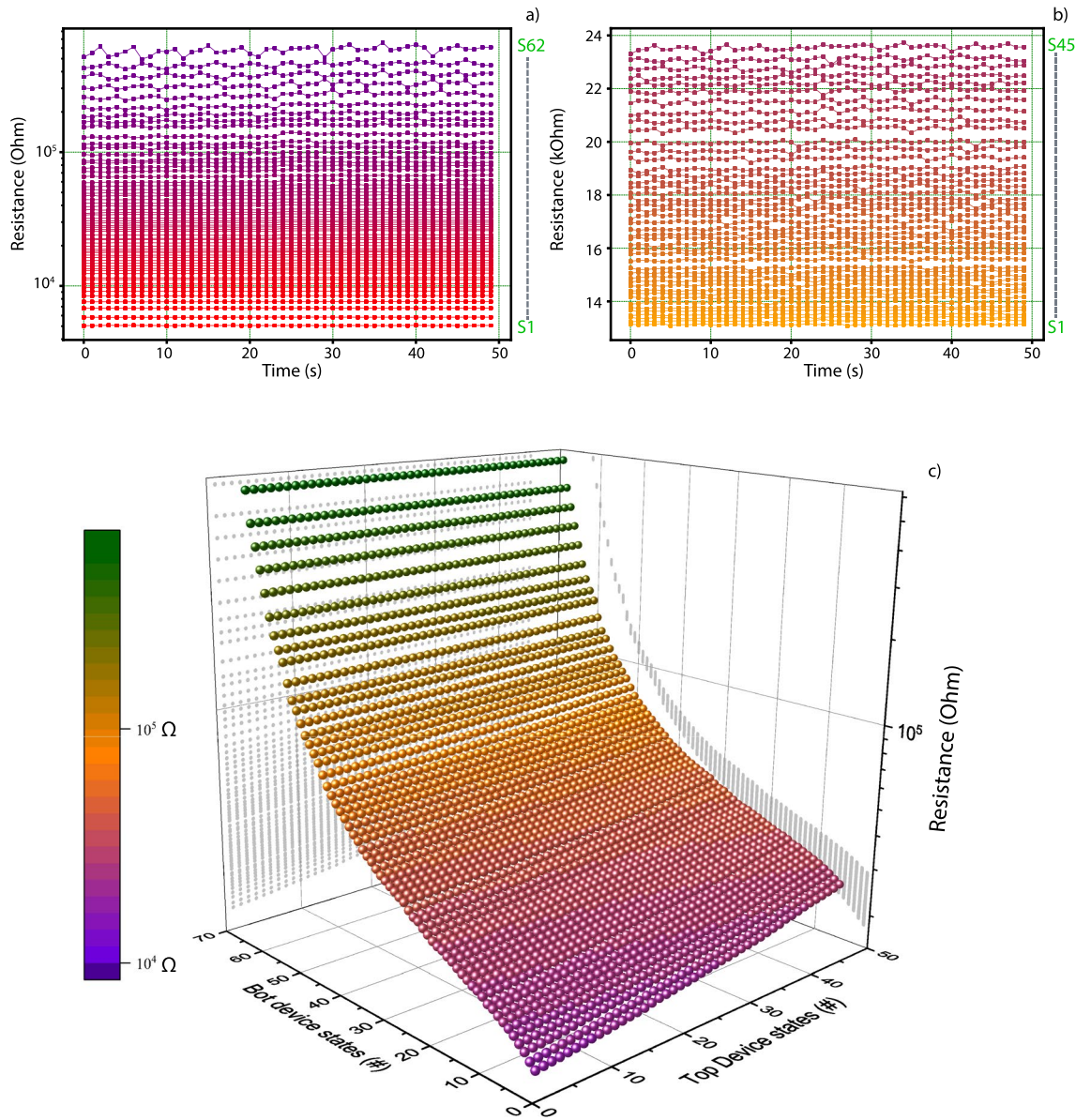
Figure 3. Improving memory density (number of memory states per device) and resolution per unit area of memristors by exploiting different resistive switching ranges in the top and Bottom devices. (**a,b**) Compiled retention measurements of distinct resistive states in the Bottom (**a**) and Top (**b**) devices in the same Complete device, with data obtained by using a measurement routine outlined in previous work[11]. The Bottom device has a range of states which spans from single-digit kΩ to hundreds of kΩ. The Top device ranges between approximately 10–30 kΩ. (**c**) All possible states that could be achieved by finely tuning each separate device, calculated by using the sum of possible states of constituent devices. Resistive values shown here will inevitably deviate a small amount from the actual values due to voltage division, but the core concept of increased memory density remains unaffected. Multiple states may overlap (i.e. multiple combinations of top and Bottom device resistive states lead to the same Complete device state), but total number of supported states will increase. This is indicative of the devices acting collaboratively in a coarse–fine tuning partnership; As seen in the projection on the right side of the 3D image, the Top device would act as a fine tuner for the coarser Bottom device states.

functionality of being able to probe the individual components to ascertain where the switching took place and how it affected them.

Two cases are studied in this section, the first is simultaneous switching of serially connected memristors, i.e. with the same switching polarity, while the second case is switching of antiserially connected memristors, i.e. alternate polarity.

Figure 4 depicts the first case, where both devices are switched in the same way. Subfigure (a) depicts a schematic of the stack and measurement setup, along with an EELS image of the type of device used, which indicates
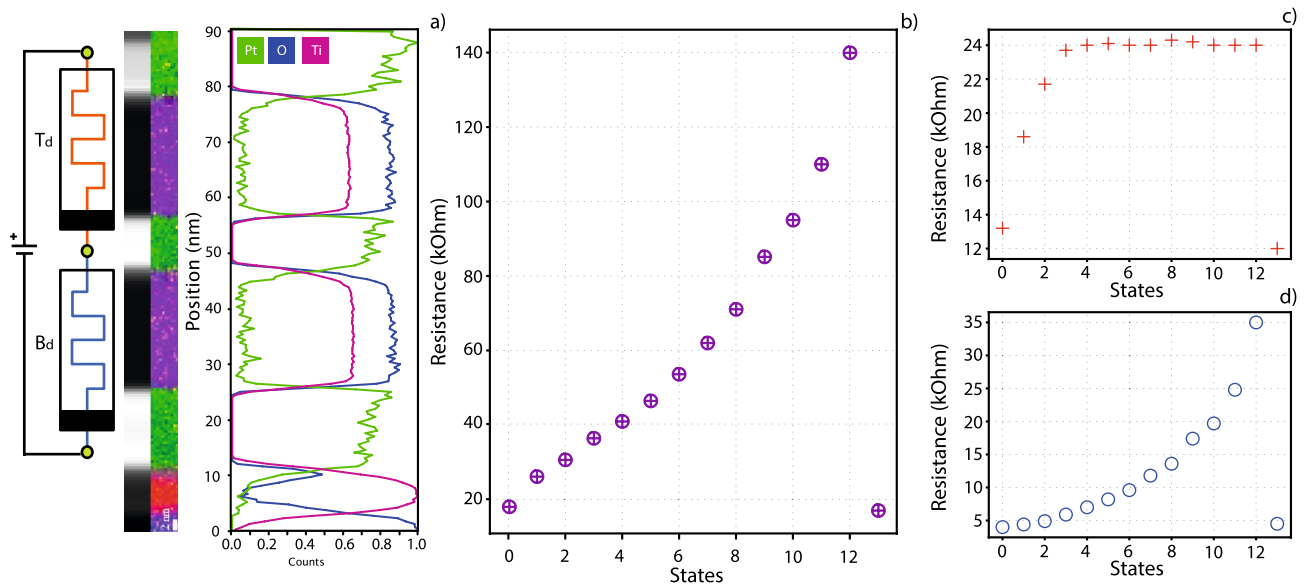
Figure 4. Simultaneous switching of memristors with the same switching polarity. Applied voltage is expected to have the same result on both devices, i.e., simultaneous resistive increase or decrease in both devices. (**a**) Schematic and an EELS image of the stack can be seen. (**b**) Complete device state evolution, where resistive change in states 1–4 is mainly driven by the Top device while resistive change in states 5–12 is driven mostly by the Bottom device. (**c,d**) State evolutions for both devices, common x-axis. After the 4th state change, the Top device saturates but the Bottom device keeps increasing its resistance.

the inner structure of the device from a materials point of view. Switching devices of comparable resistance simultaneously requires sufficient voltage reaching each device. This depends on the allocation of voltage in the potential divider that they form and the relation between the switching thresholds of the constituent devices as explained in[15]. The resistive readouts of the Complete device are depicted in Fig. 4b.

In the first 4 states, as seen in Fig. 4c,d, the Top device exhibits a bigger resistive switch, presumably due to receiving a substantial majority of the divider voltage as indicated by the difference in nominal resistances between Top device and Bottom device. After the "state 4" mark, the Top device reached a threshold where the voltage applied was no longer enough to switch it to a higher state. This in turn left the bottom device able to continue its gradual switching towards higher resistive values, which naturally also led to a higher voltage share being directed to it. This resulted in the exponential increase in resistive value for the Bottom device. Had the Top device not hit a threshold it can be inferred that the switching of the Bottom device would have been severely restricted.

Reading or switching devices by using the TE and BE of the stack has the added effect of doubling as a surge protection mechanism, as the voltage division means that devices will not receive more voltage than they can process, reducing the probability of device failure.

The last part of the test saw the simultaneous reset of both devices by only sending one pulse through the device. As devices are very sensitive to voltage, especially when applying reset pulses to them, this approach has multiple benefits. First, due to voltage division-induced negative feedback the reset pulse is less likely to exceed the absolute maximum device limits, mitigating the risk of failure. Second, reset time is effectively cut in half. Indeed even if these stacks where to be used just as two conjoined, but individually operating memory cells, the simultaneous reset could still prove extremely useful, due to halving memory reset time.

Multistate probing in this configuration does not allow full access to all possible constituent device resistive state configurations, such as when individually switching each component, with an example of this given in supplementary S2. This comes as a result of the voltage division which pushes devices to specific states. Thus, each time both devices are pushed, the intermediate states are lost, and in the event of a runaway exponential resistive switching, as depicted in fig (d), the second device becomes "state-locked", as it will continue to receive a progressively diminished share of the voltage input, effectively making switching impossible.

The second case studied, and depicted in Fig. 5, is for when devices are connected in an antiserial manner, which could result in contrary behaviour of the two devices for a voltage pulse of any specific polarity. Figure 5a presents the schematic for antiserially connected memristors, accompanied by an EELS image of this stack.

In this specific scenario the stack used was the second prototype, which was fabricated with a configuration of $Pt(BE)/[TiO_x/Al_2O_3]/Pt(ME)/TiO_x/Pt(TE)$, as is evident from the EELS image showing an Al peak in the upper Dielectric/Metal interface of the Bottom device. This stack was created to take advantage of increased multistate capabilities offered by the Bottom device, and to ascertain if mixing different types of memristors is possible. There were no indications that stacking devices with different active layers might have adverse effects on the switching behaviour of the entire stack. The same fundamental principles governing voltage division and switching conditions hold.
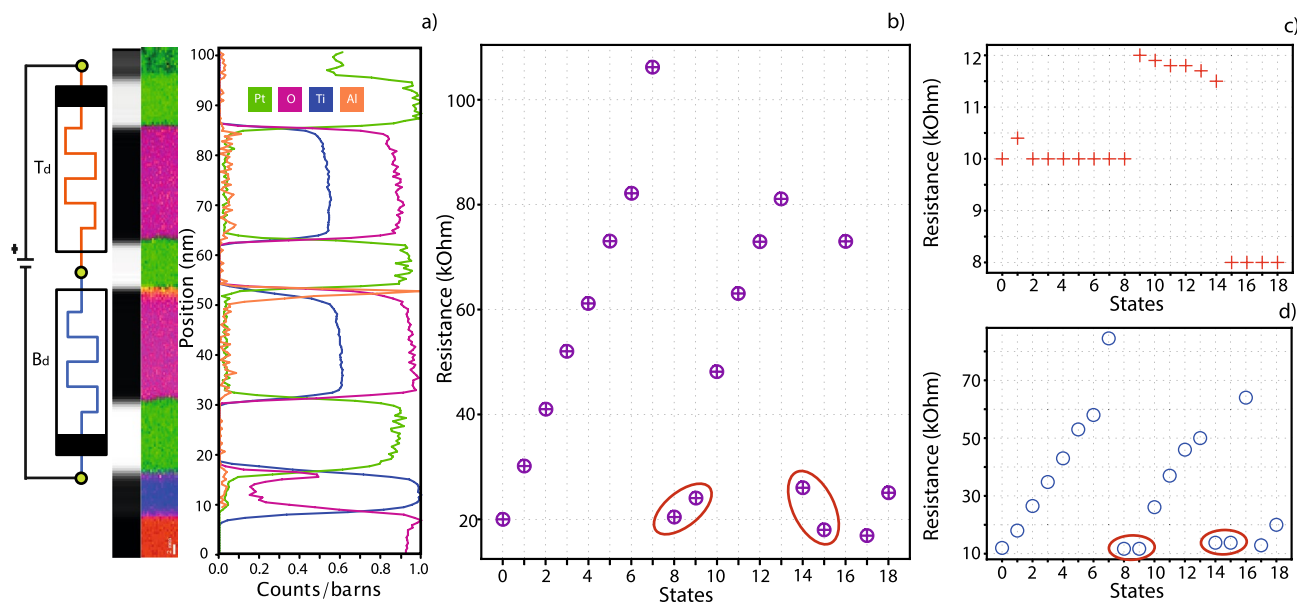
Figure 5. Simultaneous switching of antiserially connected memristors. In this case the voltage applied should have opposite effects on the devices, i.e. it could increase resistance in one and decrease it in the other. (**a**) Antiserial connection schematic and EELS image of the stack. In this case the Bottom device used was a bilayer stack to ensure cross-fabricational device functionality. Electroforming was used to force T_d to exhibit opposite polarity of switching from B_d. (**b**) State evolution of the Complete device through application of voltage pulses across the aggregate stack. Exceptions to this rule are states 9 and 15, shown inside the red ellipse, where individual switching was used for the Top device, and was carried on to the Complete device, in a process already described in Fig. 2. (**c,d**) State evolutions of antiserially connected devices. Evidently from (**c**), the device state is not affected as much when using lower voltages ($+2$ or -2 V), which is what was supplied to the whole stack, leading to the conclusion that higher stimulus would be needed to switch it. For the Top device to switch, a pulse of increased voltage ($+3$ or -3 Volts) had to be separately supplied to it. This led to switching behavior seen in states 9 and 15. During states 9 to 14, whole-stack pulsing is more successful in affecting the whole stack (switching voltage $+2$ V) and there was a gradual decrease of T_d resistance at the same time as it was increased for B_d. The Complete device evolution reflects all changes that happen to both devices. For example, transitions into states 9 and 15 are wholly dependent on T_d switching, while states 1–8 and 10–14 closely follow the evolution of B_d. States 8,9 and 14,15 are encircled in subfigure (**d**) to, highlight non-switching behaviour of the B_d, as voltage was only applied in T_d.

To test this case, a stack was generated, where, after electroforming both devices, one of them would increase its resistance for a specific voltage polarity, while the other would decrease it for that same polarity. The electroforming mechanism responsible for deciding the Set/Reset polarity is outside the scope of this work, nonetheless, it has been found that forming polarity is responsible up to a certain level for switching polarity as confirmed in Supplementary figure S3.

Another important detail is that, for this experiment, the resistive values of the devices are more important than in the previous case. Devices that have similar resistivities might exhibit resistive state changes of the same magnitude, leading to apparent Complete device inactivity, while underneath, both devices are affected. On the other hand, a significant difference in resistance, or switching voltage, will lead to resistive switching in only one of two devices. Here we present the second case, while the "similar resistances and voltage requirements" scenario is presented in supplementary figure S4.

Figure 5b presents the result of simultaneous switching in antiserially connected devices. For the initial 8 states recorded, the Bottom device followed a gradual increase in resistance while the Top device had no reaction to the voltage applied. It is believed that the inertness of the Top device is either due to insufficient switching stimulus, a situation exacerbated with the increase in resistive state of the Bottom device, or due to it already occupying its current lowest state. Following this initial resistivity increase, the Complete device was reset, by using a pulse of the opposite polarity. Then, the Top device was manually switched to a higher resistive state by applying a bespoke pulse train, with opposite polarity from the one used to switch the stack. This led to a resistive switch event, seen in the transition to state 9 of subfigure (c), which also translates to a small state change in subfigure (b). Subsequently, consecutive pulse trains were once again applied to the Complete device, which led to a gradual increase of the Bottom device, but with a concurrent gradual decrease of resistance in the Top device. The resistive change in the Top device is not extensive and we believe that the stimulus that now reaches it, due to its higher resistive value, is still not high enough to incite a strong response. Nonetheless, T_d behaviour is counter to B_d. This in effect supports the notion that antiserially connected devices have opposing behaviours, with the whole stack seemingly behaving as theorized by the memristive fuse effect, although it seems more efficient to individually switch the individual devices, considering the apparently fine balance required for meeting

the switching conditions of both devices at all times. Next, B_d is once again reset in state 14 (Fig. 5d), by applying a reset pulse to the Complete device, and, afterwards, the Top device is also set to a lower resistive state, once again, manually. Finally, another set/reset/set cycle is carried out on the entire stack. The Bottom device responds to the stimulus applied, while the Top device is once again unresponsive.

Conclusion

A double stack (M-I-M-I-M) memristive configuration was fabricated which combines two devices and the ability to individually switch them by using a middle electrode (ME), or the ability to simultaneously switch them by applying voltage pulses to the top (TE) and bottom (BE) electrodes of the device. Each individual device can be separately tuned, with resulting resistive changes carried over to the complete device. Complete device resistance is dependent on the nonlinearity of individual device IVs and thus is generally not equal to the sum of constituent device resistances, but rather the sum of their static resistances at the voltage shares they receive from the divider. Individually switching the devices and then registering the resistive state of the Complete device can lead to increased resistive state resolution and consequently device memory density, even though the intrinsic state resolution of certain device technologies may exceed measurement resolution. Completed device switching can either switch both devices at the same time if they have similar resistivities, or only the most resistive one. Constituent device resistive state will influence the voltage balance in the voltage divider, thus deciding the amount of stimulus they will receive.

In the case of serially connected devices of similar resistive range, switching will take place in both devices as long as the stimulus they receive is enough to change their state. For antiserially connected devices, evidence points towards a "memristive fuse" type of behaviour whereby due to opposing changes in resistive states across the devices, the allocation of voltage in the divider can swing much more widely than for serial devices -in principle-. In the case of similar resistive states (and switching threshold voltages) in antiserially connected devices, the Complete device may function as an attractor with unchanged resistive state, while the individual devices are impacted by the voltage stimulus applied. In either case, the existence of a second memristor in serial connection may, under the right conditions, function as a surge protection mechanism, in the same way as using a resistance in series, protecting each other from catastrophic failure. Finally, in the case of devices with the same polarity, simultaneous reset has been observed, which is a powerful tool to cut reset times in memristor arrays by half.

In conclusion, we have demonstrated in silico a 3-terminal component consisting of 2 serially connected, vertically stacked, memristors, which can be used both as a "fuse" and as individual devices. We have shown that: a) the cointegration of the two devices and b) the fact that they share an electrode does not cause any significant deviation from the theoretical behaviours that are expected when examining independent devices, either in isolation or in serial/antiserial configuration as was done in previous work. Furthermore, we show that it is possible to obtain full-stack switching in these co-integrated devices; the co-integration process does not skew the required switching conditions sufficiently to introduce catastrophic complications. We hope that this work will help the community develop such 3-terminal devices as basic components for applications that can use either their individual or their fuse-configuration properties in the future.

Methods

Device fabrication. Device composition consists of two vertically aligned memristors which share one electrode (Middle Electrode—ME) of the stack. To achieve this, five distinct deposition steps were required, one for each layer of the Complete device. Patterning of all steps was carried out by negative tone photolithography. A post-lithography surface clean was conducted by using O_2 plasma, through Reactive Ion Etching. Devices were deposited on top of a 200 nm Silicon dioxide (SiO_2) insulating layer, which was thermally grown on top of 6-inch silicon wafer substrates.

In steps 1–3-5 platinum electrodes were deposited by electron beam evaporation, with all electrodes having an average thickness of 12 nm. For step 1 an adhesion layer consisting of a thin Titanium film (10 nm) was deposited before the deposition of bottom electrodes. Following each metal deposition step a lift-off process was followed by submerging the substrates in N-Methyl-2-pyrrolidone (NMP). Thus, the three distinct electrodes were formed, Bottom Electrode (BE), Middle Electrode (ME) and Top Electrode (TE).

During steps 2 and 4 the active layers for Top and Bottom devices were deposited, for which magnetron sputtering was used. Two different material configurations were explored in this work. In case one, steps 2 and 4 had an active layer (AL) consisting of TiO_x, while in the second case an additional Al_2O_3 was grown on top of the TiO_x in step 2 only. This enabled a first look into combinations of different types of memristive devices. In this case the TiO_x/Al_2O_3 active layer device was selected as it had proven to possess good device characteristics in a previous study[11]. Deposition power used for the TiO_x layer was 2 kW and for the Al_2O_3 layer, 100 W. Flow rates were 8 sccm for O_2 and 35 sccm for Ar gas. A lift-off step was carried out after sputtering.

Data availability

All data used in plotting the figures are available at https://doi.org/10.5258/SOTON/D2257.

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Author contributions

V.M., S.S and T.P conceived the experiments. V.M. and S.S designed the devices and fabricated them. V.M. did the electrical measurements. V.M, S.S and A.S did the data analysis. V.M. wrote the main manuscript text. All authors reviewed the manuscript.

Competing interests

The authors declare no competing interests.

Additional information

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