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# Common ground type five level inverter with voltage boosting for PV applications

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The boost-switched capacitor inverter topology with reduced leakage current is highly suitable for distributed photovoltaic power generation with a transformerless structure. This paper presents a single-stage 5-level (5L) transformerless inverter with common ground (CG) topology for single-phase grid-connected photovoltaic application. A generalized version of the proposed topology is also presented. The proposed topologies are derived by combining the dc/dc boost converter and switched capacitor cell. The primary focus has been given to the 5L version of the proposed topology. The number of switch counts is reduced, the maximum voltage gain is four times, and the inrush current is suppressed due to the input inductor configuration. Also, the voltages across the switched capacitors (SCs) are self-balanced. The negative source terminal and the load are connected directly to suppress the leakage current. It is thoroughly compared with other recent CG-Type topologies to attest to the advantages of the proposed topology. The laboratory prototype is developed for 600 W with the maximum efficiency is 94.21%, and the maximum source current is not more than 25A. Further, the operation of the proposed topology is verified under dynamic loading conditions, and the results are presented.

Multilevel inverters are well-matured power converters, and they are widely used in various applications, including renewable energy sources, AC drive, HVDC, etc.,[1,2]. However, the number of dc sources and voltage boosting is another big challenge in conventional MLIs. To increase the output voltage, several single dc sources switched capacitor multilevel inverter (SCMLI) topologies were reported[3,4]. In this SCMLI, topologies are suitable for PV applications, but the leakage current is another challenge in SCMLI topologies. The transformer-less inverter is a quite attractive power converter for PV applications because it doesn't require a low-frequency, bulky and costly transformer (as the name suggests) for grid interface. The absence of a transformer leads to leakage current due to the non-existence of galvanic isolation. Here, the leakage current reduction can be achieved by adding additional power components to the inverter[5,6]. Several approaches like ac decoupling, dc decoupling, H-Bridge zero voltage rectifier (HB-ZVR), and midpoint clamped methods are available[7] for addressing the leakage current issue. Although these approaches successfully suppress the leakage current to some extent, they fail to eliminate it. This issue is effectively addressed by the common ground (CG) type topologies introduced in[8] by directly connecting the negative terminal of PV and the grid's neutral terminal, leading to zero leakage current. The CG type inverters often use a virtual dc source which can be either a floating capacitor (FC) or a switched capacitor (SC)[6]. In[9,10], the topology uses a floating capacitor which requires high capacitance values to maintain the voltage across the FC[11]. In order to avoid the high capacitance value, a self-balancing topology is proposed in[12]. However, this topology uses one SC and multiple dc-link capacitors. The SC voltage is equal to the sum of all the dc-link capacitors, which increases the SC's voltage rating.

Further, the direct charging of SC with a voltage source will introduce a high capacitor charging current which requires devices of a higher current rating. To overcome the above issue, a soft charging method is proposed in a few SC topologies by inserting an inductor in the charging path[12–15]. However, the current is not suppressed dramatically due to the soft charging inductor's low inductance value (in μH). To further suppress the charging current, the inductance should be increased to mH range, but this is not suitable because the high inductor value will disturb the nature of inverter operation. Hence, the topology should be designed so that the use of an inductor with high inductance should create any disturbance in the topology. In[16–18], the inductor is used in the circuit, and its dual playing role is to (i) act as soft charging and (b) energy storage. However, the voltage of the topology presented in[16–18] is four times that of the $v_{in}$, and it has more number of switches, and the voltage stress on the switches is twice the output voltage. Further, a five-level inverter topology is proposed in[16] to reduce the

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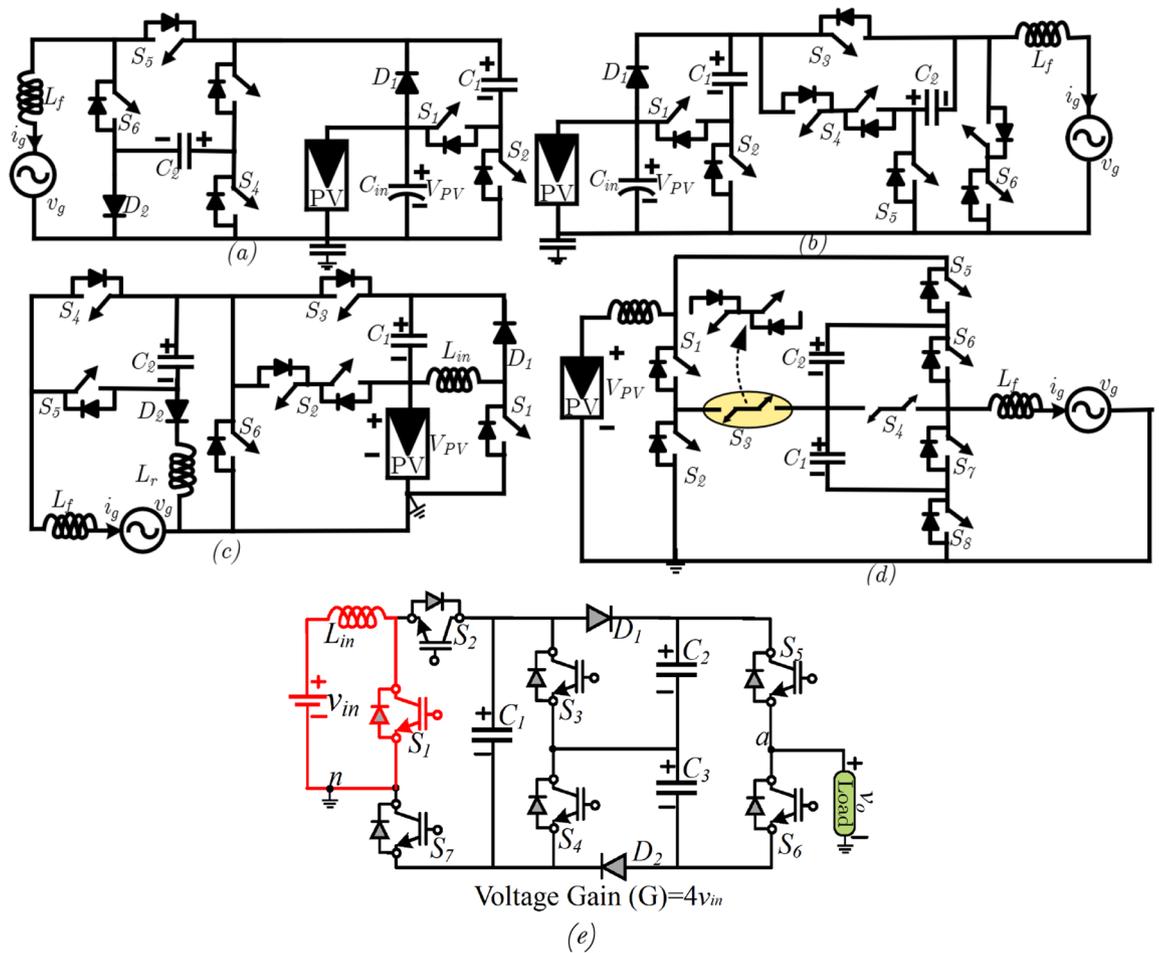
**Figure 1.** Various common ground 5L inverter circuit diagram (**a**) presented in[14], (**b**) presented in[15], (**c**) presented in[17], (**d**) presented in[18] and (**e**) proposed 5L-QBT topology.

voltage stress. In this topology, the number of device counts is high, and the voltage gain is four times that of the $v_{in}$, but the switch count is not reduced. It is important to mention that both the proposed topology and the one in[16] fall under a common ground type inverter category. However, the proposed topology in this work has a lower number of switching devices compared to the topology in[16]. While the proposed topology has SEVEN switching devices, the topology in[16] has TEN switching devices. Consequently, the proposed topology has a lower number of ON State switches, gate driver circuits, and other supporting components like heat sinks. This paper proposes a five-level CG type transformerless inverter topology with reduced switch count and high voltage boosting capability. The output voltage ($v_o$) is four times (Quadratic Boost Inverter—QBI) the input voltage ($v_{in}$). The other merits of this topology are given below:

    i.   The required number of IGBT is less than[14–18].
    ii.   Suppression of inrush and leakage current.
    iii.   Suitable to operate in high reactive power load.
    iv.   The maximum voltage stress on the switch is equal to the $v_o$ compared to[18].
    v.   The maximum voltage stress across the SC is $2v_{in}$.

**Proposed 5L-QBI topology.** *Description of proposed topology.* The circuit diagram of the proposed single-stage topology is shown in Fig. 1. The proposed topology uses seven switches, two diodes, and three capacitors. Each capacitor is charged to 2vin, and the switch S1 is operated in a 50% duty cycle.

*Modes of operations.* The proposed 5L-QBI inverter topology simultaneously performs both boosting and inverting operations. For better understanding, Fig. 1 is considered for describing the modes of operation. In each mode, the inductor charging and discharging are explained with corresponding circuit diagrams as depicted in Fig. 2a–e. Moreover, the duty cycle of the embedded boost converter is fixed to 50%, and the corresponding switching sequence is given in Table 1. The capacitors' charging currents are defined as $i_{c1}$, $i_{c2}$, $i_{c3}$, and the load current io.
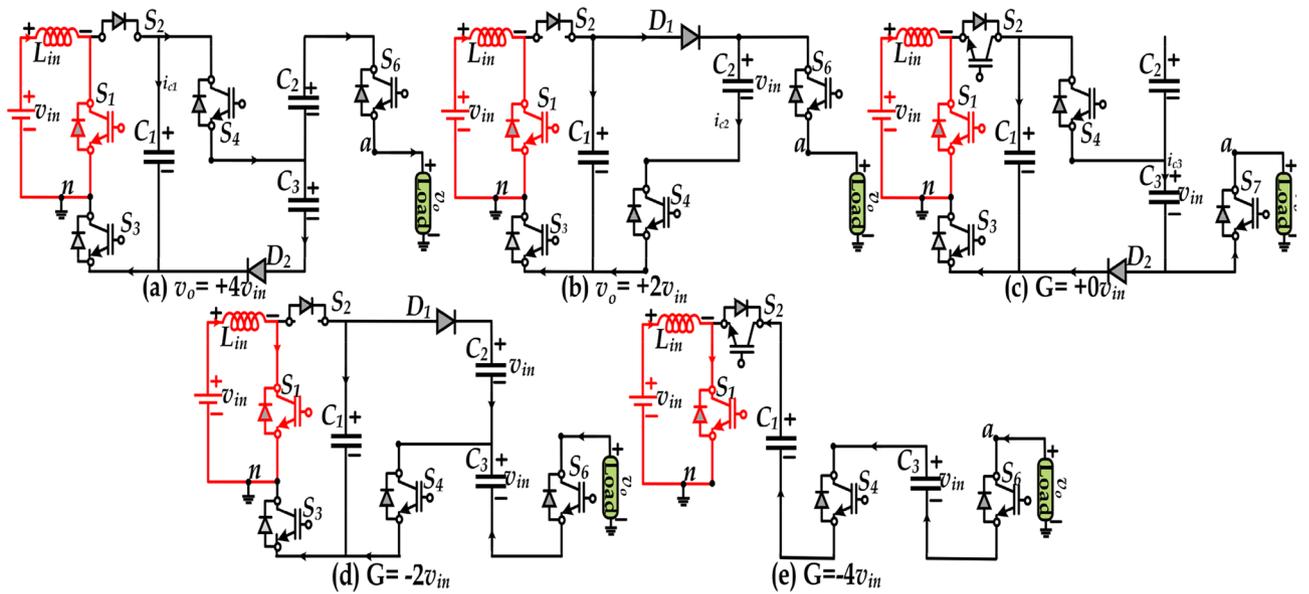
**Figure 2.** Modes of operation (**a**) $L_{+2}$ ($+4\,v_{in}$), (**b**) $L_{+1}$ ($+2\,v_{in}$), (**c**) $L_0$ ($+0\,v_{in}$), (**d**) $L_{-1}$ ($-2\,v_{in}$), and (**e**) $L_{-2}$ ($-4\,v_{in}$).

| Level | ON state switches | | $v_o$ | $L_{in}$ | $C_1$ | $C_2$ | $C_3$ |
|---|---|---|---|---|---|---|---|
| | $S_2$-$S_7$ | $S_1$ | | | | | |
| $L_{+2}$ | 011010 | $P_{ON}$ | $+4v_{in}$ | Charging | $\downarrow$ | $\downarrow$ | $\uparrow$ |
| | | $P_{OFF}$ | | Discharging | | | |
| $L_{+1}$ | 010110 | $P_{ON}$ | $+2v_{in}$ | Charging | $\uparrow$ | $\uparrow$ | - |
| | | $P_{OFF}$ | | Discharging | | | |
| $L_{+0}$ | 011001 | $P_{ON}$ | $0\,v_{in}$ | Charging | - | $\uparrow$ or - | -or $\uparrow$ |
| | | $P_{OFF}$ | | Discharging | | | |
| $L_{-1}$ | 010101 | $P_{ON}$ | $-2v_{in}$ | Charging | $\uparrow$ | - | $\uparrow$ |
| | | $P_{OFF}$ | | Discharging | | | |
| $L_{-2}$ | 100101 | 1 | $-4v_{in}$ | Charging | $\downarrow$ | $\uparrow$ | $\downarrow$ |

**Table. 1.** Switching sequence of 5L-QBI topology. *D-Diode, P-Pulse, $\uparrow$-Charging $\downarrow$-discharging, $P_{ON/OFF}$-Pulse ON /OFF.

*Top positive voltage level ($+4\,v_{in}$).* In this mode, $v_o$ is the sum of the voltage across the inductor and the capacitor $C_1$ i.e., $v_o = v_L + v_{c1}$ and the $v_L = \left[1/(1-d)\right]v_{in}$, where the $d$ is kept at a 50% constant value. Here, the $C_1$ is discharging, and $C_2$ is charging to $2\,v_{in}$. The switches $S_3$ and $S_6$ are turned ON, and the anti-parallel diode of $S_2$ and diodes $D_2$ and $D_a$ are conducting. When the dc source is connected parallel to the SCs, the SCs draw a considerable current during starting, often called the inrush current. The inrush current magnitude is too high, and it can be suppressed by adding more resistance or inserting the inductor in the charging path. It can be observed that the proposed 5L-QBI topology uses an inductor and it serves two purposes which are as follows: -(i) boosting the input voltage and (ii) limit/suppressing the inrush current. Note that the proposed topology belongs to the boosting inverters family with 4 gain i.e., the input current on the input side is 4-times higher than the output current. Due to the inductor on the input side, the inrush current in the proposed topology is reduced by 5-times as compared to the non-inductor topology. Further, similar inductor-based SC-MLI topologies are already addressed[16–18].

*Switch Stress:* The maximum voltage (MVS) and current stress (MCS) for each level are $2\,v_{in}$ and $i_{c2}+i_o$, respectively.

*First positive voltage level ($+2\,v_{in}$).* The value of $v_o$ is two times of $v_{in}$ due to the storage element inductor is acting as a voltage booster. The capacitor $C_1$ gets charged to this level, but $C_2$ is neither connected with the source nor load. The switch $S_4$ is turned ON to charge the upper capacitor $C_1$ and the switches in ON state are $S_4$, $S_5$, and $S_6$. *Switch Stress:* The MVS and MCS are $v_{in}$ and $i_{c1} + i_o$.
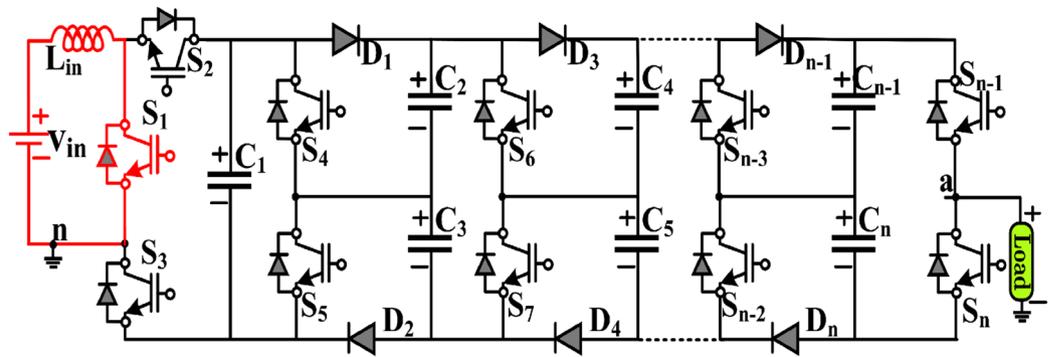
**Figure 3.** Proposed extended structure.

*Zero voltage level (+ 0 $v_{in}$).* The freewheeling path for the load is provided in this mode. The load voltage equals zero, but the capacitor $C_2$ is charged via $S_3$, $S_7$, and D. The switch $S_1$ continues to act as a boost converter switch at a fixed 50% of the duty cycle. The voltage across $C_2$ is equal to $2v_{in}$. *Switch Stress:* The MVS and MCS are respectively $2v_{in}$ and $i_{c1} + i_o$.

*First negative voltage level (-2 $v_{in}$).* The SC $C_2$ discharges to the load via $D_a$, $S_4$ & $S_7$, and the upper SC $C_1$ is charged to $2v_{in}$ simultaneously. The switch $S_1$, which is turned ON and OFF at high frequency, forms the boost converter and the inductor $L_{in}$ and capacitor $C_1$. *Switch Stress:* The MVS and MCS are respectively $v_{in}$ and $i_o$.

*Top negative voltage level (-2 $v_{in}$).* In this mode, the switch $S_1$ is turned ON to provide the path for the 5th voltage level, as shown in Fig. 2e. Here, the **switch** $S_1$ will not operate as a boost converter switch, and the pulses change over to the inverter pulses.

Now, the load voltage is equal to sum of the $C_2$ & FC i.e. $v_o = -3v_{in}/2$. The Diode *Dx* provides the current path during the lagging or leading power factor. The above discussion clearly shows that the proposed topology uses fewer ON state switches in each voltage level. The stress analysis on the switches is the important parameter for capacitor self-balanced inverter topologies. The high inrush current will occur during the parallel connection of FC and $v_{in}$. The current small inductor can be added to the circuit loop to prevent the inrush. It confirms that the proposed topology's maximum voltage stress equals $2v_{in}$ and current stress is $i_o + i_c$ occurred in only two switches. Other topologies presented in[8–11] needed four switches with high current stress.

*Extended structure.* Figure 3 shows the extended structure of the proposed topology. The boosting module is connected parallel to the dc source, and it can be extended to the "*n*" number of modules. Each module consists of two capacitors, two diodes, and two switches. Further, all the capacitors are charged to $v_{in}/(1 - d)$, i.e. $2v_{in}$ where $d = 0.5$ constant.

The number of output voltage level ($N_{Level}$), switches ($N_{Switch}$), diode ($N_{Diode}$) and capacitors ($N_{Capacitors}$) for "*n*" number of modules is given in (1)-(4).

$$N_{Level} = 2n + 3 \tag{1}$$

$$N_{Switch} = 2n + 5 \tag{2}$$

$$N_{Diode} = 2n \tag{3}$$

$$N_{Capacitors} = 2n + 1 \tag{4}$$

$$Output\ Voltage\ Gain\ (v_G) = 2(n + 1)v_{in} \tag{5}$$

The voltage gain of the extended topology increases with the increase in the number of modules as given in (5).

**Modulation technique and passive component design guidelines.** *Proposed PWM Scheme.* The proposed PWM technique is depicted in Fig. 4. The level-shifted triangular carrier signal ($A_1$-$A_4$) is used in the conventional sinusoidal PWM technique. The switching sequence for each voltage level is stored as given in Table 1. The parameter "L" is the sum of all the comparators' output. L is given as the input to the lookup table. Except level -2, the switch $S_1$ is operated by an independent pulse (ON/OFF) train with a switching frequency of $f_{s1}$, as depicted in Fig. 4. When $L$ is equal to the -2, $S_1$ will be turned ON as Table 1. The front side of both inverters looks the same. However, the proposed topology has distinct features in which the pulse generation and switching schemes are not the same. Moreover, the proposed topology is extendable to $N_{Level}$, whereas presented in[19] is

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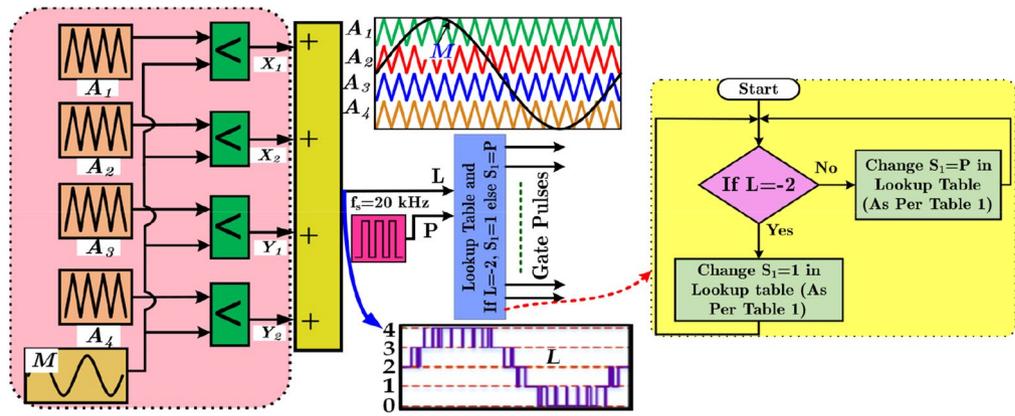
**Figure 4.** Proposed PWM scheme.
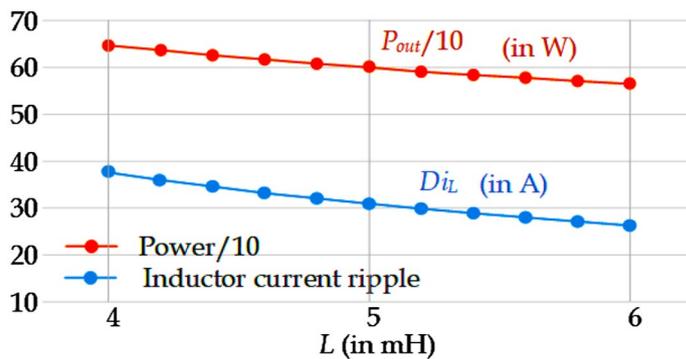


**Figure 5.** The inductor current ripple and output power vs the value of inductance for $L_{in}$.

limited to nine-level. In[19], a constant is compared with the carrier to generate pulses that are used to control the switches ($S_1$ and $S_2$). However, the magnitude of this constant is not clear and makes it doubtable to be used for the MPPT, whereas the proposed topology is driven by an independent pulse generation scheme that makes it an optimal option to achieve the MPPT. The logic sequence for switches is given in (10).

$$
\left.
\begin{aligned}
i_L &= \frac{1}{L} \int \{(1 - S_1)[v_{C3}(L_{+2} + L_{+0}) + v_{C2}(L_{+1} + L_{-1})] + S_1 v_{in}\}dt \\
v_{C1} &= \frac{1}{C_1} \int \{(L_{+2} + L_{+0})[(1 - S_1)i_L - (v_{C1} - v_{C3})/r] + (L_{+1} + L_{-1})[(1 - S_1)i_L - (v_{C1} - v_{C2})/r] + L_{-2}i_{Load}\}dt \\
v_{C2} &= \frac{1}{C_2} \int \{(L_{+2} + L_{+0})[-i_{Load}] + (L_{+1} + L_{-1})[(v_{C1} - v_{C2})/r - i_{Load}]\}dt \\
v_{C3} &= \frac{1}{C_3} \int \{(L_{+1} + L_{-1})[-i_{Load}] + (L_{+2} + L_{+0})[(v_{C1} - v_{C3})/r - i_{Load}]\}dt
\end{aligned}
\right\}
$$

(6-9)

$$
\left.
\begin{aligned}
S_1 &= P \text{ for } L \neq -2 \\
&= 1\, L = -2
\end{aligned}
\right\}
$$
$$
S_2 = Y_2, \; S_3 = X_2 + Zero, \; S_4 = X_1\overline{X_2} + Y_1\overline{Y_2},
$$

(10)

$$
S_5 = Y_2, \; S_6 = X_1, \; S_7 = Y_1
$$

*Design of L and C components.* The proposed topology switching function analysis is used to design the capacitor and the inductor. The following switching functions $L_k$ (where $k \in \{2,1, 0, -1, -2\}$) and $S_1$ are defined. The switching function $L_k$ assumes the value '1' if the generated voltage level is '$k$'. However, if the above condition is not satisfied, $L_k$ is equal to '0'. The other switching function $S_1 = 1$, when switch $S_1$ is turned on, otherwise $S_1 = 0$. The following equations may be derived for the current of inductor $L_{in}$ ($i_L$) and the voltages of capacitors $C_1$, $C_2$, $C_3$ (respectively $v_{C1}$, $v_{C2}$, and $v_{C3}$). The (6)-(9) $i_{Load}$ is the load current, and $r$ is the charging path resistance. By solving these equations using numerical methods for an R-L type of load with R = 50 Λ, L = 1mH, r = 100 mΛ, and $v_{in}$ = 50 V at 0.95 modulation index ($m_a$ = 0.95), a few graphs are obtained as given in Figs. 5 and 6. Figure 5.
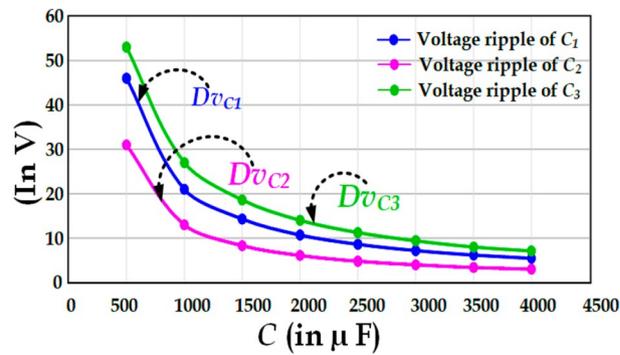
**Figure 6.** The capacitor voltage ripple vs the value of capacitance for the capacitors $C_1$, $C_2$, and $C_3$.
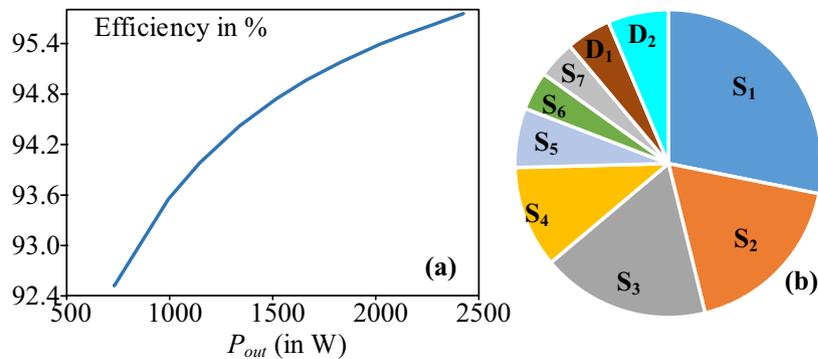


**Figure 7.** (**a**) Efficiency vs the output power curve and (**b**) loss distribution considering various power switches at 2.4 kW. (PLECS V4.1.2- https://www.plexim.com/).

shows that the inductor current ripple varies with the inductance $L_{in}$. However, the output power is also slightly influenced by the inductance variation, as observed from Fig. 5. From the curve given in Fig. 5, the inductance value of $L_{in}$ is chosen as 3 mH which corresponds to 600 W and 30 A current ripple.

Figure 6. shows the capacitor voltage ripple vs capacitance for the capacitors $C_1$, $C_2$, and $C_3$. It may be observed that $C_3$ has a slightly higher voltage ripple than $C_1$ or $C_2$ whereas $C_2$ has the lowest voltage ripple. It is worth noting that this curve is plotted by considering $C_1 = C_2 = C_3 = C$.

*Loss analysis:* Loss analysis of the proposed topology is carried out in PLECS software with the following devices models: IKW30N60T_IGBT and IKW30N60T_Diode. The loss analysis is carried out with the following parameters: $V_{in} = 50$ V, $L_{in} = 5$ mH, $C_1 = C_2 = C_3 = 3000$ μF, and $f_s = 5$ kHz. The efficiency vs output power curve is shown in Fig. 7a where a drop in efficiency is observed at lower output power. The loss distribution for various switches in the proposed topology is shown in Fig. 7b for 2.4 kW. It may be observed that the losses for switch $S_1$ is higher than the other devices. In fact maximum amount loss of the system is shared by the switches $S_1$, $S_2$, $S_3$, and $S_4$.

## Results and discussions

The prototype hardware setup of proposed topology is shown in Fig. 8. The Semikron IGBT 600 V/75A is used in this circuit. Further, the TLP 250 driver circuits is used with external RC delay circuit to provide the deadtime of 3 μs—4 μs for each switch to avoid the short circuit. Moreover, the 3 mH iron core inductor is used, and 3000 (F capacitance capacitors are used. Initially, the input voltage is given to the circuit and the switch $S_1$ is turned on/off to boost the voltage. The pulses are generated from the MATLAB and embedded into the texas controller TMS320F28379D. The Keysight DSOX2002A probe is used to measure the voltage and probe can withstand up to 300Vrms and there was a small voltage fluctuation during the experimental measurement. Since the output power is low, the waveforms are not affected.. Figure 9a shows the measured value of output voltage, current and inductor current during the steady-state condition for the RL load (50Ω + 100mH) @ power factor of 0.85 lagging. The maximum output voltage ($v_{o,max}$) is 200 V, maximum output current ($i_{o,max}$) = 3.3 A. Further, the voltage across the inductor is maintained at 100 V and the maximum current is 25 A as shown in Fig. 9b. Moreover, the capacitor across the voltage $C_1$ and $C_2$ is captured and shown in Fig. 9b. Further to investigate the proposed topology is dynamic performances, the modulation index variation and load variations are applied and results are measured as shown in Fig. 10a and b. The modulation index is reduced from the 1.0 to 0.45 by varying the potentiometer. From Fig. 10, it is confirmed that the voltages of the capacitors are slightly reducing during the low modulation index. This is because the duration of top negative level is reduced, where the inductor gets continuously charged. However, the capacitors are discharged during the negative cycle.
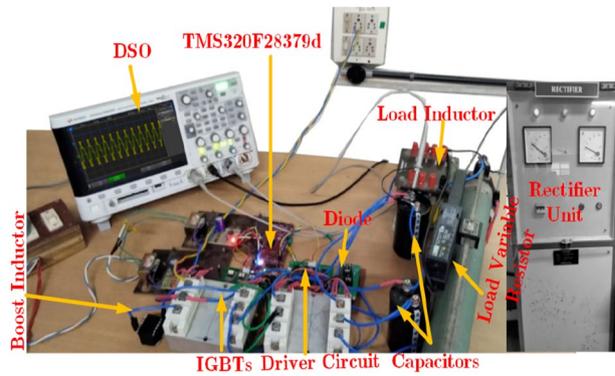
**Figure 8.** Prototype Hardware Setup.
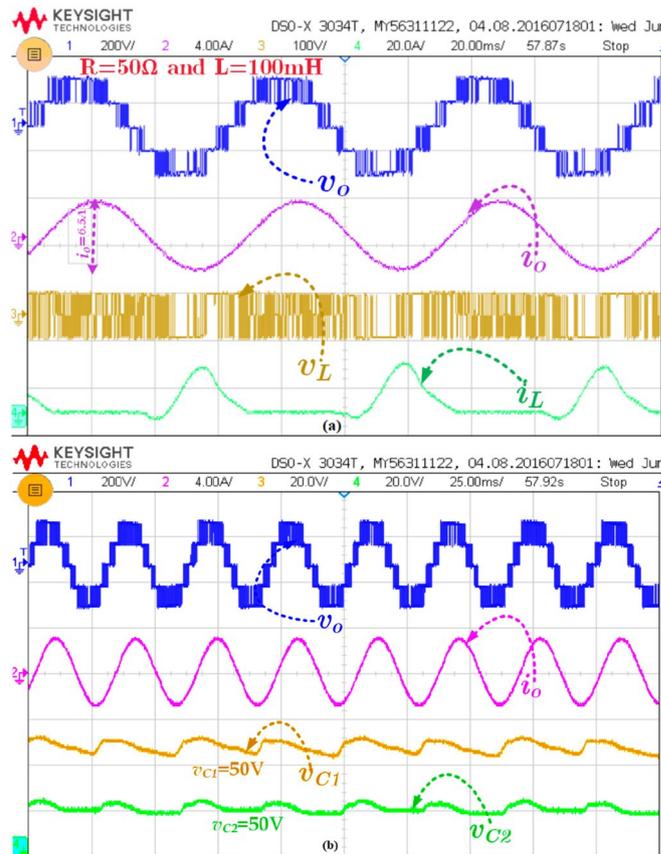


**Figure 9.** Experimental result of (a) $v_o$, $i_o$, $v_L$, and $i_L$ for R = 50 Ω and L = 100 mH and (b) $v_o$, $i_o$, $v_{C1}$, and $v_{C2}$.

Most of the inverter loads are highly dynamic in behaviour. Therefore, a highly reliable topology is needed to adopt the load variations. The proposed topology is verified under the varying load condition, and the corresponding results are shown in Fig. 11. In fact, the load variations are carried out by keeping the load inductance constant but varying the resistance of the rheostat.

The capacitor ($C_1$) current and voltages are measured during this load variation, as shown in Fig. 11a. The capacitor voltage from the initial duration is shown in Fig. 11a. This waveform is captured by discharging all the capacitors used in the circuit. In fact, the capacitor charging is too high due to the low resistance series to the capacitors. The various capacitors and their currents and switch currents are shown in Fig. 11b. Without the inductor, the charging will be ten times higher than the load current, but the inductor, which acts as a current limiter, limits the maximum charging current.

The summary for the comparison of recent switched capacitor and common ground type topologies are listed in Table 2. In this[16], uses the ten switches whereas the proposed topology uses seven switches with additional two diodes. It is worth mentioning that the diode is lower than the switches and doesn't require gate driver circuits. Obviously, the cost of the proposed topology is less than the[16] and achieves better performance. Another CG-type
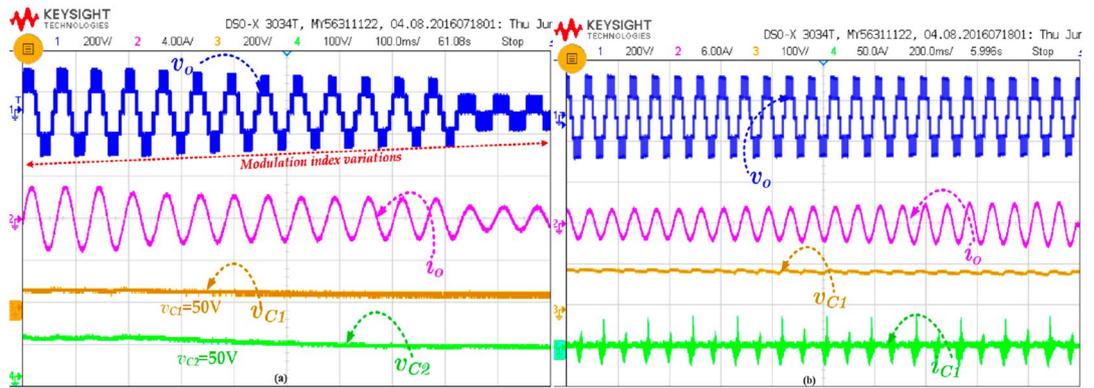
**Figure 10.** Experimental result of (**a**) modulation index variations and (**b**) load variations.
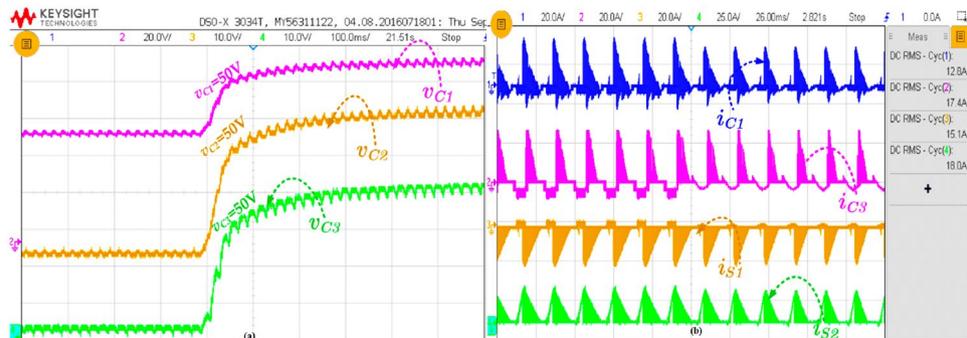


**Figure 11.** Experimental result of (**a**) capacitors voltages and (**b**) voltage and current of capacitors $C_1$ and switch $S_1$.

| Ref | $N_L$ | $N_{S+DC}$ | $N_D$ | $N_{SC}$ | $T_C$ | $v_{SC}$ | G | $I_{CC}$ | Efficiency (%) |
|---|---|---|---|---|---|---|---|---|---|
| [8] | 5 | 8 + 8 | – | 1 | 17 | $v_{in}$ | M | No | 97 |
| [9] | 7 | 8 + 8 | 1 | 2 | 19 | $2v_{in}$ | M | No | 96.3 |
| [14] | 5 | 6 + 6 | 2 | 2 | 16 | $2v_{in}$ | $2v_{in}$ | No | 98.1 |
| [15] | 5 | 8 + 6 | 1 | 2 | 17 | $2v_{in}$ | $2v_{in}$ | No | 96 |
| [16] | 5 | 10 + 10 | – | 2 | 22 | $2v_{in}$ | 2 M/(1-D) | Yes | 97.13 |
| [17] | 5 | 7 + 6 | 2 | 2 | 17 | $2v_{in}$ | M/(1-D) | Yes | 97 |
| [18] | 5 | 10 + 8 | – | 2 | 20 | $2v_{in}$ | 2 M/(1-D) | Yes | 98.2 |
| Prop | 5 | 7 + 7 | 2 | 3 | 19 | $2v_{in}$ | 2 M/(1-D) | Yes | 94.5 |

**Table. 2.** Summary Comparison. $N_L$-Number of level, $N_{S+DC}$-Number of switch and driver circuits, $N_D$-number of diodes, $N_{SC}$-Number of switched capacitor and $T_C$-total power component, $V_{SC}$-voltage rating of SC, G-voltage gain and $I_{CC}$-Input continuous current.

topology[17,18] topologies generate the five-level with boosting factor 2 M/(1-D). However, these topologies' switch count is high but in[17], the voltage gain is half of the proposed topology. Further, the series connection of dc source and capacitors will introduce the pulsating dc which affect the source. The simulated total harmonics distortion (THD) for the proposed topology is shown in Fig. 12 without output filter. The voltage THD is 34.64% and for current THD 2.19%. Finally, the voltage across the switches ($V_{S1}$-$V_{S7}$) is given in Fig. 13 and its confirming that the maximum blocking voltage is not more than output voltage ($v_o$).

## Conclusion

A new five-level inverter topology with the common ground was discussed. The detailed operation of each mode and PWM scheme was presented. The integrated boost inverter is operated so that it suppresses the SC charging current and boosts the input voltage. The extended structure of the proposed topology was also discussed. Since the 5L-QBI is a common ground type, the leakage current is eliminated, allowing the proposed topology to be more suitable for transformerless applications. The main advantage of the proposed topology is the availability

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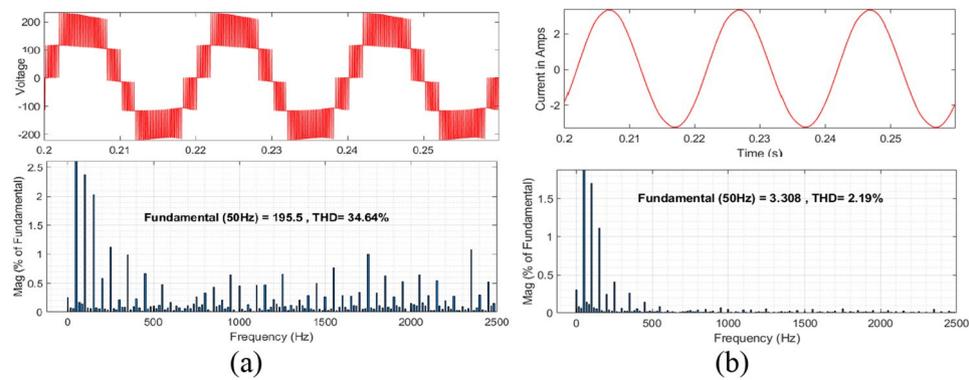
**Figure 12.** Totalharmonic distortion (**a**) for Voltage and (**b**) for current.
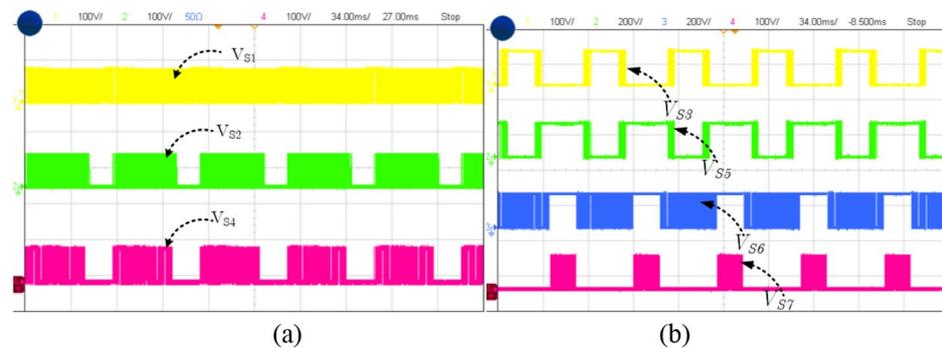


**Figure 13.** Voltage across the switches (**a**) $V_{S1}$, $V_{S2}$, $V_{S4}$ and (**b**) $V_{S1}$, $V_{S2}$, $V_{S4}$.

of the charging state for every switching state except the -2 level. Further, the number of devices and rating of the devices is less than the similar topologies. A measured efficiency value is 94.21% at ~ 600 W, which is close to the simulation value of 94.8%. From the above points, the proposed topology is a suitable candidate for transformerless PV application with reduced device count, reduced current stress, and voltage boosting capability.

## Data availability
The datasets analyzed during the current study are available from the corresponding author on reasonable request.

## References
1. Pakdel, M. & Jalilzadeh, S. A new family of multilevel grid connected inverters based on packed U cell topology. *Sci. Rep.* **7**, 12396 (2017).
2. Xu, S. *et al.* Fault-tolerant control of ANPC three-level inverter based on order-reduction optimal control strategy under multi-device open-circuit fault. *Sci. Rep.* **7**, 14447 (2017).
3. Sathik, M. J. *et al.* Experimental validation of new self-voltage balanced 9L-ANPC inverter for photovoltaic applications. *Sci. Rep.* **11**, 5067 (2021).
4. Almakhles, D. J. A new seven level boost-type ANPC inverter topology for photovoltaic applications. *Sci. Rep.* **11**, 22487 (2021).
5. Li, W. *et al.* Topology review and derivation methodology of single-phase transformerless photovoltaic inverters for leakage current suppression. *IEEE Trans. Ind. Electron.* **62**(7), 4537–4551 (2015).
6. Zhu, X. *et al.* Leakage current suppression of single-phase five-level inverter for transformerless photovoltaic system. *IEEE Trans. Ind. Electron.* **68**(11), 10422–10435 (2021).
7. Xiao, H. Overview of transformerless photovoltaic grid-connected inverters. *IEEE Trans. Power Electron.* **36**(1), 533–548 (2021).
8. Kadam, A. & Shukla, A. A multilevel transformerless inverter employing ground connection between pv negative terminal and grid neutral point. *IEEE Trans. Ind. Electron.* **64**(11), 8897–8907 (2017).
9. Grigoletto, F B. Multilevel common-ground transformerless inverter for photovoltaic applications. *IEEE J. Emerg. Sel. Topics in Power Electron.* 9(1), 831–842, (2021).
10. Siwakoti, Y. P. & Blaabjerg, F. Common-ground-type transformerless inverters for single-phase solar photovoltaic systems. *IEEE Trans. Ind. Electron.* **65**(3), 2100–2111 (2018).
11. Chattopadhyay, S. K. & Chakraborty, C. A new multilevel inverter topology with self-balancing level doubling network. *IEEE Trans. Ind. Electron.* **61**(9), 4622–4631 (2014).
12. Sandeep, N. *et al.* Common-ground-type five-level transformerless inverter topology with full DC-bus utilization. *IEEE Trans. Ind. Appl.* **56**(4), 4071–4080 (2020).

13. Sathik, M. J., Sandeep, N., Siddique, M. D., Almakhles, D. & Mekhilef, S. Compact Seven-Level Boost Type Inverter Topology. *IEEE Trans. Circuits Syst. II Express Briefs* **68**(4), 1358–1362 (2021).
14. Vosoughi, N., Hosseini, S. H. & Sabahi, M. A new transformer-less five-level grid-tied inverter for photovoltaic applications. *IEEE Trans. Ene. Conv.* **35**(1), 106–118. https://doi.org/10.1109/TEC.2019.2940539 (2020).
15. Kumari, S., Verma, A. K., Sandeep, N., Yaragatti, U. R. & Pota, H. R. A five-level transformer-less inverter with self-voltage balancing and boosting ability. *IEEE Trans. Ind. Appl.* **57**(6), 6237–6245. https://doi.org/10.1109/TIA.2021.3116222 (2021).
16. Jagabar Sathik, M., Hota, A., Sandeep, N., Almakhles, D., A single-stage common ground type transformerless five-level inverter topology. *IEEE J. Emerg. and Sel. Topics Power Electron.*, (*early view*) (2021)
17. Barzegarkhoo, R. *et al.* Implementation and analysis of a novel switched-boost common-ground five-level inverter modulated with model predictive control strategy. *IEEE J. Emerg. and Sel. Topics Power Electron.* **10**(1), 731–744. https://doi.org/10.1109/JESTPE.2021.3068406 (2022).
18. Barzegarkhoo, R., Lee, S. S., Siwakoti, Y. P., Khan, S. A. & Blaabjerg, F. design, control, and analysis of a novel grid-interfaced switched-boost dual t-type five-level inverter with common-ground concept. *IEEE Trans. Ind. Electron.* **68**(9), 8193–8206 (2021).
19. S. S. Lee, Y. P. Siwakoti, R. Barzegarkhoo, F. Blaabjerg, A novel common-ground-type nine-level dynamic boost inverter, *IEEE J. Emerg. Sel. Topics Power Electron.* https://doi.org/10.1109/JESTPE.2021.3104939.

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## Author contributions

All authors have contributed equally to the work. J.S. wrote the main manuscript text and prepared the figures, tables and developed the experimental hardware setup. D.A. validated the experimental results, reviewed the paper and corrected the grammatical mistakes. All authors contributed to and have approved the final manuscript.

## Competing interests

The authors declare no competing interests.

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