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Performance and reliability improvement in intercalated MLGNR interconnects using optimized aspect ratio

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In this work, aspect ratio of various intercalation doped MLGNR interconnects are optimized using a numerical approach to achieve improved performance and reliability. A numerical optimization method is presented to estimate optimized aspect ratio considering combined effects of performance, noise and reliability metrics for any arbitrary nano interconnect system. This approach is cost effective and will be extremely useful to industry for selection of aspect ratio of interconnects as it is a non-SPICE method and reduces fabrication iterations for achieving desired performance and reliability. Our numerical method suggests that by minimizing the figure of merit (i.e. Noise Delay Power Product / Breakdown Power P_{BD} ratio), aspect ratio of $FeCl_3$ doped MLGNR interconnect is optimized at 0.987, 0.61 and 0.579 for local, intermediate and global level, respectively at 7 nm node. Comparing the optimized performance metrics in this work with the estimated metrics at prescribed aspect ratio by *IRDS* roadmap, delay, noise delay product (*NDP*), power delay product (*PDP*), PDP/P_{BD} ratio and figure of merit are improved by (∼2% and ∼25%), (∼44% and ∼50%), (∼9% and ∼48%), (∼6% and ∼48%) and (∼49% and ∼68%) for 10 μ m and 1 mm long $Fecl_3$ doped MLGNR interconnect, respectively at 7 nm node. Increase in contact resistance leads to significant decrease in performance and increase in optimized aspect ratio of local $Fecl_3$ doped MLGNR interconnect. Scaling down from 10 to 7 nm node results in increase of optimized aspect ratio in all levels of interconnects. Even though the performance of MLGNR degrades with scaling down but when compared to copper, the performance improves with technology scaling. Finally, this study provides circuit designers a detailed guideline for selecting an optimized aspect ratio for achieving better performance, power efficiency and reliability in doped MLGNR interconnects.

Copper interconnects have reached their performance limits due to high resistivity, grain boundary scattering effects and electromigration issues[1]. Their current carrying capacity has reduced resulting in poor IC performance[2,3]. Other alternative materials such as cobalt and ruthenium were proposed due to their higher EM reliability even though they have higher resistivity than copper[4,5]. Graphene nanoribbons (*GNRs*) have proved to have high conductivity, great electromigration reliability and superior transport properties making them more suitable as an alternative interconnect material than copper[6,7].

Multilayer Graphene Nanoribbons (*MLGNRs*) are preferred over single layer graphene because of their lower resistivity. However, due to inter-sheet electron hopping, it suffers from decrease in conductivity. To solve this issue, intercalation doped *MLGNRs* were first proposed by Xu et al.[6]. Sahoo et al. analyzed the crosstalk and reliability effects in MLGNR interconnects in[8]. Liao et al. in[9] investigated high field transport in GNRs up to breakdown. In[10], Jiang et al. proposed $Fecl_3$ doped MLGNR for better performance and reliability to challenge copper as an interconnect. They showed that $Fecl_3$ doping is very efficient for diffusion in scaled MLGNRs, is stable at room temperature and shows excellent current carrying capacity >200 MA/Cm^2. But Jiang et al. did not consider the effects of via and aggressor nets which is a pressing concern in IC design. Agashiwal et al. in[11] engineered a CMOS-compatible solid-phase growth technique to yield large-area multilayer graphene on dielectric (SiO) and metal (Cu) substrates and subsequently demonstrating multi-level interconnects with metal vias. Also, Fischer and his team demonstrated an ingenious method in[12] to produce metallic GNRs based on the atomically precise

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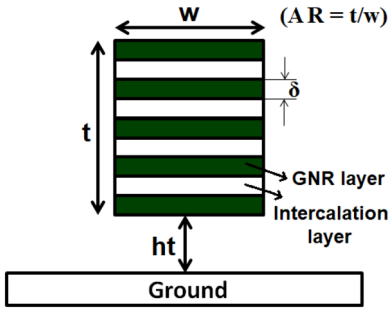

Figure 1. Structural representation of doped MLGNR interconnect.

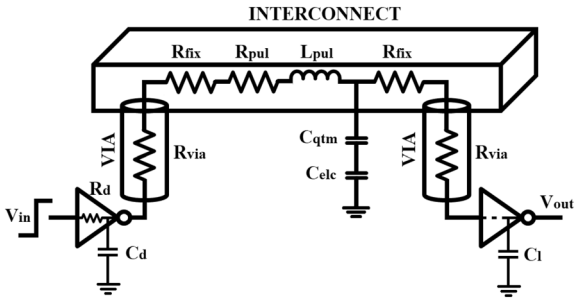

Figure 2. Electrical equivalent of MLGNR interconnect system.

bottom-up synthesis. These fabricational advancements have strengthened the claim of graphene nanoribbons as an effective alternative to commercial metals. Wang et al. in[13] also advertised graphene nanoribbon as a promising candidate for quantum electronic applications praising its high mobility and current-carrying capability. Nishad et al. in[14] optimized thickness of Lithium and AsF_5 intercalated Top-Contact MLGNR (TC-MLGNR) interconnects and compared with copper and pristine interconnects. Both Jiang et al. and Nishad et al. have not shown any dimensional optimization for improved performance and reliability issues which is a concerning factor to consider for commercialization of MLGNR interconnects in near-future VLSI circuits.

In this work, a numerical model is developed for optimization of aspect ratio (*AR*) by minimizing delay and FOM ($NPDP/P_{BD}$ ratio) for local, intermediate and global level MLGNR interconnects considering different intercalation dopants. This model is supported by the simulation results provided in "Results and discussion" section . Delay, Delay/P_{BD}, *NDP* and *PDP*, PDP/P_{BD} and $NPDP/P_{BD}$ are compared by considering *AR* prescribed by IRDS 2018 roadmap[1] and the optimized *AR* obtained from this work (for $FeCl_3$ doped MLGNR). Impact of scaling on optimization of *AR* is studied for two representative nodes, 7 *nm* and 10 *nm*. Effect of contact resistance on numerically optimized *AR* is shown which acts as an important factor in sub-10 nm technology nodes. Our study is in accordance with the trends observed in IRDS roadmap. A realistic model including the effects of crosstalk and vias is adopted which is not considered in[10]. Modeling of coupled three conductor line system shown in Fig. 3 is performed in Verilog-A. This proposed numerical methodology is applicable to all types of nano-interconnects making it a generalized model. We have validated this model with experimental data from[10] and simulation data from[14].

The remainder of the paper is organized as follows: "Circuit modeling of MLGNR interconnects—an overview" section presents the equivalent electrical model of MLGNR interconnects. "Formulation and methodology" section proposes an numerical model for optimizing *AR*. "Results and discussion" section presents the simulation results. Finally, "Conclusion" section concludes this paper.

Circuit modeling of MLGNR interconnects—an overview

The structural representation of MLGNR interconnect is shown in Fig. 1. Here, thickness and width are denoted by *t* and *w*, respectively and *ht* denotes the height of interconnect above ground plane. The spacing between two layers of MLGNR is represented by δ. The advantage of doping is that each layer of intercalated MLGNR can be understood as stacked single layer *GNR*s because these layers do not have any interaction with each other. So, every layer of MLGNR can be modeled as Equivalent Single Conductor (*ESC*) model as shown in Fig. 2.

Electrical equivalent model of MLGNR interconnect system is shown in Fig. 2 where driver and load (at active device level) are connected to the interconnect metal line though vias. Copper is chosen as the via material in this study whose dimensions are taken from IRDS 2018 roadmap.

The electrical circuit of MLGNR interconnect model consists of lumped resistance, ($R_{fix} = \frac{R_{con}+R_{qtm}}{2}$) where R_{con} is the imperfect contact resistance (MLGNR to Nickel contact) which is taken as $6\,\Omega - \mu m/W$[10]. R_{qtm} is the quantum resistance which is given by[8],

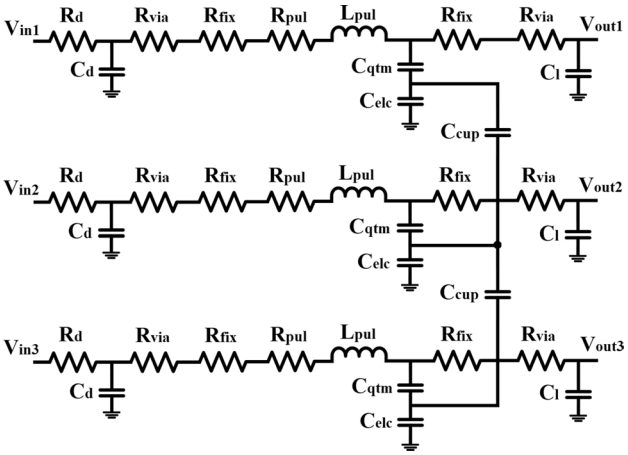

Figure 3. Electrical equivalent of three-line MLGNR interconnect system.

$$R_{qtm} = \frac{\frac{h}{2q^2}}{N_{ch}N_{oL}} = \frac{12.94K\Omega}{N_{ch}N_{oL}} \tag{1}$$

where N_{oL} denotes the total number of layers present in MLGNR and and N_{ch} represents number of conducting channels associated with each layer of MLGNR[8].

The per unit length (p.u.l) distributed resistance of MLGNR as shown in Fig. 2 can be calculated as[6],

$$R_{pul} = \frac{1}{G_{pul} * N_{oL}} \tag{2}$$

where G_{pul} represents the p.u.l conductance of a single layer MLGNR as expressed below[6],

$$G_{pul} = \frac{2q^2}{h} f(\lambda_D, w) \frac{2w^2}{h v_f} 2K_b T log\left(2cosh\left(\frac{E_f}{2K_b T}\right)\right) \tag{3}$$

where q is the elementary charge, h is Planck's constant, $v_f = 10^6$ m/s is the Fermi velocity, E_f is the Fermi level, K_b is Boltzmann's constant, T is the temperature (here room temperature is considered), w is the width of the MLGNR and $f(i, \lambda_D, w)$ as expressed in[10], is a function of specularity parameter where, $i = (1 - P)$, λ_D is the mean free path determined by the Matthiessen's equation[10]. P represents specularity index which is a measure of specularity of GNR edges. $P = 1$ means completely specular edges whereas $P = 0$ implies completely diffusive edges[6].

The p.u.l capacitance (C_{pul}) is a series combination of quantum capacitance (C_{qtm}) and electrostatic capacitance (C_{elc}) as described below[15].

$$C_{qtm} = N_{ch}N_{oL}.\frac{4q^2}{h v_F} = N_{ch}N_{oL} \times 193.18aF/\mu m \tag{4}$$

$$C_{elc} = C_{gnd} + C_{inter} + C_{intra} \tag{5}$$

where C_{gnd}, C_{inter} and C_{intra} are wire to ground capacitance, inter-layer capacitance and intralayer capacitance, respectively explained in detail in[15].

The coupling capacitance between two interconnect lines as shown in Fig. 3 is given by[8],

$$C_{cup} = \epsilon_0 \epsilon_r \left[1.14\frac{t}{S}\left(\frac{ht}{ht + 2.06S}\right)^{0.09} + 0.74\left(\frac{w}{w + 1.59S}\right)^{1.14} + 1.16\left(\frac{w}{w + 1.87S}\right)^{0.16}\left(\frac{ht}{ht + 0.98S}\right)^{1.18}\right] \tag{6}$$

where ϵ_0 and ϵ_r are the dielectric constant and permittivity in the free space, respectively. t denotes the thickness of MLGNR, ht represents the height of the interconnect above ground plane and S is spacing between adjacent interconnects.

The p.u.l inductance (L_{pul}) of MLGNR is sum of p.u.l kinetic inductance (L_{kn}) and self inductance (L_{sf}) and is expressed as $L_{pul} \approx (L_{kn} + L_{sf})$[15]. L_{sf} and the electrostatic capacitance (C_{elc}) of MLGNR are considered same as of copper interconnect having equal dimensions[10]. Here, we have ignored the mutual inductance because the analysis is done for low/mid frequency range where effect of mutual inductance is negligible.

The capacitance model used for copper and cobalt interconnect is taken from[8] and the resistance model is described in[4] where 30% of the copper line is occupied by liner and cobalt has no liner.

Properties	Neutral[6]	AsF_5[22]	$FeCl_3$[10,22]	Lithium[14,23]
Stage of intercalation	NA	Stage 1	Stage 2	Stage 1
Mean free path (μm)	0.42	1.03	1	1.76
Fermi level (eV)	0.2	0.6	0.68	1.5
Avg layer Spacing (nm)	0.34	0.575	0.47	0.37

Table 1. Electronic properties of different intercalated MLGNR interconnects.

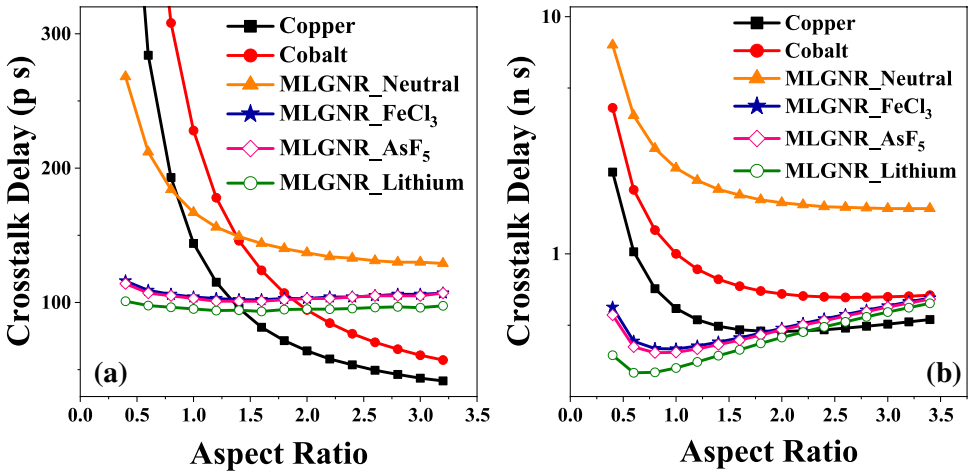

Figure 4. Optimized *AR* at minimum crosstalk induced delay in (**a**) intermediate level (L = 10 μm) and (**b**) global level (L = 1 mm) interconnects.

Results and discussion

The simulations are carried out in Cadence Virtuoso, version IC 6.1.6-64B.5004 under standard desktop environment. The coupled three conductor model as described in Fig. 3 is modeled using Verilog-A including the effects of vias ad crosstalk. IRDS 2018 roadmap[1] is considered for extracting the parameters used in the calculations. 7 *nm* technology node is used for intermediate and global level interconnects.

Length of local level (Metal line 1), intermediate level (Metal level 2) and global level (Metal level 6) interconnects are considered as 500 *nm*, 10 μm and 1 *mm*, respectively. Nearly specular (i.e. $P = 0.8$) MLGNR interconnects is considered for all the calculations. Properties of various intercalated MLGNR interconnect materials are described in Table 1.

Aspect ratio is varied from 0.4 to 3.2 for intermediate level and 0.4 to 3.4 for global level interconnects. Width of local level (Metal line 1) interconnects is considered as w_{min} as specified in IRDS roadmap[1] for 7 and 10 nm nodes. It is taken as 1.5 times the w_{min} for intermediate level and 5 times the w_{min} for global level as specified in IRDS roadmap[1] to reduce delay and power consumption[24].

Optimizing AR by minimizing various metrics. Figure 4 shows the optimized *AR* in AsF_5, $Fecl_3$, Lithium doped MLGNR, neutral MLGNR, cobalt and copper interconnects. Intercalated MLGNR experiences very low delay when compared to neutral MLGNR and conventional metals irrespective of interconnect length for smaller *AR*. The *AR* for intermediate level, AsF_5, $FeCl_3$, *Lithium* doped MLGNR optimizes at 1.4, 1.4 and 1.2 for intermediate level and at 1.0, 1.0 and 0.8 for global level interconnects. Delay in neutral MLGNR and copper interconnect saturates for higher *AR*. Also it can be observed that copper and cobalt interconnects outperform all the doped MLGNRs after reaching an *AR* value of 1.4 and 1.8, respectively for intermediate level. Also, copper performs better than $Fecl_3$ doped MLGNR for an *AR* value of 2.0 or higher for global level interconnects. *AR* of global level interconnects optimizes at larger value as compared to intermediate level because of higher resistance as implied by Fig. 14 and this trend matches with the IRDS suggestion.

Optimized *AR* at minimum *NDP* is shown in Fig. 5. AsF_5, $Fecl_3$, Lithium doped MLGNR is optimized at 0.8, 0.8 and 0.6 for intermediate level and at 0.6 for global level interconnects. Intermediate level copper and cobalt cut all the doped MLGNR at *AR* value of 1.6 and 2, respectively. Hence, intermediate level MLGNR interconnects are more prone to noise for higher *AR* as compared with copper and cobalt as shown in Fig. 5a. But Fig. 5b shows that this is not the case for global level interconnect.

Figure 6a,b show power consumption in cobalt, copper, neutral and various doped MLGNR interconnects for intermediate and global level respectively. Switching power is the dominating factor in total power consumed by the repeaters. P_{switch} increases as *AR* increases. So, interconnects with large *AR* consume more power as

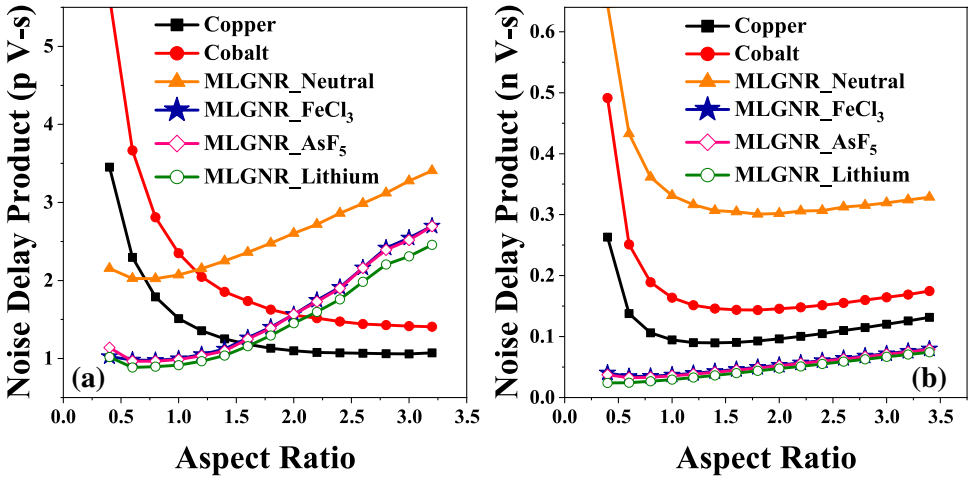

Figure 5. Optimized *AR* at minimum noise delay product in (**a**) intermediate level (L = 10 μm) and (**b**) global level (L = 1 mm) interconnects.

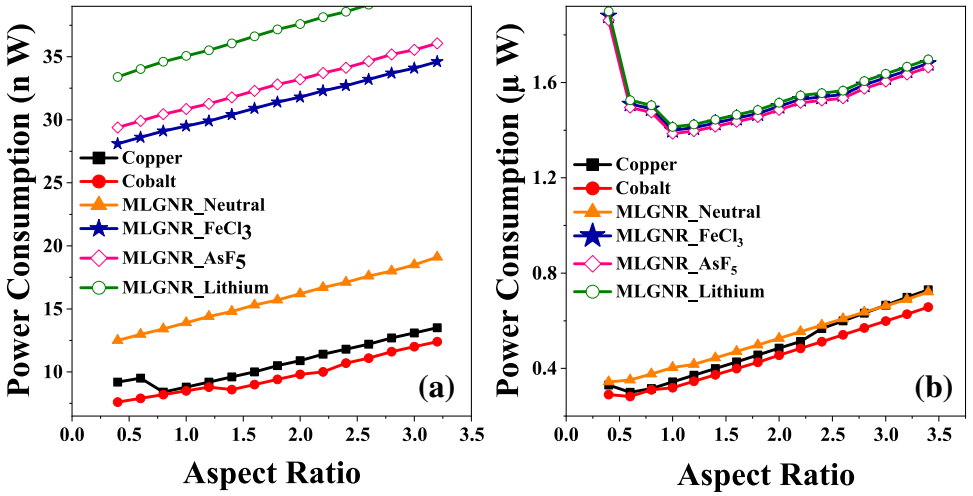

Figure 6. Comparison of power consumption in interconnects at (**a**) intermediate level (L = 10 μm) and (**b**) global level (L = 1 mm) interconnects.

inferred from Fig. 6. Cobalt interconnect consumes least power among others as it has lower capacitance and higher resistance value.

The least *PDP* is obtained at *AR* value of 1.0, 1.0 and 0.6 for intermediate level AsF_5, $Fecl_3$, Lithium doped MLGNR interconnects but copper and cobalt beats them at even lower *AR* as shown in Fig. 7a. Figure 7b shows optimization at 0.8 which is also the crossing point after which copper exceeds all the doped MLGNR interconnect.

Figure 8 shows the variation of breakdown power with respect to aspect ratio of interconnects. Here, we can see an increasing curve of breakdown power as the aspect ratio increases. Thermal healing length increases with an increase in *AR*. Breakdown power is a function of thermal healing length for intermediate level when L_{TH} is comparable to GNR length. doped MLGNRs appear to be the most reliable candidates among all as they have large breakdown power.

The optimization of *AR* by minimizing the metric $(Power * Delay/P_{BD})$ is shown in Fig. 9. The optimization for AsF_5, $Fecl_3$, Lithium doped MLGNR interconnects are obtained at 1.0, 1.0 and 0.6. In case of cobalt and copper interconnects, the metric decreases with increasing *AR*.

We have considered the metric $(Noise * Delay * Power/P_{BD})$ as the Figure of Merit (FOM) which gives a measure of performance, noise, power consumption and reliability effects. The optimization of *AR* by minimizing this FOM for intermediate level interconnects is shown in Fig. 10. Here, we get an optimization AsF_5, $Fecl_3$, Lithium doped MLGNR interconnects at 0.6, 0.6 and 0.5, respectively. The FOM first decreases and then saturates with increasing *AR* for neutral MLGNR. It keeps decreasing with increasing *AR* for cobalt and copper interconnects. Doped MLGNRs are far better candidates considering an overall performance and reliability aspect specially at lower *AR*. Although Lithium dopant gives the highest advantage but $Fecl_3$ is explored more in

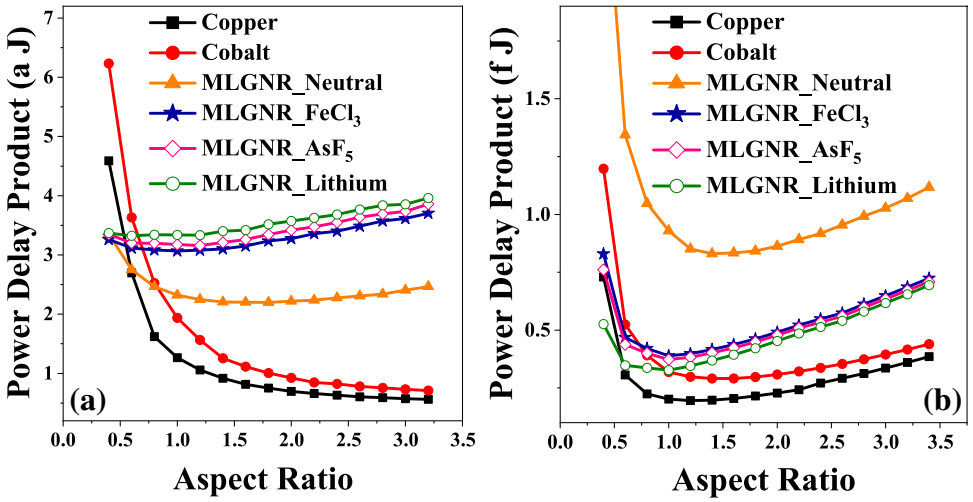

Figure 7. Optimized *AR* at minimum power delay product in (**a**) intermediate level (L = 10 μm) and (**b**) global level (L = 1 mm) interconnects.

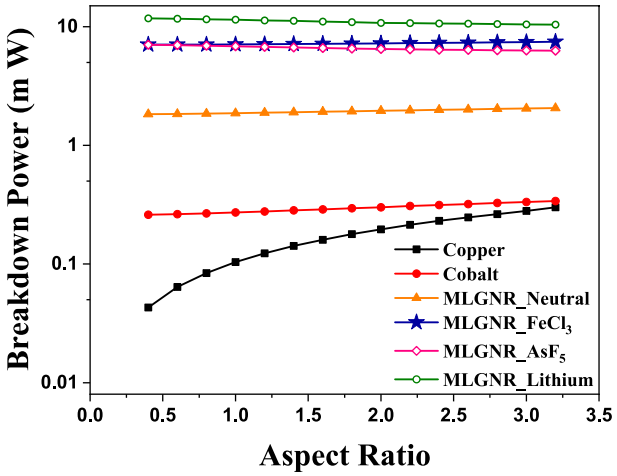

Figure 8. Variation of breakdown power versus aspect ratio for 10 μm long interconnects.

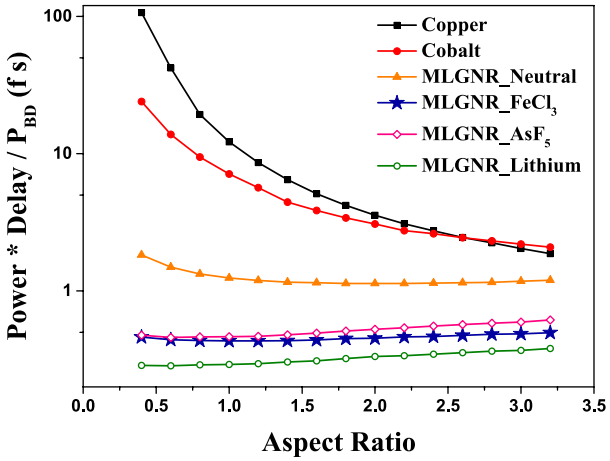

Figure 9. Optimized *AR* at minimum (power delay product/breakdown power) for 10 μm long interconnects.

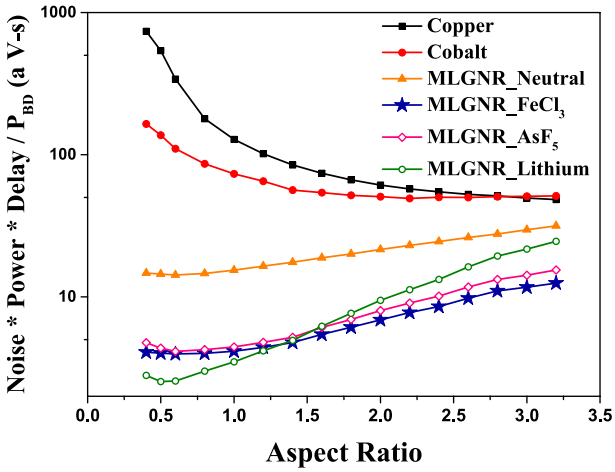

Figure 10. Optimized *AR* at minimum (noise power delay product / breakdown power) for 10 μm long interconnects.

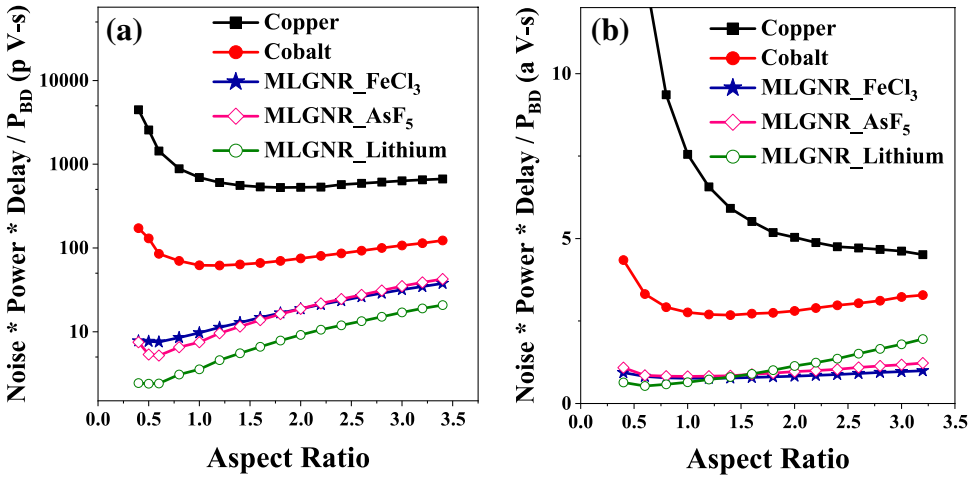

Figure 11. Optimized *AR* at minimum (noise power delay product / breakdown power) in (**a**) global level (L = 1 mm) and (**b**) local level (L = 500 nm) interconnects.

Performance metrics	Results[10]	Our results
Delay ($p-sec$)	5.5	5.236
Energy (x$10^{-16}J$)	2.80	2.648
Power (μW/mm)	20.8	19.49

Table 2. Calibration of our results ($FeCl_3$ doped interconnect) with[10] at 11 nm technology node.

experimental literature's. Figure 11a,b show the optimization for global and local level interconnects, respectively. FOM for global level AsF_5, $Fecl_3$, Lithium doped MLGNR interconnects are minimum at *AR* of 0.6, 0.6 and 0.5, respectively. And for local level it is 1.0, 1.0 and 0.6, respectively. Doped MLGNR interconnect outperforms all other candidates by having minimum FOM at all metal levels as shown in Figs. 10 and 11. Thus we propose swapping all the metal lines (conventional copper lines) with any doped MLGNR interconnect in order to achieve performance as well as reliability.

Validation with existing results. For calibration of the electrical model, we have estimated delay, energy and power consumption in $FeCl_3$ doped MLGNR at 11 nm technology node utilizing the models described in this work (refer "Circuit Modeling of MLGNR Interconnects - An Overview" section) and compared them with

Optimization parameters	Optimized AR (Existing Works)	Optimized AR (Numerical Model)
Minimizing Delay of $FeCl_3$ doped MLGNR interconnect	0.8[10]	0.88
Minimizing Delay of AsF_5 doped TC-MLGNR interconnect	0.958[14]	1.04
Minimizing Delay ofLithium doped TC-MLGNR interconnect	0.802[14]	0.871
Minimizing EDP of AsF_5 doped TC-MLGNR interconnect	0.479[14]	0.52
Minimizing EDP of *Lithium* doped TC-MLGNR interconnect	0.37[14]	0.415

Table 3. Validation of our numerical model (section "Formulation and methodology") with[10] and[14].

Performance metrics	IRDS specs	Our results	% decrease
Intermediate level (L=10 μm)	(AR = 2.1)		
Delay ($p-sec$)	104	102 (optimized AR = 1.4)	1.92
NDP ($pV-sec$)	1.75	0.975 (optimized AR = 0.8)	44
PDP ($aW-sec$)	3.36	3.07 (optimized AR = 1.0)	8.63
PDP/P_{BD} ratio ($f-sec$)	0.46	0.43 (optimized AR = 1.0)	6.28
NPDP/P_{BD} ratio ($aV-sec$)	7.765	3.97 (optimized AR = 0.6)	48.85
Global level (L=1 mm)	(AR = 2.3)		
Delay ($n-sec$)	0.531	0.397 (optimized AR = 1.0)	25.2
NDP ($nV-sec$)	0.088	0.044 (optimized AR = 0.6)	50.45
PDP ($fW-sec$)	0.467	0.243 (optimized AR = 0.8)	48
PDP/P_{BD} ratio ($f-sec$)	0.142	0.074 (optimized AR = 0.8)	48
NPDP/P_{BD} ratio ($aV-sec$)	23.51	7.541 (optimized AR = 0.6)	68

Table 4. Comparison of our results (considering $FeCl_3$ doped MLGNR interconnect) with IRDS 2018 Roadmap suggestion of Aspect Ratio (for copper interconnect)[1] at 7 nm technology node.

	Optimized AR (FOM value)		
Contact resistance	Local	Intermediate	Global
5 $K\Omega$	0.87 (0.567 aV-sec)	0.617 (3.97 aV-sec)	0.58 (7.541 pV-sec)
10 $K\Omega$	1.02 (0.765 aV-sec)	0.62 (4.01 aV-sec)	0.582 (7.547 pV-sec)
15 $K\Omega$	1.09 (1.07 aV-sec)	0.626 (4.07 aV-sec)	0.586 (7.556 pV-sec)
20 $K\Omega$	1.18 (1.8 aV-sec)	0.633 (4.2 aV-sec)	0.591 (7.57 pV-sec)

Table 5. Impact of contact resistance on optimized AR and FOM $Fecl_3$ doped MLGNR interconnects at 7 nm technology node.

results obtained by Jiang et al.[10]. The comparison is shown in Table 2. All the dimensional parameters are taken from[10] for comparison.

Also to validate our numerical model, comparison is shown in Table 3. Optimized AR estimated using our numerical model is compared with that obtained from existing works[10,14]. All the dimensional parameters are considered to be same as in respective papers for a fair comparison.

Comparison with IRDS roadmap suggestion. Table 4 shows a comparison between our results (considering $FeCl_3$ doped MLGNR interconnect) and results obtained using IRDS roadmap guidelines. Here, minimum delay, NDP and PDP are calculated and compared considering the optimized AR obtained in our work and the AR prescribed by IRDS 2018 roadmap[1]. It can be observed that there is an insignificant advantage in intermediate level interconnect performance but when it comes to global level, a substantial improvement is registered. This improvement in global metal line becomes more valuable as the effect of via is more dominant in global metal path. Our results show improved performance in $Fecl_3$ doped MLGNR interconnect for optimized value of AR as compared to IRDS roadmap 2015 prescribed AR. Also the improvement in FOM metric is significant indicating lower AR should be adopted considering overall performance and reliability.

Impact of contact resistance. Table 5 gives us an understanding of effect of contact resistance on numerically optimized AR and FOM. Here we have varied the contact resistance from 5 $K\Omega$ to 20 $K\Omega$[25]. As we can see, intermediate and global lines are not affected by it. But when it comes to local lines, increase in contact resistance leads to significant decrease in performance and increase in optimized AR. With a 75% increase in contact resistance, ~66%, ~5.5% and ~0.4% degradation in FOM of local, intermediate and global level $Fecl_3$ doped MLGNR

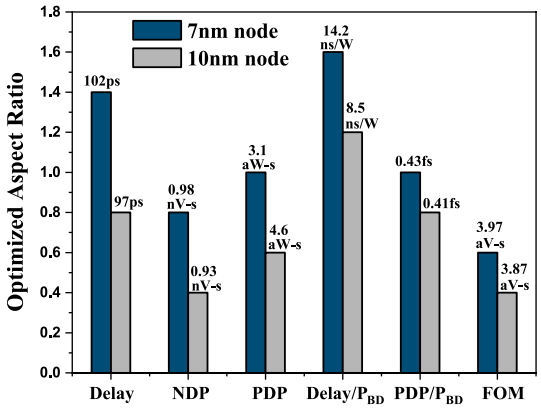

Figure 12. Impact of scaling on $Fecl_3$ doped MLGNR interconnect of length 10 μm (Intermediate level).

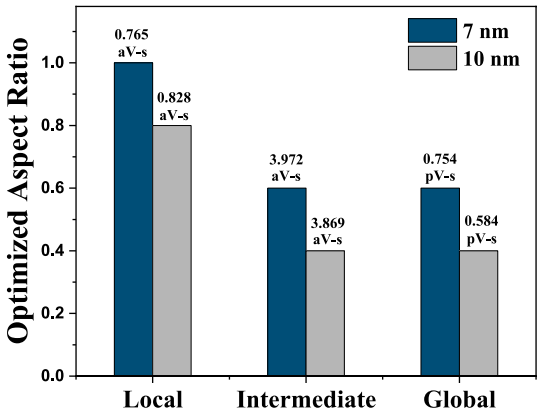

Figure 13. Impact of scaling on $Fecl_3$ doped MLGNR interconnect considering FOM at local, intermediate and global level.

interconnect, respectively is witnessed. Optimized *AR* also experiences an increase of ~26%, ~2.5% and ~1.8% in local, intermediate and global level, respectively. This infers that when the contact resistance increases, then in order to compensate the decrease in performance, *AR* can be increased (which will lead to increase in number of layers and thus decrease in contact resistance). So the performance of MLGNR interconnects will not improve beyond a certain limit.

Impact of scaling. The Impact of scaling (from 10 to 7 nm node) on optimized *AR* value of 10 μm long $Fecl_3$ doped MLGNR interconnect is shown in Fig. 12. Here, we can observe that scaling leads to an increase in optimized *AR* value along with degradation in performance and reliability for intermediate level interconnects following IRDS trends. When compared to copper with cobalt liner (considering IRDS suggested dimensions), Improvement in FOM of $Fecl_3$ doped MLGNR interconnect (calculated at optimized *AR*) is ~ 54%, ~ 93% and ~ 98% at local, intermediate and global levels, respectively for 7 *nm* and for 10 nm, it is ~ 43%, ~ 85% and ~ 91% at local, intermediate and global levels, respectively. The point to be noted here is that even though the performance of MLGNR degrades with scaling but when compared to copper, the performance increases with decreasing technology node. Figure 13 gives an understanding on effect of scaling on local, intermediate and global level $Fecl_3$ doped MLGNR interconnect considering the FOM. Scaling down from 10 *nm* to 7 *nm* node leads to degradation in FOM in $Fecl_3$ doped MLGNR interconnect by 2.6% and 22.6% in intermediate and global level, respectively even though we increase the *AR* from 0.4 to 0.6. But in case of local level, FOM is improved while scaling down by 8% if we increase the *AR* from 0.8 to 1.0. It is evident that with scaling there is a need of increase in *AR* in order to improve performance and reliability. The optimized (recommended) aspect ratio in this paper is less than 1.0. Although scaling down from 10 to 7 nm leads to an increase in optimized *AR*, but still it is lower as compared to IRDS suggestions ($AR > 2$). Jiang et al. have fabricated $Fecl_3$ doped MLGNR interconnect with aspect ratio of 0.4 and 0.6[10], which strengthens our claim from manufacturing point of view.

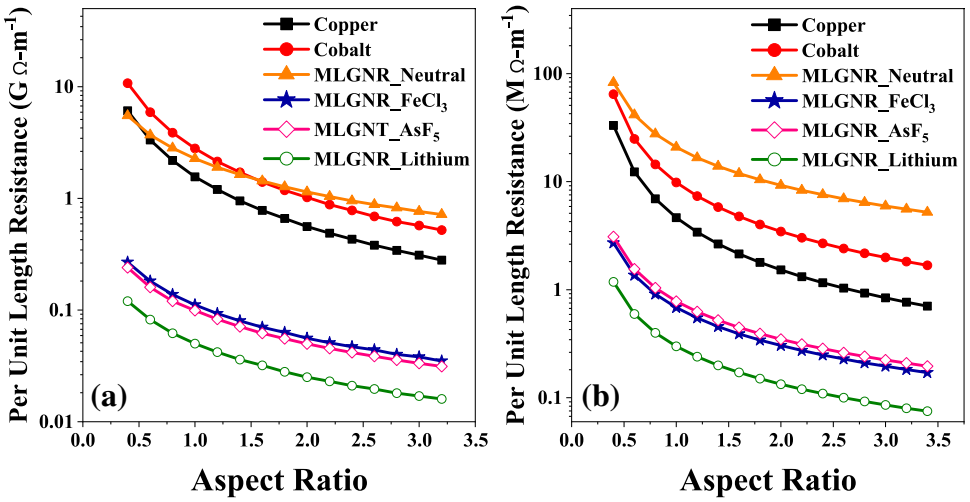

Figure 14. Per unit length electrical resistance for (**a**) intermediate level (L = 10 μm) and (**b**) global level (L = 1 mm) interconnects.

Formulation and methodology

This proposed methodology provides a detailed numerical dimensional optimization procedure and is applicable to any generic nano-interconnect system. This numerical methodology can avoid costly simulators set-ups and expensive fabrication procedures for providing the dimensional design guidelines to achieve such improvement in performance. Aspect ratio (AR) optimization serves to be an effective dimensional optimization technique for achieving superior performance and reliability metrics. Here, dependence of the RLC parameters on AR is discussed in order to establish relation between AR of interconnect and its delay, noise induced effects, power consumption and breakdown power.

From $N_{oL} = 1 + \lfloor \frac{t}{\delta} \rfloor$, we get $N_{oL} \propto AR$. And N_{ch} is a function of width of the interconnect. Therefore $R_{qtm} \propto (1/AR)$ as N_{ch} is constant and N_{oL} is a function of AR.

So, $R_{pul} \propto (1/AR)$ as shown in Fig. 14 because G_{pul} is a constant here as it is a function of width and N_{oL} is directly proportional to AR.

Similarly, C_{pul} is an increasing function of AR. C_{gnd}, C_{intra} and C_{inter} collectively adds to C_{elc}, where C_{inter} can be neglected[15]. They can be described as functions of AR as mentioned in Eqs. (7) and (8),

$$C_{gnd} \propto \left[\frac{1}{AR} + \left(\frac{1}{1+AR}\right)^{1.16} + 1\right] \tag{7}$$

$$C_{intra} \propto \left[A.R^{1.7}\left(\frac{1}{1+AR}\right)^{0.7} + 1\left(\frac{AR}{1+AR}\right)^{0.8} + 1\left(\frac{AR}{1+AR}\right)^{3.5}\right] \tag{8}$$

The dependence of C_{cup} on AR is described as,

$$C_{cup} \propto \left[AR^{1.09}\left(\frac{1}{1+AR}\right)^{0.09} + 1\left(\frac{AR}{1+AR}\right)^{1.18} + 1\right] \tag{9}$$

Noise and power consumption are a function of capacitance and hence they increase with increasing AR. However, delay is the dominating factor in NDP and PDP metrics. So, the expression of NDP and PDP leads to an optimized AR value.

Delay centric design. Propagation delay in an interconnect is basically a function of its RC product. With increasing AR, resistance decreases as shown in Fig. 14. But the capacitance increases, therefore an optimized value of AR is obtained for minimum delay point. The transfer function for the crosstalk delay or noise evaluation in the victim net will be denoted as $H(s)$. The second-order *Pade's* expansion of the transfer function is given by[16]:

$$H(s) \approx \frac{1}{1 + sb_1 + s^2 b_2} \tag{10}$$

The two poles of the transfer function are:

$$s_{1,2} = \frac{-b_1 \pm \sqrt{b_1^2 - 4b_2}}{2b_2} \tag{11}$$

where b_1 and b_2 are functions of R,L,Cs provided in[16]. They can be defined as a function of AR as follows,

$$b_1 \propto \frac{c_1}{AR} + c_2 + c_3 A.R \tag{12}$$

$$b_2 \propto \frac{a_1}{AR} + a_2 \tag{13}$$

The coefficients a_1, a_2, c_1, c_2, c_3 are described as:

$$a_1 = \frac{2R_dC_dC_lR_{qtm}\delta + LC_lL_{qtm}\delta + 2LC_lR_{qtm}^2C_{qtm}\delta}{N_{ch}w} + \frac{LC_l\delta R_{qtm}C_{qtm}}{G_{pul}w} + \frac{L^3C_lC_{qtm}N_{ch}\delta}{6G_{pul}^2w} \tag{14}$$

$$\begin{aligned} a_2 = {} & \frac{L^2L_{qtm}C_{qtm}}{2} + \frac{L^4C_{qtm}^2N_{ch}^2}{24.G_{pul}^2} + \frac{L^2R_d(C_d + C_l)C_{qtm}N_{ch}}{2G_{pul}} + \frac{L^3R_{qtm}C_{qtm}^2N_{ch}}{6G_{pul}} \\ & + LR_d(C_d + C_l)R_{qtm}C_{qtm} + \frac{L^3R_dC_{qtm}^2N_{ch}^2w}{6G_{pul}\delta} \end{aligned} \tag{15}$$

$$c_1 = \frac{2C_lR_{qtm}\delta}{N_{ch}w} + \frac{LC_l\delta}{G_{pul}w} \tag{16}$$

$$c_2 = LR_{qtm}C_{qtm} + \frac{L^2C_{qtm}N_{ch}}{2G_{pul}} + R_d(C_d + C_l) \tag{17}$$

$$c_3 = \frac{LR_dC_{qtm}N_{ch}w}{\delta} \tag{18}$$

The step response, which is the inverse Laplace transform of $\frac{1}{H(s)}$, is given by:

$$v(t) = V_0\left[\frac{1 - s_2}{s_2 - s_1}\exp(s_1t) + \frac{s_1}{s_2 - s_1}\exp(s_2t)\right] \tag{19}$$

The 50% propagation delay (τ) is given by[16],

$$0.5 - \frac{s_2}{s_2 - s_1}\exp(s_1\tau) + \frac{s_1s_2 - s_1}{\exp}(s_2\tau) = 0 \tag{20}$$

$$\tau = \frac{b_2}{b_1}\left[ln(0.5) + ln\left(\frac{b_1}{\sqrt{b_1^2 - 4b_2}} - 1\right) - ln\left(\frac{b_1}{\sqrt{b_1^2 - 4b_2}} + 1\right)\right] \tag{21}$$

Delay in terms of AR can be defined as:

$$\begin{aligned} \tau = {} & \left(\frac{a_1 + a_2.AR}{c_1 + c_2.AR + c_3.AR^2}\right)\left[ln(0.5) + ln\left(\frac{c_1 + c_2.AR + c_3.AR^2}{\sqrt{q_1 + q_2.AR + q_3.AR^2 + q_4.AR^3 + q_5.AR^4}} - 1\right)\right. \\ & \left. - ln\left(\frac{c_1 + c_2.AR + c_3.AR^2}{\sqrt{q_1 + q_2.AR + q_3.AR^2 + q_4.AR^3 + q_5.AR^4}} + 1\right)\right] \end{aligned} \tag{22}$$

Setting the derivative of delay with respect to AR to zero, we can obtain the optimized AR at which delay is minimum:

$$\frac{\partial\tau}{\partial AR} = 0 \tag{23}$$

$$\tau = u * v \implies \frac{\partial\tau}{\partial AR} = u * \frac{\partial v}{\partial AR} + v * \frac{\partial u}{\partial AR} = 0 \tag{24}$$

where u, v, $\frac{\partial u}{\partial AR}$ and $\frac{\partial v}{\partial AR}$ are described as:

$$u = \left(\frac{a_1 + a_2.AR}{c_1 + c_2.AR + c_3.AR^2}\right) \tag{25}$$

$$v = \left[ln(0.5) + ln\left(\frac{c_1 + c_2.AR + c_3.AR^2}{\sqrt{q_1 + q_2.AR + q_3.AR^2 + q_4.AR^3 + q_5.AR^4}} - 1\right) - ln\left(\frac{c_1 + c_2.AR + c_3.AR^2}{\sqrt{q_1 + q_2.AR + q_3.AR^2 + q_4.AR^3 + q_5.AR^4}} + 1\right)\right] \tag{26}$$

$$\frac{\partial u}{\partial AR} = \left[\frac{a_2(c_1 + c_2.AR + c_3.AR^2) - (a_1 + a_2.AR)(c_2 + 2c_3.AR)}{(c_1 + c_2.AR + c_3.AR^2)^2}\right] \tag{27}$$

$$\frac{\partial v}{\partial AR} = \left(\sqrt{q_1 + q_2.AR + q_3.AR^2 + q_4.AR^3 + q_5.AR^4}.(c_2 + 2c_3.AR)\right) - \left[(c_1 + c_2.AR + c_3.AR^2)\left(\frac{q_2 + 2q_3.AR + 3q_4.AR^2 + 4q_5.AR^3}{2\sqrt{q_1 + q_2.AR + q_3.AR^2 + q_4.AR^3 + q_5.AR^4}}\right)\right] \tag{28}$$

The constant coefficients q_1, q_2, q_3, q_4, q_5 are described here as follows,

$$q_1 = c_2^2 \tag{29}$$

$$q_2 = 2c_1c_2 - 4a_2 \tag{30}$$

$$q_3 = c_1^2 + 2c_2c_3 - 4a_1 \tag{31}$$

$$q_4 = 2c_1c_3 \tag{32}$$

$$q_5 = c_3^2 \tag{33}$$

Equation (23) can be numerically solved (here Newton Raphson is used) to obtain the optimized AR value at which delay is minimum. The initial guess value of AR was taken as 1 and the equation converged in less than 8 iterations giving optimized AR value of 1.418, 1.3329 and 1.213 for intermediate level AsF_5, $FeCl_3$ and Lithium doped MLGNR interconnects, respectively. Global level AsF_5, $FeCl_3$, and Lithium doped MLGNR interconnects optimized at AR of 1.06, 0.87 and 0.76, respectively.

FOM centric design. Similar approach is adopted to obtain the optimized AR at minimum FOM. We define Figure of Merit (FOM) as:

$$FOM = \tau * N_{peak} * Power/P_{BD} \tag{34}$$

where τ is given in equation (4), peak noise voltage (N_{peak}) is given by[17,18],

$$N_{peak} = \frac{C_{cup}}{s_2}\left(\frac{s_2}{s_1 - s_2}\right)\left[\left(\frac{s_1}{s_2}\right)^{\frac{-s_2}{(s_1 - s_2)}} - \left(\frac{s_1}{s_2}\right)^{\frac{-s_1}{(s_1 - s_2)}}\right] \tag{35}$$

The total power consumed in the interconnect is mainly because of the power consumed by driver and load buffers which is given by[19],

$$P_{total} = (N_{opt} + 2)(P_{switch} + P_{short} + P_{leak}) \tag{36}$$

where P_{switch}, P_{short} and P_{leak} are switching, short circuit and leakage power of a repeater, respectively. The definition of various parameters are specified in detail in[20]. Switching power dominates the equation thus is considered for further calculation for simplicity[19].

$$P_{\text{switching}} = S_f(S_r(c_d + c_l) + L_{rep}C_{pul})V_{DD}^2 f_{\text{clk}} \tag{37}$$

where V_{DD} is power supply voltage, f_{clk} is the clock frequency, L_{rep} is the inter repeater stage length, S_r is the ratio of buffer size to minimum sized buffer and S_f is the switching factor, which is the fraction of repeaters on a chip that are switched during an average clock cycle. It can be taken as 0.15[20]. P_{switch} as a function of AR can be defined as:

$$P_{switch} = \left[\frac{1}{AR} + \left(\frac{1}{1+AR}\right)^{1.16} + AR\left(\frac{AR}{1+AR}\right)^{0.7} + \left(\frac{AR}{1+AR}\right)^{0.8} + \left(\frac{AR}{1+AR}\right)^{3.5}\right] \left[\sqrt{AR^2 + AR(1+AR)^{1.16} + AR + (1+AR)^{0.8} + \left(\frac{(1+AR)}{AR}\right)^{0.7} + (1+AR)^{3.5} + 1}\right] \quad (38)$$

In order to have an understanding of reliability, we need to calculate and analyse the power consumed at the point where GNR interconnects breakdown and is given by[9,21],

$$P_{BD} = gL(T_B - T_A)\left[\frac{cosh(\frac{L}{2L_{TH}}) + gL_{TH}R_T sinh(\frac{L}{2L_{TH}})}{cosh(\frac{L}{2L_{TH}}) + gL_{TH}R_T sinh(\frac{L}{2L_{TH}}) - 1}\right] \quad (39)$$

where L_{TH} is defined as the thermal healing length of the metal line[21]. Breakdown power as a function of AR can be defined as:

$$P_{BD} \propto \left[\frac{cosh(\frac{1}{\sqrt{AR}}) + \sqrt{AR}sinh(\frac{1}{\sqrt{AR}})}{cosh(\frac{1}{\sqrt{AR}}) + \sqrt{AR}sinh(\frac{1}{\sqrt{AR}}) - 1}\right] \quad (40)$$

Setting the derivative of FOM with respect to AR to zero, we can obtain the optimized AR at which FOM is minimum:

$$\frac{\partial FOM}{\partial AR} = 0 = \frac{P_{BD}\left(\frac{\partial \tau}{\partial AR}N_{peak}P_{sw} + \frac{\partial N_{peak}}{\partial AR}\tau P_{sw} + \frac{\partial P_{sw}}{\partial AR}\tau N_{peak}\right) - \tau N_{peak}P_{switch}\frac{\partial P_{BD}}{\partial AR}}{(P_{BD})^2} \quad (41)$$

This equation is numerically solved (here Newton Raphson is used) to obtain optimized AR value which minimizes the FOM. Here the initial guess value of AR was taken as 0.5 and the equation converged in 11 iterations giving optimized AR value of 0.633, 0.61 and 0.583 for intermediate level AsF_5, $FeCl_3$, and Lithium doped MLGNR interconnects, respectively. Global level AsF_5, $FeCl_3$, and Lithium doped MLGNR interconnects optimized at AR of 0.585, 0.579 and 0.481, respectively. And local level AsF_5, $FeCl_3$, and Lithium doped MLGNR interconnects optimized at AR of 1.08, 0.987 and 0.623, respectively.

Conclusion

This work focuses on numerically determining optimum aspect ratio in order to improve performance, reliability and minimize noise effects and power consumption. This approach will be extremely useful to industry for selection of AR of interconnects as it is a non-SPICE method. Our approach provides a detailed guideline for the Aspect ratio optimization and reduces fabricational cost to achieve high performance and reliability MLGNR interconnects by reducing iterations during fabrication process for achieving desired performance. The optimized AR of AsF_5, $FeCl_3$, Lithium doped MLGNR interconnects by minimizing delay is obtained at 1.4, 1.4 and 1.2 for intermediate level and 1.0, 1.0 and 0.8 for global level interconnects, respectively. Intermediate level, AsF_5, $FeCl_3$, Lithium doped MLGNR interconnects have an optimized AR of 1.0, 1.0 and 0.6 and global levels have an optimized AR of 0.8 at which minimum PDP is registered. PDP/P_{BD} ratio is minimized at an aspect ratio of 1.0, 1.0 and 0.6, respectively. The FOM is minimized at an aspect ratio of 1.0, 1.0 and 0.6 for local level and 0.6, 0.6 and 0.5 for intermediate and global level AsF_5, $FeCl_3$, Lithium doped MLGNR interconnects, respectively. Increase in contact resistance leads to significant decrease in performance and increase in optimized AR of local $FeCl_3$ doped MLGNR interconnect. As we scale down, the optimized AR increases with decrease in performance and reliability for intermediate and global levels. But while scaling down, increase in optimized AR leads to better FOM in local level doped MLGNR interconnect. When compared to copper (considering IRDS suggested dimensions), Improvement in FOM of $FeCl_3$ doped MLGNR interconnect (calculated at optimized AR) is $\sim$ 54%, $\sim$ 93% and $\sim$ 98% at local, intermediate and global levels, respectively for 7 nm and for 10 nm, it is $\sim$ 43%, $\sim$ 85% and $\sim$ 91% at local, intermediate and global levels, respectively. When compared to IRDS suggestion, the estimated delay in intermediate level $FeCl_3$ doped MLGNR interconnect is improved by $\sim$2%, NDP by 44%, PDP by $\sim$9%, the PDP/P_{BD} is improved by $\sim$6% and FOM by $\sim$49%. Similarly in global level, delay, NDP, PDP, PDP/P_{BD} and FOM is improved by 25%, 50%, 48%, 48% and 68%, respectively. This study has systematically formulated a numerical optimization methodology and guideline for selecting an optimized aspect ratio to achieve improved performance and reliability for doped MLGNR interconnects.

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All the authors contributed equally in the manuscript.

Competing interests
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