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Author Correction: A pseudo-softmax function for hardware-based high speed image classification

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The original version of this Article contained an error in Figure 3 where panels (b) and (c) were incorrectly captured. The original Figure 3 and accompanying legend appear below.

The original Article has been corrected.

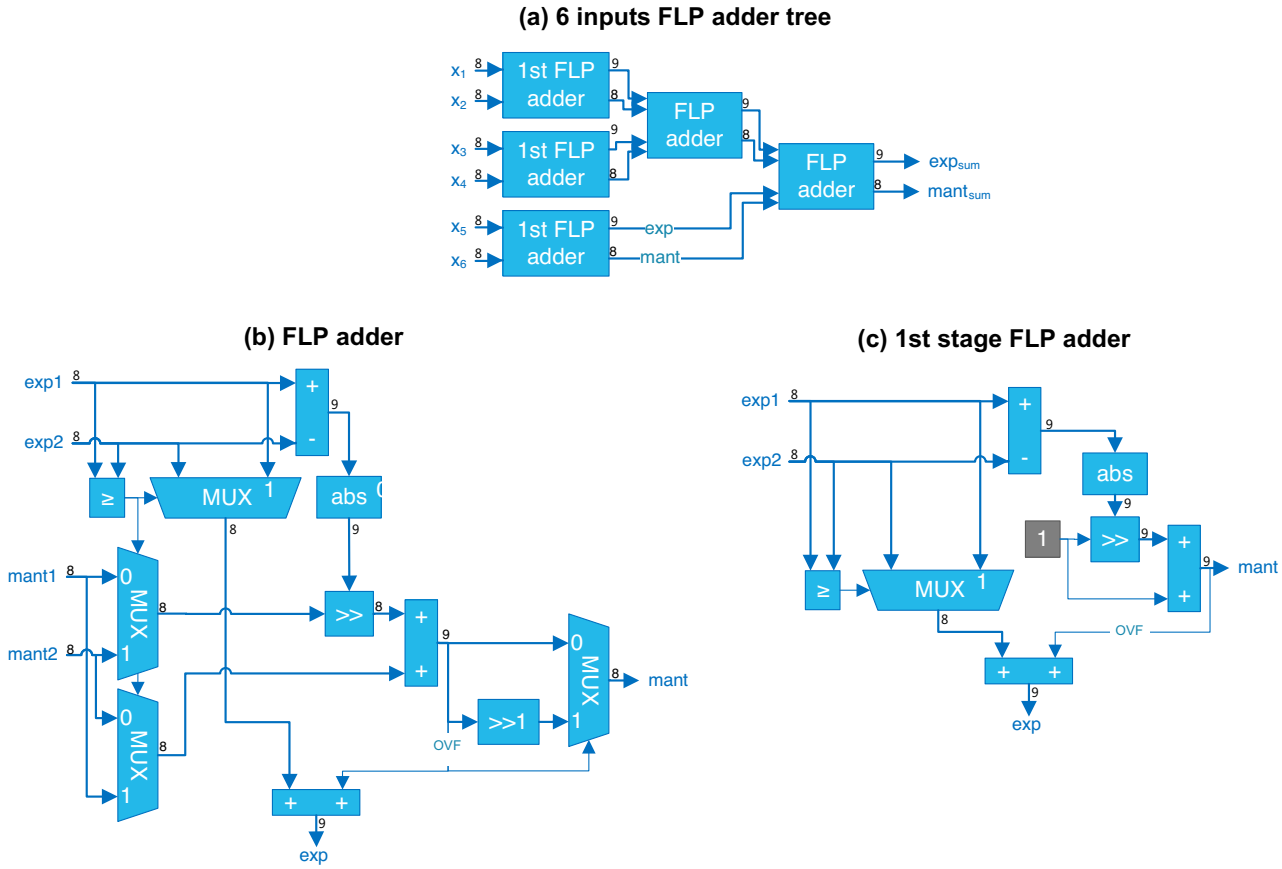

Figure 3. (**a**) Example of 6 8-bit inputs FLP adder tree. (**b**) Architecture of a FLP adder. (**c**) Architecture of the optimized FLP adder used in the first level of the tree.