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Dicing of composite substrate for thin film AlGaInP power LEDs by wet etching

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In this paper, thin film AlGaInP LED chips with a 50 µm thick composite metal substrate (Copper-Invar-Copper; CIC) were obtained by the wet etching process. The pattern of the substrate was done by the backside of the AlGaInP LED/CIC. There was no delamination or cracking phenomenon of the LED epilayer which often occurs by laser or mechanical dicing. The chip area was 1140 µm × 1140 µm and the channel length was 360 µm. The structure of the CIC substrate was a sandwich structure and consisted of Cu as the top and bottom layers, with a thickness of 10 µm, respectively. The middle layer was Invar with a 30% to 70% ratio of Ni and Fe and a total thickness of 30 µm. The chip pattern was successfully obtained by the wet etching process. Concerning the device performance after etching, high-performance LED/CIC chips were obtained. They had a low leakage current, high output power and a low red shift phenomenon as operated at a high injected current. After the development and fabrication of the copper-based composite substrate for N-side up thin-film AlGaInP LED/CIC chips could be diced by wet etching. The superiority of wet etching process for the AlGaInP LED/CIC chips is over that of chips obtained by mechanical or laser dicing.

It is well known that thin film AlGaInP with a mirror substrate created by epilayer transferring can offer the maximum output power for power red light-emitting diode (LED) applications due to the lattice-matching GaAs substrate being an absorbing substrate[1,2]. $(Al_xGa_{1-x})_{0.5}In_{0.5}P$ based red LEDs whose internal quantum efficiencies (IQE) exceed 90% because of epilayer grown on precisely lattice-matched GaAs substrate by MOCVD without the generation of redundance displacement[3–7]. In general, AlGaInP LED epilayers have always been transferred to a CuW substrate or Si permanent substrates with a mirror structure. Nevertheless, a CuW metal substrate is expensive, it is difficult to achieve a thickness below 150 µm, and it is hard to dice by dicing saw and laser. Concerning the Si permanent substrate, it is necessary to perform more processes, such as lapping Si substrate to a 150-µm thickness, depositing the Al metal, and performing thermal annealing (to obtain the Ohmic contact property between the Al metal and Si)[8,9]. If the thickness of Si substrate is too thin (< 150 µm), the cracking phenomenon of the LED epilayer could often occur during the processing. For these kinds of substrates, it is required to dice the wafers into chips using a saw or laser-based dicing[10–14]. Although the diamond saw and laser dicing processes are mature, they require extra time and can easily induce damage, e.g. epilayer delamination or chip cracking. Damage to the LED chips during laser and saw dicing is a serious issue. This technology faces a number of challenges to meet demands for next-generation device manufacturing processes, including chipping and cracking of the dice, limitations in street width, limitations in die shape, mechanical stress of the dies, and limitations in processed materials[15,16]. To overcome these problems, wet chemical etching dicing, which is a novel substrate level dicing method for low cost and high-performance LEDs, was proposed. Wet etching has the potential to dice a whole substrate with thicknesses less than 100 µm. Correspondently, crack could be induced if the Si substrate was thinned less than 150 µm. In contrast, no physical damage to the LED chips during this process (such as cracking) is likely to occur[17–21]. Therefore, the strength of LED chip with CIC substrate can be improved as compared to that of LED with thin Si substrate resulting from saw or laser dicing[22,23]. Concerning the CIC substrate, mechanical strength has been already proposed and fabricated for thin film AlGaInP LED applications in our recent study[8,24]. In this study, the thin film AlGaInP epilayer was successfully transferred to a CIC substrate with a 50-µm thickness using wafer bonding and epilayer transferring technologies[3,25,26]. Thin film AlGaInP LED chips with a composite metal substrate were developed and obtained high-performance LED/CIC chips using the wet etching process. The substrate pattern was performed on the backside of AlGaInP LED/

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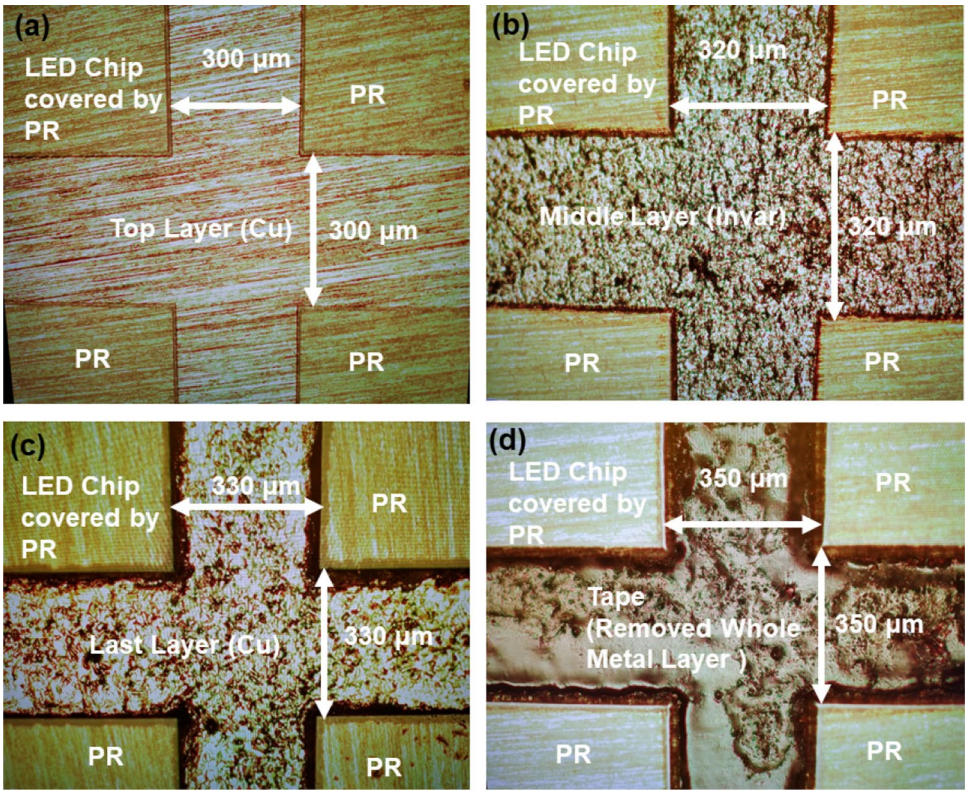

Figure 1. Channel variations of the chip pattern during the dicing process as measured by optical microscope (OM): (**a**) top layer (Cu); (**b**) middle layer (Invar); (**c**) bottom layer (Cu); (**d**) removed whole layer.

CIC chips with a 1200-μm^2 chip size and a 300-μm channel width. Moreover, the chip pattern was successfully obtained. The results indicated that dicing could be achieved with low leakage current, high output power, and a low red shift phenomenon by the wet etching process.

Results and discussion

It is well known that most chemical etching processes for metal are a type of isotropic etching, and that inside edge etching can exist. To evaluate the existence of side etching, the etching channel was measured before and after the etching process. Because the CIC substrate was a composite metal substrate made of Cu, Invar and Cu layers, the dicing was processed in three steps. Every layer was etched by the chemical solution. It is worthy to mention that both the CuR-8000S and NiE-7520 chemical solutions were used to etch the Cu and Invar layers, respectively. Both presented high metal etching selectivity because the top and bottom layer (Cu) were etched away from the CuR-8000S. Moreover, etching of the top layer (Cu) stopped when the middle layer (Invar) was exposed. The invar layer was removed from the NiE-7520 and the etching stopped when the bottom layer (Cu) was exposed. Figure 1 shows the channel variation of the chip pattern before and after CIC etching, as examined by an optical microscope (OM). As shown in Fig. 1a, the channel dimension defined by photolithography was 300 um. After removing the 10-um thickness of the top layer (Cu) in the channel region by a chemical solution (CuR-8000S) to expose the Invar layer, it was found that the size of the channel became wider by about 20 um, from 300 to 320 um, as shown in Fig. 1b. Approximately seven to eight minutes were needed to etch the top Cu layer. After removing the 30-um thickness of the Invar layer by NiE-7520 to expose the last Cu layer, the channel dimension further increased from 320 to 330 um, as shown in Fig. 1c. The etching time for this step was about 9 to 10 min. Figure 1d shows the OM image after removing the last Cu layer in the channel region. The final dimension of the channel was 350 um. It is worthy to mention that all chips were still attached on the tape. Moreover, the last etched layer took less time (about 4–5 min) and had a high etching rate as compared to the top layer. This resulted in the etching area becoming larger than that of the first Cu layer.

The chip dimensions before and after the wet etching process from the backside of the CIC metal substrate was examined by OM and SEM, as shown in Fig. 2. Before etching, the epilayer with the CIC metal substrate was face down and attached to the tape. A double side aligner photolithography machine was used to define a chip area of 1200 um × 1200 um, which was protected by PR, shown in Fig. 2a. After etching the first Cu layer, the chip dimension was measured by SEM and became 1180 um × 1180 um with a channel width of 320 um, as shown in Fig. 2b. This measurement agreed with that measured by OM, shown in Fig. 1b. Concerning the Invar etching, the size of the chips was further reduced by about 10 μm from each side and was reciprocal with the channel width. Figure 2c presents the top-view SEM image of the last Cu layer in the channel region, in which the dimension of the chip was 1170 um × 1170 um. For discrete dicing chips, the last Cu layer was needed to etch

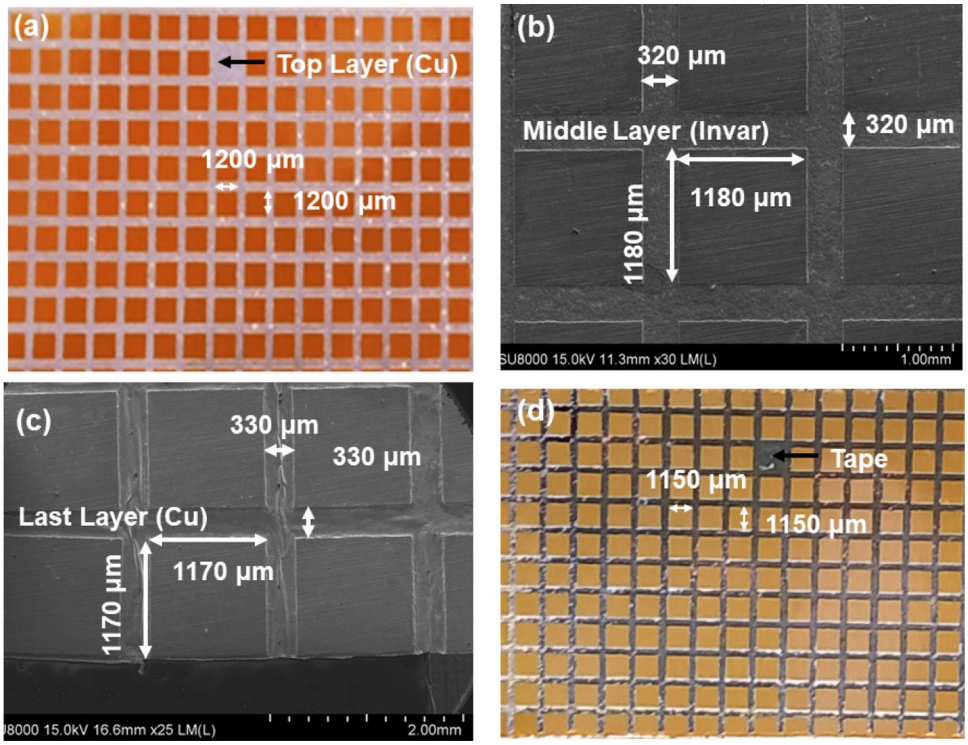

Figure 2. Chip dimensions before and after wet etching from the back side of the CIC for dicing: (**a**) OM image of the chip pattern before the etching process; (**b**) SEM image of the middle layer (Invar); (**c**) SEM image of the last layer (Cu); (**d**) OM image of the diced chip.

Layers	Thickness of layer (µm)	Chip size after etching layers (µm)	Channel width after etching layers (µm)	Etching time (min.)	Etching rate (µm/min)	Side edge etching (µm)
Cu	10	1180	320	7–8	1.43–1.25	20/side
Invar	30	1170	330	9–10	3.3–3	10/side
Cu	10	1150	350	4–5	2.5–2	20/side

Table 1. Summary of the etching layers during the dicing process.

away. Figure 2d shows the chips pattern and OM image after removing the last layer (Cu) from the channel region. The size of the chips became 1150 um × 1150 um, after which the LEDs took on a chip form. The dimensions of LED chips changed from 1200 um × 1200 um to 1150 um × 1150 um. Noted that the etching yield is above 99%. The 1% loss was resulted from chips peel off from the tape during etching. A summary of the etching layer parameters for dicing by a chemical solution are shown in Table 1. The etching rate of first Cu is about 1.43–1.25 µm /min. Then the etching rate of Invar is about 3.3–3 µm/min. The etching rate of the last Cu layer is about 2.5–2 µm/min. It is worthy to mention that the lower etch rate for the first Cu layer than that of the second Cu layer, it could be due to the surface being oxidized for the first layer. After the Invar etched away, the Cu is fresh and easily etch by chemical.

Concerning the side edge of the diced chip created by wet etching, it was observed that the chip size was reduced by about 50 µm from each side. In order to avoid the inside edge cutting the LED epilayer from the front side, the dimensions of the chip patterns were modified using the channel length from the backside of the CIC substrate. Chip patterns sized 1200 um × 1200 um with a channel length of 300 um could be matched to the front side of the LED epilayer sized 1140 um × 1140 um with a channel length of 360 µm during the dicing process. Details of the dimensions of the LED chips from the front side and those of the dicing chips from the backside of the CIC substrate are shown in Table 2.

Figure 3 presents the typical single chip thin-film AlGaInP LED on a CIC metal substrate. The dimensions of the LED epilayer were 1140 um × 1140 um and 1150 um × 1150 um for the diced chip. It is worthy to mention that the side wall of the LED and CIC substrate were very clean. There were no chipping or cracking problems which exist in dicing saw and ablation phenomenon resulting from the laser dicing. After dicing of the LED/CIC, the most important issue was the LED performance. The reverse and forward currents of the LED/CIC chips as a function of voltage are shown in Fig. 4a,b, respectively. The inset of Fig. 4b shows the turning on of the

Patterns	Chip size	Channel width (μm)
LED chips from the front side	1140 μm × 1140 μm	360
Dicing chips from the backside	1200 μm × 1200 μm	300

Table 2. Dimensions of the LED chips from the front side and dicing patterns from the backside of the CIC substrate.

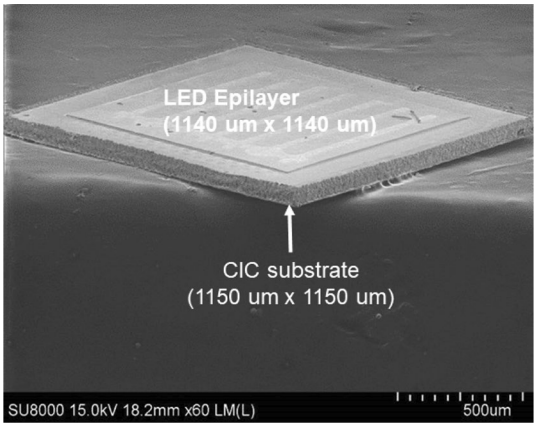

Figure 3. Typical single chip thin film AlGaInP LED on a CIC metal substrate.

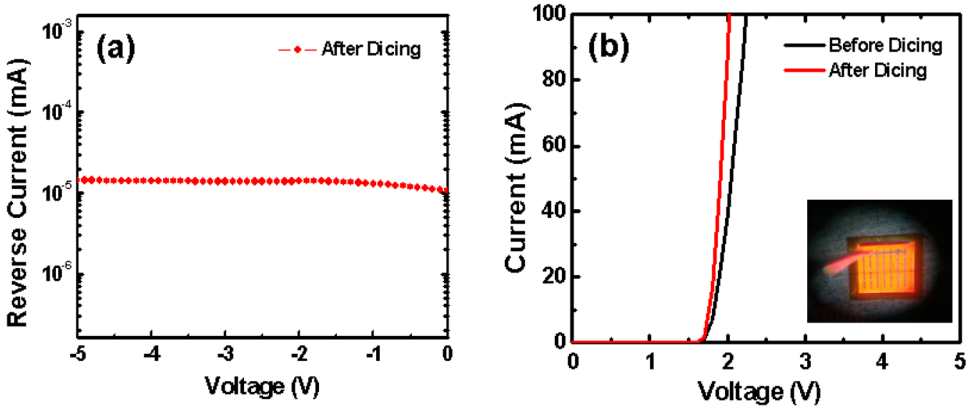

Figure 4. (**a**) Reverse I–V curves; (**b**) I–V characteristics of the LED/CIC chips before and after dicing. The inset shows the lightening picture of the LED/CIC chips after dicing.

LED/CIC chips after dicing. A low leakage current of about 1.5×10^{-8} A was obtained when the reverse voltage was – 5 V. The forward voltages of the LED/CIC chips before chemical dicing were about 1.91 V and 2.81 V with an injection current of 20 mA and 350 mA, respectively. It is worthy to mention that although picosecond and femtosecond lasers are mature and remain a good candidate for dicing device chips, the leakage of LEDs is easily created by the metal splashing during the dicing. Furthermore, the CIC metal is easily melted back during dicing, especial for the small dicing channel. As concerning these problem, they did not occur for the chemical dicing.

After chemical dicing, the forward voltages of the LED/CIC chips were about 1.82 V and 2.34 V with an injection current of 20 mA and 350 mA, respectively. It was noted that the LED/CIC chips presented a lower forward voltage (1.82 V) due to the low electrical resistance and thickness of the substrate for the discrete chip[24]. Concerning the optical performance, the output power presented a linear relation with a current injection of 0 to 700 mA, as shown in Fig. 5a. Here, the output power became saturated as the injected current increased to 700 mA, due to the LED/CIC chips remaining packaged.

Moreover, the chips offered good thermal dissipation in the wavelength variation[8,24]. The thermal dissipation was related to the thickness of the substrates, meaning that a higher thermal dissipation required less thickness[8]. The wavelength of the LED/CIC chips changed from 627.9 to 633.13 nm as the current increased from 100 to

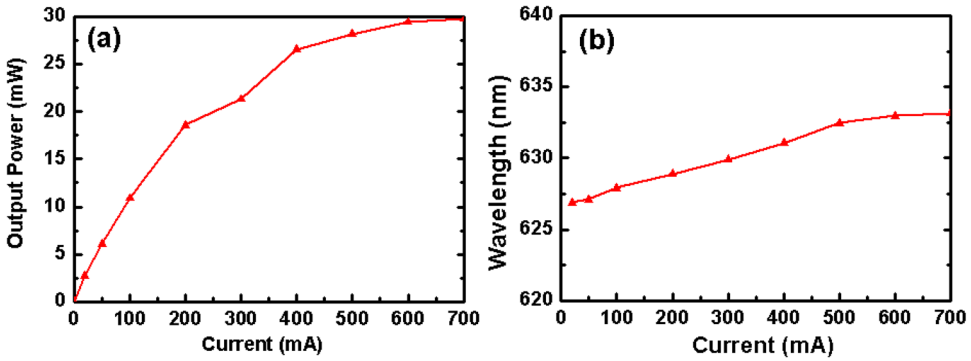

Figure 5. (**a**) Output power; (**b**) wavelength as a function of current for the LED/CIC chips after dicing.

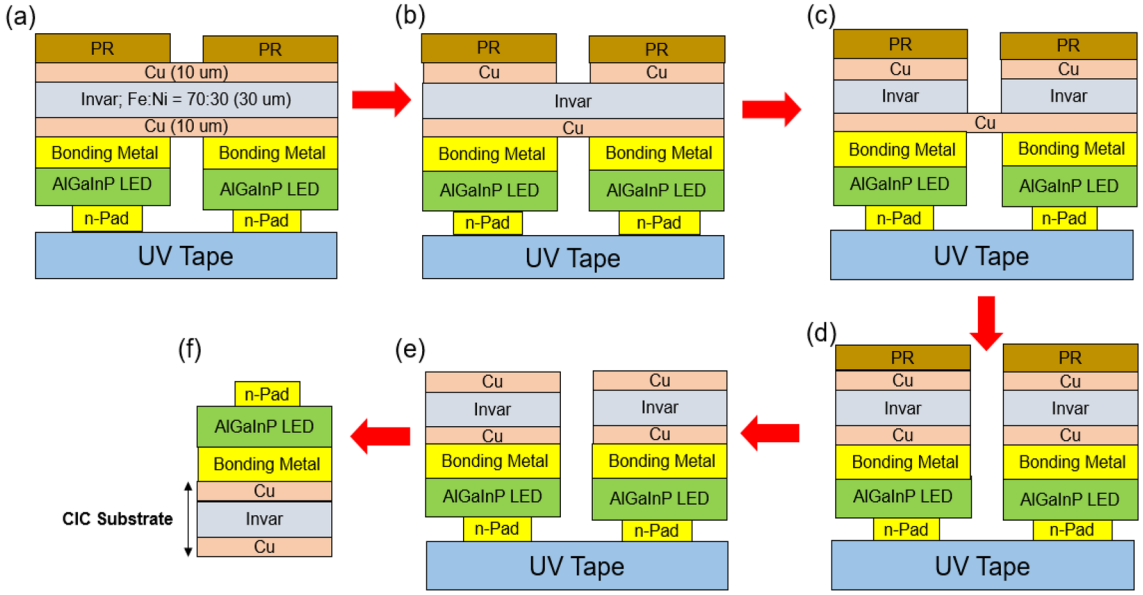

Figure 6. Process flow for the dicing of LED/CIC chips from the back side of the CIC.

700 mA, as shown in Fig. 5b. These results suggested that the dicing of LED/CIC chips by the wet etching process could offer good electrical and optical properties.

Conclusion

In this paper, dicing of LED/CIC chips was obtained by the wet etching process. The pattern of the substrate was made on the backside of the CIC substrate and compared with the front side of the AlGaInP LED chip pattern due to the side edge etching that occurred during the etching process. Due to its low cost, thickness, high thermal conductivity and ease of dicing, CIC substrate have the potential and mechanical strength to replace CuW and Si permanent substrates. Concerning the device performance, LED/CIC chips presented low leakage current, high output power and a low red shift phenomenon as they operated at a high injected current. The results suggested that the CIC substrate can be diced by the wet etching process without any physical damage or epilayer cracking, indicating that the wet etching process can be used in place of saw or laser dicing and extended for thin film micro LED applications, thereby meeting demands for next-generation device manufacturing processes.

Methods

The epilayer structure and fabrication process for thin film AlGaInP LED applications were proposed in our previous study[8,24,27]. Here, this study focused on the dicing of chips from the backside of the substrate by wet etching. Figure 6 shows the complete process flow chart for the dicing of the LED/CIC chips from the backside. First, the AlGaInP/LED chips on the CIC substrate was cleaned with acetone (ACE) and Isopropyl alcohol (IPA) to remove the impurities, then the pattern was created on the backside using a conventional lithography technology. After, the wafer was attached to UV tape from the front side to protect the AlGaInP/LED chips during the chemical dicing process, as shown in step (a). The 10-μm thick top layer (Cu) was removed from the Copper etcher chemical solution (CuR-8000S) in step (b), and the 30-μm thick middle layer (Invar) was removed

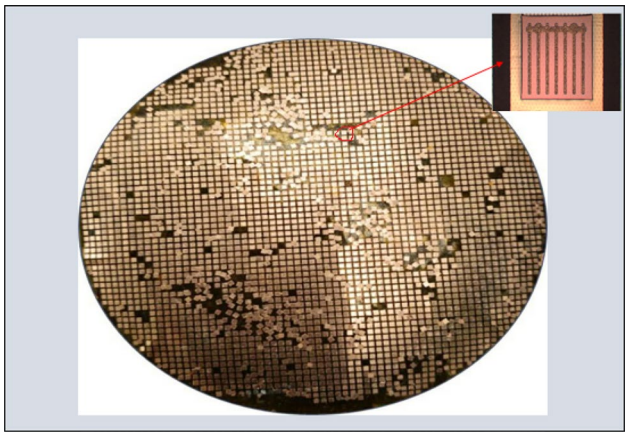

Figure 7. Diced LED/CIC chips from the back side of the CIC by the wet etching process.

from the Nickel etcher chemical solution (NiE-7520) in step (c). All etching process was carried out at room temperature and chemical was no stirring. Between the step (b) and step (c), wafer was rinsed by DI water. For the last Copper layer, the etching process was the same with the step b. After removing the entire CIC layers in the channel region, the AlGaInP/LED chips were diced from the backside of the substrate, as shown in Fig. 7. It can be find that the yield is about 90%. The 10% loss was resulted from the chips peeling off from the tape after the metal totally dicing. It can be overcome to find the high adhesive tape to increase the yield.

In this study, the dicing pattern from the backside was evaluated using the LED chip pattern from the front side of the substrate due to the existence of side edge etching during the etching process. LED/CIC chips could be successfully diced by the wet etching process without any physical damage or epilayer cracking, which can occur during saw or laser-based dicing. Wet etching dicing has the potential to dice substrates with thickness greater than 100 μm.

After completion of the whole process for the dicing of LED/CIC chips from the backside, the electrical and optical characteristics of the diced LED/CIC chips were measured using a multi-function power meter (KEITHLEY 2400) and an integrating sphere. The data for all measured LED/CIC chips were averaged from 20 different samples.

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References

1. Schnitzer, I., Yablonovitch, E., Caneau, C. & Gmitter, T. J. Ultrahigh spontaneous emission quantum efficiency 99.7% internally and 72% externally from AlGaAs/GaAs/AlGaAs double hetero-structures. *Appl. Phys. Lett.* **62**(2), 131–133 (1993).
2. Lee, H. K., Kim, M. S. & Yu, J. S. Improved device performance of AlGaInP-based vertical light-emitting diodes with low-n ATO antireflective coating layer. *Microelectron. Eng.* **104**, 29–32 (2013).
3. Horng, R. H. *et al.* Development and fabrication of AlGaInP-based flip-chip micro-LEDs. *IEEE J. Electron. Device* **6**, 475–479 (2018).
4. Schnitzer, I., Yablonovitch, E., Caneau, C. & Gmitter, T. J. Ultrahigh spontaneous emission quantum efficiency 99.7% internally and 72% externally from AlGaAs/ GaAs/AlGaAs double hetero-structures. *Appl. Phys. Lett.* **62**(2), 131–133 (1993).
5. Kuo, C. P. *et al.* High performance AlGaInP visible light-emitting diodes. *Appl. Phys. Lett.* **57**(27), 2937–2939 (1990).
6. Sugawara, H., Ishikawa, M. & Hatakoshi, G. High-efficiency InGaAlP/GaAs visible light-emitting diodes. *Appl. Phys. Lett.* **58**(10), 1010–1012 (1991).
7. Gessmann, T. & Schubert, E. F. High-efficiency AlGaInP light emitting diodes for solid-state lighting applications. *J. Appl. Phys.* **95**(5), 2203–2216 (2004).
8. Sinha, S., Feng, H. A., Chung, C. Y., Tu, C. W. & Horng, R. H. Comparison of properties of thin film AlGaInP LEDs with composite metal and Si substrates. *ECS J. Solid State Sci. Technol.* **9**(1), 015015. https://doi.org/10.1149/2.0342001JSS (2020).
9. Chen, S., Tsai, C. Z., Wu, E., Shih, I. G. & Chen, Y. N. Study on the effects of wafer thinning and dicing on chip strength. *IEEE Trans. Adv. Packag.* **29**(1), 149–157. https://doi.org/10.1109/TADVP.2005.849552 (2006).
10. Kommera, S. Fabrication of precise die edges for micro-optical and MEMS applications. *IEEE Trans. Adv. Packag.* **30**(4), 725–730. https://doi.org/10.1109/TADVP.2007.908025 (2007).
11. Cheung, A. T. Dicing advanced materials for microelectronics. In Proceedings International Symposium Exhibition Advanced Packaging Materials Processes, 149–152. https://doi.org/10.1109/ISAPM.2005.1432066 (2005).
12. Efrat, U. Optimizing the wafer dicing process. In IEEE/CHMT European International Electronic Manufacturing Technology Symposium, 245–253. https://doi.org/10.1109/IEMT.1993.398195 (1993).
13. McCabe, P. Sawing silicon. *Adv. Pack.* **14**(3), 26–27 (2005).
14. Adachi, T., Matsumaru, K. & Ishizaki, K. Fabrication of highly efficient dicing blade for cutting Al2O3-TiC composite. *J. Ceram. Soc. Jpn.* **114**(1320), 336–340 (2006).
15. Danyluk, S. Four point probe resistivity measurements of dicing damage In (100) And (1 I 1) single crystal silicon wafers. *J. Mater. Sci.* **25**, 4892 (1990).
16. Chen, S., Tsai, C. Z., Wu, E., Shih, I. G. & Chen, Y. N. Study on the effects of wafer thinning and dicing on chip strength. *IEEE Trans. Adv. Pack.* **29**, 149–157 (2006).
17. Li, X. Metal-assisted chemical etching in HF/H2O2 produces porous silicon. *Appl. Phys. Lett.* **77**, 2572 (2000).
18. Huang, Z. Metal-assisted chemical etching of silicon: A review. *Adv. Mater.* **23**, 285–308 (2011).

19. Li, L. Uniform vertical trench etching on silicon with high aspect ratio by metal-assisted chemical etching using nanoporous catalysts. *ACS Appl. Mater. Interfaces* **6**, 575–584 (2014).
20. Chartier, C. Metal-assisted chemical etching of silicon in HF–H2O2. *Electrochim. Acta* **53**, 5509 (2008).
21. Peng, K. Motility of metal nanoparticles in silicon and induced anisotropic silicon etching. *Adv. Funct. Mater* **18**, 3026–3035 (2008).
22. Asano, Y., Matsuo, K., Ito, H., Higuchi, K., Shimokawa, K. & Sato, T. A novel wafer dicing method using metal-assisted chemical etching, In IEEE 65th Electronic Components and Technology Conference (ECTC), 853–858. https://doi.org/10.1109/ECTC.2015.7159692 (2015).
23. Lianto, P. Vertical etching with isolated catalysts in metal-assisted chemical etching of silicon. *Nanoscale* **4**, 7532–7539 (2012).
24. Horng, R. H. *et al.* Composite metal substrate for thin film AlGaInP LED applications. *Opt. Express* **27**, A397–A403 (2019).
25. Tseng, M. C. *et al.* P-side-up thin-film AlGaInP-based light emitting diodes with direct ohmic contact of an ITO layer with a GaP window layer. *Opt. Express* **22**(S7), A1862–A1867 (2014).
26. Zuo, Z. *et al.* Ultra bright AlGaInP light emitting diodes with pyramidally patterned GaP spreading layer. *Appl. Phys. Lett.* **99**(12), 121104 (2011).
27. Horng, R. H., Lee, C. E., Kung, C. Y., Huang, S. H. & Wuu, D. S. High-power AlGaInP light-emitting diodes with patterned copper substrates by electroplating. *Jpn. J. Appl. Phys.* **43**(4B), L576–L578 (2004).

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Author contributions

R.H.H. conceived and designed the experiments. H.A.F. and C.W.T. provided the CIC metal and etcing process. S.S. and F.G.T. designed experiments, analyzed, verified the data. R.H.H. and S.S. wrote the main manuscript. All authors read and approved the final version of the manuscript to be submitted.

Competing interests

The authors declare no competing interests.

Additional information

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