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A quantitative approach for trap analysis between $Al_{0.25}Ga_{0.75}N$ and GaN in high electron mobility transistors

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The characteristics of traps between the $Al_{0.25}Ga_{0.75}N$ barrier and the GaN channel layer in a high-electron-mobility-transistors (HEMTs) were investigated. The interface traps at the $Al_{0.25}Ga_{0.75}N$/GaN interface as well as the border traps were experimentally analyzed because the $Al_{0.25}Ga_{0.75}N$ barrier layer functions as a dielectric owing to its high dielectric constant. The interface trap density D_{it} and border trap density N_{bt} were extracted from a long-channel field-effect transistor (FET), conventionally known as a FATFET structure, via frequency-dependent capacitance–voltage (C–V) and conductance–voltage (G–V) measurements. The minimum D_{it} value extracted by the conventional conductance method was 2.5×10^{12} $cm^{-2} \cdot eV^{-1}$, which agreed well with the actual transistor subthreshold swing of around 142 $mV \cdot dec^{-1}$. The border trap density N_{bt} was also extracted from the frequency-dependent C–V characteristics using the distributed circuit model, and the extracted value was 1.5×10^{19} $cm^{-3} \cdot eV^{-1}$. Low-frequency (1/*f*) noise measurement provided a clearer picture of the trapping–detrapping phenomena in the $Al_{0.25}Ga_{0.75}N$ layer. The value of the border trap density extracted using the carrier-number-fluctuation (CNF) model was 1.3×10^{19} $cm^{-3} \cdot eV^{-1}$, which is of a similar level to the extracted value from the distributed circuit model.

Recently, GaN-based high-electron-mobility-transistors (HEMTs) have gained considerable attention because of their outstanding material properties and device performance, including power and RF applications up to the sub-terahertz regime[1–3]. These advantageous properties and performance are attributable mainly to the high quality of the epitaxial layer comprising the $Al_xGa_{1-x}N$ barrier and the GaN channel layer, which causes the formation of two-dimensional electron gas (2DEG) on top of Si, Sapphire, and SiC substrates[4,5]. The quality of the $Al_xGa_{1-x}N$/GaN interface is crucial to the improvement of the carrier transport in the channel during device operation[6,7]. In addition to the performance of AlGaN/GaN HEMTs, their reliability is an ongoing topic of research that requires examination of a variety of factors. Most of the reliability issues are related to the AlGaN layer, which is the surface layer in the gate-to-drain access region and contains deep-level traps[8]. These issues become more critical in deeply scaled transistors for high-frequency applications. Most previous research on the reliability of AlGaN/GaN HEMTs focused mainly on the surface traps in the access region and on their passivation using dielectric materials[9,10]. Plasma treatment was also utilized to decrease these deep-level traps in the AlGaN barrier layer[11]. Characterization of interface traps and deep-level border traps is important for improving the 2DEG carrier concentration and reducing interface roughness scattering to enhance mobility, with the eventual aim of improving device reliability and performance. Previous studies focused on the characterization of traps formed at the insulator/AlGaN interface in a metal–oxide–semiconductor field-effect transistor (MOSFET) structure via frequency-dependent capacitance–voltage (C–V) and conductance–voltage (G–V) measurements[9,10]. Some studies even discussed the interface trap states in AlGaN/GaN Schottky-HEMT as well as MOS-HEMT but their results conclude that the trap states are mainly located at the surface interface within

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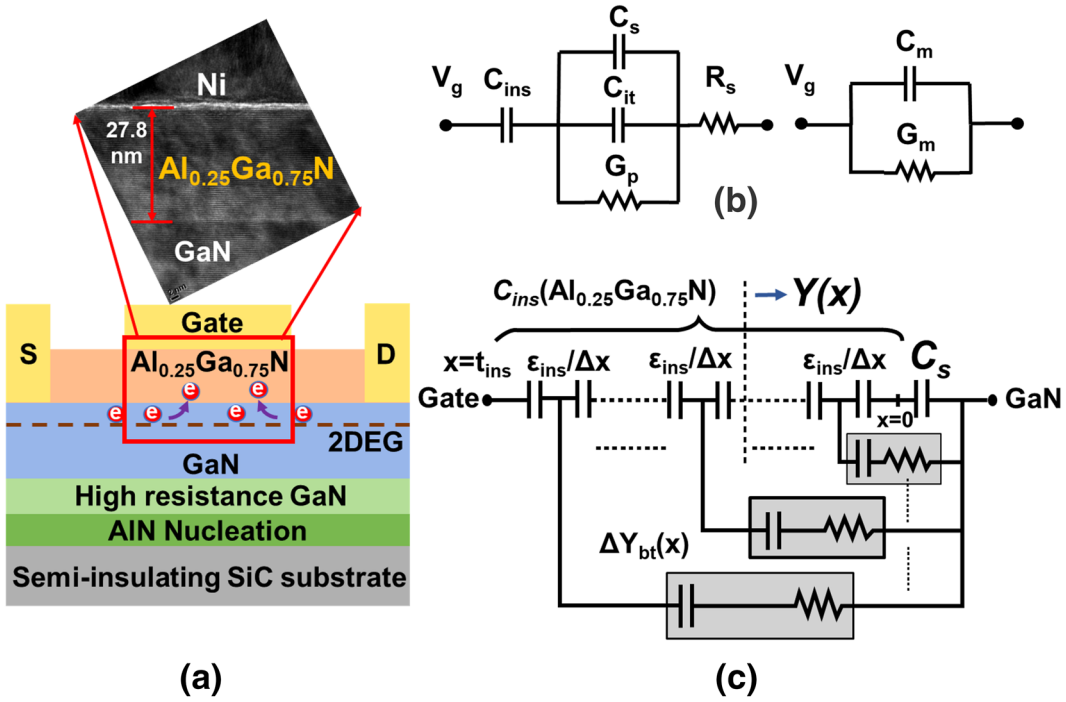

Figure 1. (**a**) Schematic cross-section and high-resolution TEM image of $Al_{0.25}Ga_{0.75}N$/GaN device. (**b**) Equivalent circuit diagram representing metal–insulator–semiconductor structure in depletion mode. (**c**) Equivalent circuit representing distributed bulk-oxide trap model[16,17].

the dielectric or the passivation layer[12,13]. However, from a device point of view, characterization of the AlGaN/GaN interface would be more beneficial because this interface is directly related to carrier transport.

In this study, we tried to include all types of AlGaN/GaN interfacial trapping analysis for a better understanding. We extracted the interface trap density (D_{it}) between AlGaN and GaN and the deep-level/border trap density N_{bt} in the AlGaN barrier layer in a long-channel AlGaN/GaN HEMT fabricated on a SiC substrate. We mainly focused on the trap states inside the AlGaN layer, located at the interface and near the interface of the AlGaN/GaN, and tried to eliminate other probable interfacial trap contributing factors such as dielectric layers for passivation. We used the conventional frequency-dependent C–V and G–V characteristics to understand the interactions of the interface traps[14,15]. Along with these characteristics, we also investigated the deep-level/border trap behavior in the accumulation region by examining split C–V characteristics, which are typically observed in the conventional Si MOS structure[16,17]. Although some researchers have discussed border/bulk trap extraction with threshold voltage shift profiling, discharging-based trap energy profile technique, etc., the frequency-dependent CV method for border trap density extraction for AlGaN/GaN heterostructure is not present[18–20]. We further performed low-frequency (1/*f*) noise measurements as they are a highly powerful tool for analyzing the defects and impurities in semiconductor devices and because they aid in the estimation of the efficiency and reliability of these devices[21].

Experimental details

Figure 1a illustrates the cross-sectional schematic and the transmission electron microscopy (TEM) image of the HEMT device used in this study. Epitaxial layers were grown on a semi-insulating 330 µm SiC substrate by metal–organic-chemical-vapor-deposition (MOCVD). Layers were deposited from bottom to top in the following order: an AlN nucleation layer, a 2.6 µm high-resistance GaN layer, a 150 nm GaN channel, and a 28 nm $Al_{0.25}Ga_{0.75}N$ barrier layer. Hall measurements revealed the mobility (μ_{n_Hall}) and the sheet charge density (2DEG) to be 2200 $cm^2 \cdot V^{-1} \cdot s^{-1}$ and 9×10^{12} cm^{-2}, respectively. Mesa isolation was carried out with Cl_2 based inductively-coupled-plasma (ICP) etching to isolate the devices. Before ohmic metal deposition, the substrate was diluted with a mixture of HCl and deionized water (1:5) for 30 s to remove any kind of formed native oxide. To facilitate ohmic contact formation, a Si/Ti/Al/Ni/Au (1/25/160/40/100 nm) alloy was deposited on source and drain area using an electron beam (e-beam) evaporator and rapid thermal annealing at 830 °C was subsequently performed in N_2 ambient for 30 s. The contact resistance (R_C) and sheet resistance (R_{SH}) were extracted by transmission-line-method (TLM) measurements to be 1.2 Ω·mm and 320 Ω/□ respectively. A Ti/Au (20/300 nm) padding layer was deposited using the E-beam evaporator to achieve strong probe contact. Finally, gate metal consisting of Ni/Au (20/400 nm) was also deposited using e-beam evaporator. The gate length (L_g), gate width (W_g), and source-to-drain distance (L_{sd}) of the fabricated devices were 14, 50, and 18 µm, respectively. All the devices had the same source-to-gate (L_{sg}) distance and gate-to-source distance (L_{gd}) of 2 µm. From the high-resolution TEM image shown in Fig. 1a, the well deposited $Al_{0.25}GaN_{0.75}N$/GaN interface can be observed. The thickness of $Al_{0.25}GaN_{0.75}N$ was well around 28 nm (27.8 nm) and formed a good interface with the GaN channel layer.

Extraction model

Interface trap model. In conventional Si MOSFET devices, the conductance method is one of the most popular methods for determining the interface trap density (D_{it})[14,22]. Typically, the interface between the dielectric and the semiconductor is analyzed for trap extraction. In our study, we applied the conductance method to our device structure. Because the $Al_{0.25}Ga_{0.75}N$ barrier layer has a wide band gap (~4 eV) and a high dielectric constant (~9.4), it can act as an insulator and perform comparably to a dielectric material. The conductance method relies on the extraction of the equivalent parallel conductance (G_P) from the measured frequency-dependent C–V and G–V characteristics. Figure 1b shows the equivalent circuit of a MOSFET in the depletion region, where C_{it}, C_S and R_S represents the interface trap capacitance, the semiconductor capacitance, and series resistance, respectively. The interface trap capacitance can be expressed as $C_{it} = qD_{it}$ (where q denotes the elemental charge). G_P can be determined by the following equation:

$$G_p = \frac{\omega^2 C_{ins}^2 G_c}{G_c^2 + \omega^2 (C_{ins} - C_c)^2} \tag{1}$$

Here, C_{ins} is the insulator capacitance; ω is the angular frequency; and C_c and G_c are, respectively, the corrected measured capacitance and conductance corresponding to the series resistance R_S.

Using the normalized $(G_P/\omega)_{max}$ value, we can determine the value of D_{it} as follows[23]:

$$D_{it} \approx \frac{2.5}{Aq}\left(\frac{G_p}{\omega}\right)_{\max} \tag{2}$$

Here, A denotes the device area.

The trap response of the interface states can be determined from the Shockley–Read–Hall statistics of capture and emission[24]:

$$\tau = \frac{1}{2\pi f} = \frac{1}{\omega} = \frac{e^{\left(\frac{\Delta E}{K_B T}\right)}}{\sigma \nu_{th} D_{dos}} \tag{3}$$

Here, ΔE denotes the difference of energy between the conduction band E_C and trap energy level E_T. K_B and T are the Boltzmann constant and temperature. σ, ν_{th} and D_{dos} represent the cross–section of traps, the average thermal velocity, and the effective density of states, respectively.

Border trap model. The distributed circuit model shown in Fig. 1c was used for the extraction of border traps[16,17]. It can provide information on the border trap states inside the insulator bulk with frequency-dependent C-V measurement. This model can be represented by the following first-order differential equation:

$$\frac{\partial Y}{\partial x} = -\frac{Y^2}{j\omega\varepsilon_{ins}} + \frac{q^2 N_{bt} \ln\left(1 + j\omega\tau\right)}{\tau} \tag{4}$$

This equation has a boundary condition of $x = 0$, $Y = j\omega C_S$, while Y being the total admittance. N_{bt} in the above equation denotes the density of border traps in the insulator layer.

Usually, the carriers in the channel region and the border traps in the insulator layer can exchange charge through tunneling[16]. The average time (τ) required for an empty trap to capture electron can be calculated as[25]

$$\tau = \tau_o e^{2kx} \tag{5}$$

$$\text{where, } k = \frac{\sqrt{2m* \times E_b}}{\hbar}$$

Here, τ_o denotes the time constant of the capture and emission of a trap. x denotes the distance between the interface and the trap. m^* and k denote the effective mass of the $Al_{0.25}Ga_{0.75}N$ layer and the attenuation coefficient respectively. The barrier height between the $Al_{0.25}Ga_{0.75}N$ and the GaN channel conduction band is denoted by E_b and the reduced Plank's constant by $\hbar$.

τ_o can be characterized as

$$\tau_o = (n_s \nu_{th} \sigma)^{-1} \tag{6}$$

where n_s, ν_{th} and σ are the electron density of the channel surface, the average thermal velocity of the electron, and the border trap cross-section area of capture/emission, respectively.

Equation 4, can be simplified into the following equation for the total capacitance, C_{tot}[26],

$$C_{tot} = \frac{1}{\frac{1}{C_{ins}} + \frac{1}{2k\varepsilon_{ins}} C_2(\omega)} \tag{7}$$

$$C_2(\omega) = 2k\sqrt{\frac{\varepsilon_{ins}}{qN_{bt}}} \coth(B) + \ln(\omega\tau_o) - \coth^2(B) \tag{8}$$

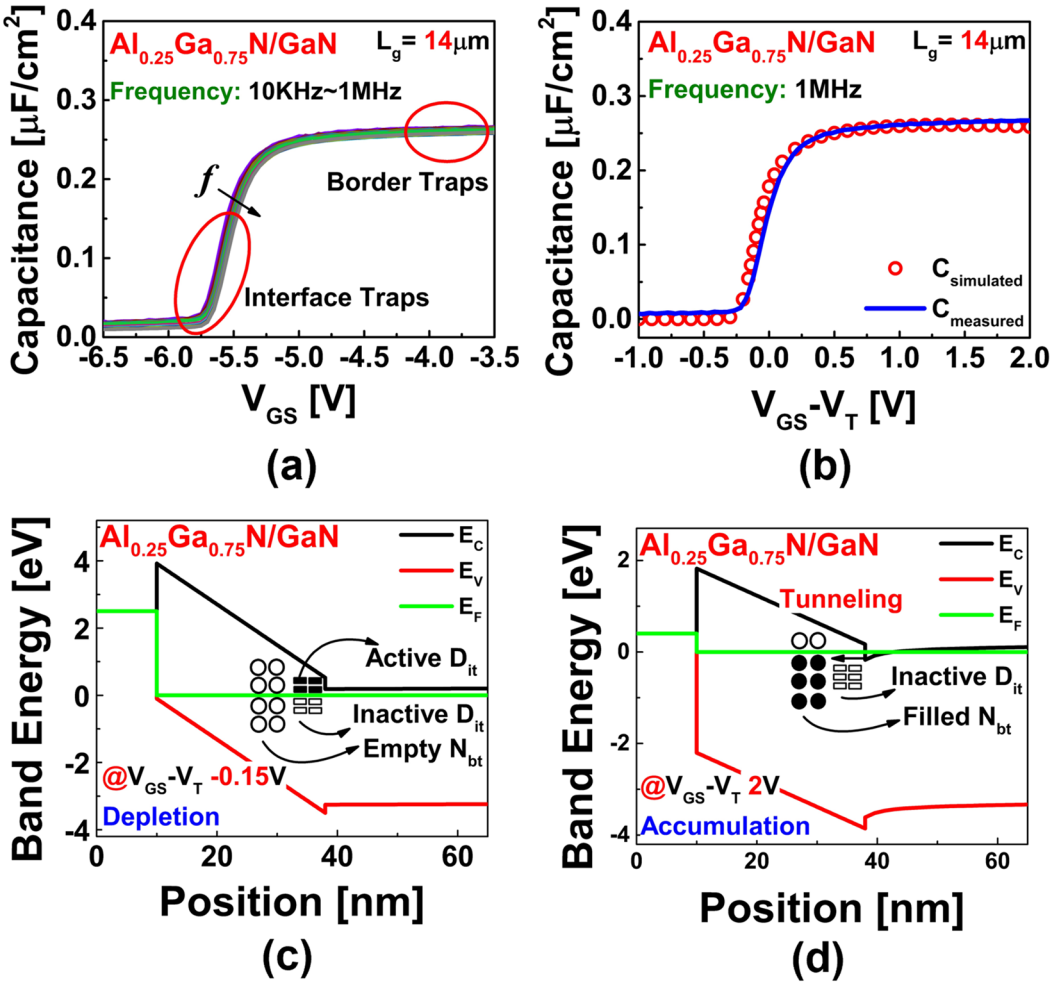

Figure 2. (**a**) Results of frequency-dependent C–V measurements showing active response region of traps. (**b**) Comparison between measured and simulated C–V characteristics. Simulated band diagram showing trap behavior (**c**) in depletion and (**d**) in accumulation.

$$B = a\tanh\left(\sqrt{\frac{1}{qN_{bt}\varepsilon_{ins}}}C_s\right) - \frac{1}{2k}\sqrt{\frac{qN_{bt}}{\varepsilon_{ins}}}\ln(\omega\tau_o) \tag{9}$$

Using N_{bt} and τ_o as fitting parameters, the best-fitted curve of C_{tot} with respect to frequency can be generated for the measured capacitance which will be discussed more in the results and discussion section.

The probing distance (X_p) of a border trap with a fixed frequency (f) while, $\omega\tau = 1$, can be described as[27]

$$X_p = \frac{1}{2k}\ln\frac{1}{2\pi f\tau_o} \tag{10}$$

Results and discussion

Figure 2a shows the results of the frequency-dependent C–V measurements of the $Al_{0.25}GaN_{0.75}N$/GaN HEMT where frequency dispersion is evident. Frequency dispersion can be caused by various reasons. Some of the main causes of frequency dispersion during C–V measurement are parasitic effect, lossy interfacial layer, surface roughness, and quantum mechanical confinement etc[28]. Among them, the most influential reason is the lossy interfacial layer of AlGaN/GaN. The trap states in the AlGaN layer are mostly the reason behind the dispersion. The frequency dispersion in the depletion region indicates that this region is the dominant region for interface traps, whereas the dispersion in the accumulation region indicates the dominant region of the border traps. We used the Nextnano simulation tool (one-dimensional Poisson–Schrodinger solver) to compare the measured and simulated capacitance with respect to a constant gate overdrive ($V_{GS} - V_T$), as shown in Fig. 2b. It is evident that both the measured and the simulated C–V curves are similar which indicates lower leakage current effect on the measured data. Thus, the AlGaN layer can be treated as an insulator owing to its high dielectric constant, similar to the MIS/MOS structure. Figure 2c, d show the band diagrams (determined via simulation) in the depletion

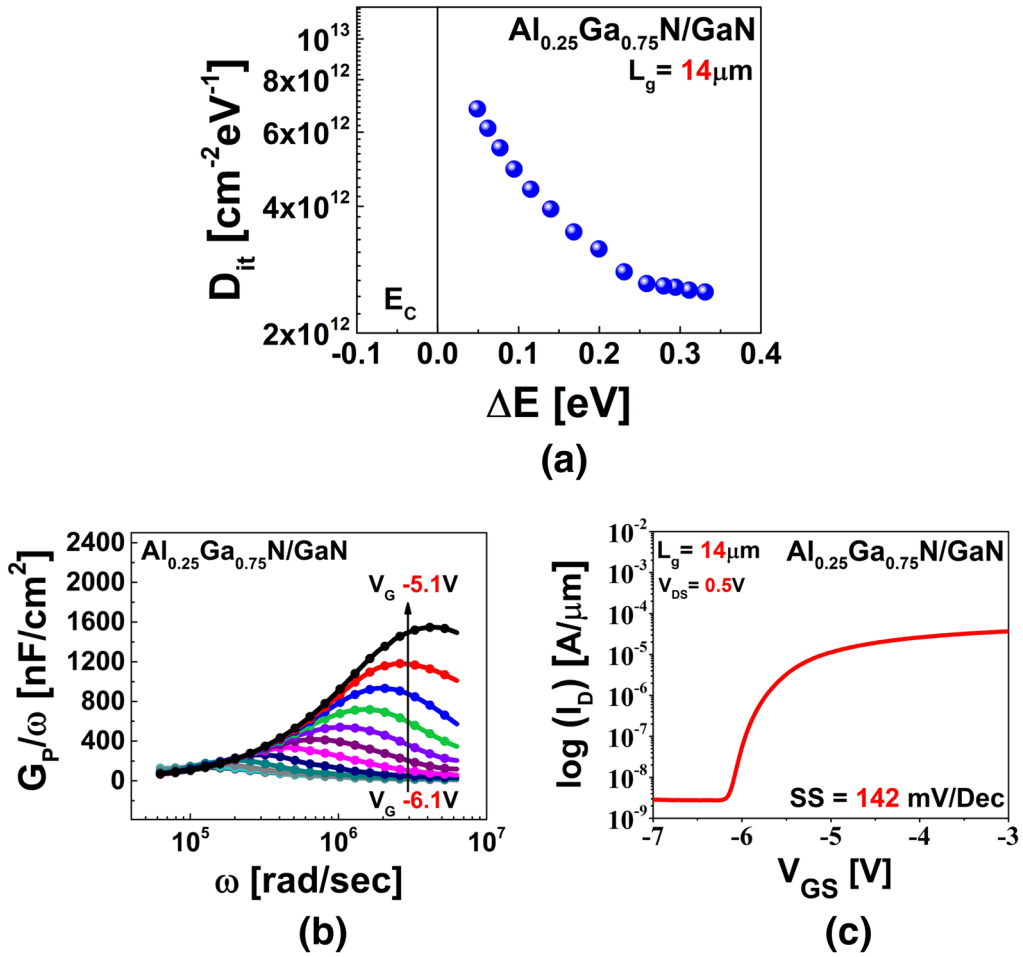

Figure 3. (**a**) Distribution of interface traps as a function of band energy state. (**b**) Equivalent parallel conductance (G_P/ω) with respect to frequency at different gate bias points. (**c**) Basic transfer curve ($\log(I_D)$–V_{GS}) showing SS of device.

and accumulation regions, respectively. In the depletion region, the interface traps above the Fermi level E_F are mostly active; this causes the capture and emission of the carriers in the channel region. In the accumulation region, where E_F penetrates the conduction band E_C, the electrons on the surface are captured and emitted by the border traps via tunneling.

A Keysight B1500A semiconductor device analyzer and an Agilent 4384A precision LCR meter were used for all DC measurements. 1/*f* measurements were performed using a setup comprising battery operated SRS SR570 low-noise current preamplifier, HP 35670A dynamic signal analyzer, and a 1 Hz filter unit.

The insulator capacitance was determined by the following equation:

$$C_{ins} = \frac{\varepsilon_o \varepsilon_{ins}}{t_{ins}} \tag{11}$$

Here, ε_o is the permittivity of free space and ε_{ins} is the relative permittivity of the $Al_{0.25}Ga_{0.75}N$ layer. As it is known from the literature, the value of ε_{ins} as calculated from $\varepsilon = -0.5x + 9.5$—where x denotes the Al content of the $Al_xGa_{1-x}N$ layer—for $x = 25\%$ is around 9.375[29,30]. The tensor components of AlN and GaN's {0001} relative permittivity are linearly interpolated to obtain the relation. The parallel equivalent conductance G_p was calculated using Eq. 1 with correction of the measured capacitance and conductance for the series resistance. Figure 3b shows a plot of the parallel conductance G_p/ω versus the angular frequency ω. D_{it} was measured from the $(G_p/\omega)_{max}$ peak, using Eq. 2; The extracted value of D_{it} using the conductance method was in the range of 2.5×10^{12} $cm^{-2} \cdot eV^{-1}$ to 7.1×10^{12} $cm^{-2} \cdot eV^{-1}$ which is well within the range of 10^{11}–10^{14} cm^{-2} eV^{-1} for S-HEMT and MOS-HEMT from literature[10,12,31]. Figure 3a shows the active D_{it} with respect to the trap energy (ΔE), which was determined from Eq. 3. For this calculation, the frequency corresponding to $(G_p/\omega)_{max}$ was considered. At room temperature (300 K), the average thermal velocity v_{th} and the effective density of states (D_{dos}) of the GaN material were considered to be 2.6×10^7 $cm \cdot s^{-1}$ and 1.2×10^{18} cm^{-3}, respectively[31]. The value of the capture cross-section σ was assumed to be 3.4×10^{-15} cm^2 from the literature[32]. The reliability of the extracted value of D_{it} was determined via a theoretical calculation of the subthreshold swing (SS) using the following equation[33]:

Sample	$Al_{0.25}Ga_{0.75}N$/GaN
Parameter	Value
t_{ins} [nm]	28
ε_{ins}	9.375
m^* [m_o]	0.19
E_b [eV]	0.8
k [nm^{-1}]	1.99
C_S [$\mu F{\cdot}cm^{-2}$]	0.27
τ_o [s]	1×10^{-12}
D_{it} [$cm^{-2}{\cdot}eV^{-1}$]	2.5×10^{12}
N_{bt} [$cm^{-3}{\cdot}eV^{-1}$]	1.5×10^{19}
N_t [$cm^{-3}{\cdot}eV^{-1}$]	1.3×10^{19}

Table 1. Parameters used and extracted values of D_{it} and N_{bt}.

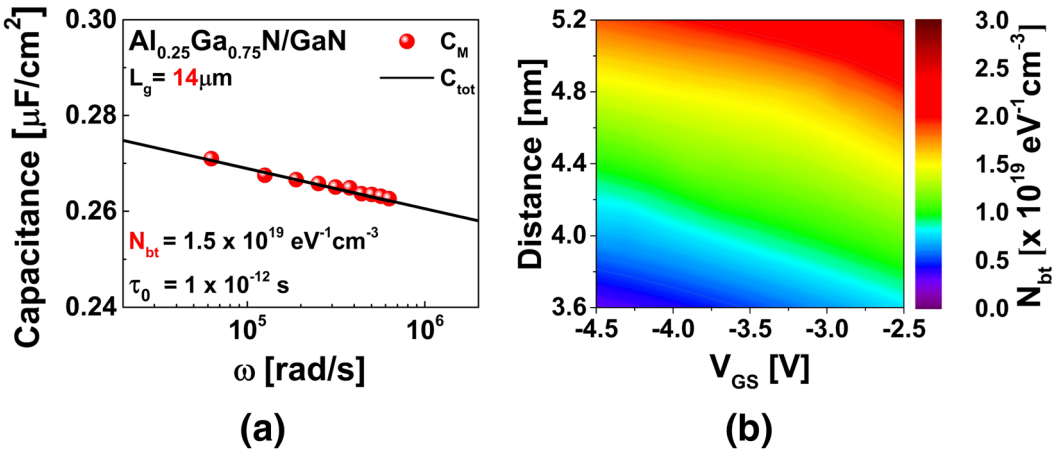

Figure 4. (**a**) Fitting curves generated using distributed circuit model at $V_{GS} = -3.5$ V. (**b**) Contour mapping of border trap distribution in $Al_{0.25}Ga_{0.75}N$ layer from $Al_{0.25}Ga_{0.75}N$/GaN interface.

$$SS = \frac{kT}{q}\ln 10.\left(1+\frac{qD_{it}}{C_{ins}}\right) \tag{12}$$

The value of the SS calculated from the lowest extracted D_{it} was around 143 mV·dec^{-1}, whereas the value determined by the basic I–V measurement was found to be 142 mV·dec^{-1} (Fig. 3c). This similarity of the measured and calculated values confirms the reliability of the extracted value of D_{it}.

We used the parameters in Table 1 to extract the border trap density N_{bt}. For the calculation of the attenuation coefficient, the effective mass of $Al_{0.25}Ga_{0.75}N$ was considered to be $0.19m_o$ (where m_o denotes the electron mass at rest)[34]. The semiconductor capacitance C_S was estimated via Nextnano simulation at an accumulation gate bias of − 3.5 V, which was the primary N_{bt} extraction voltage considered in this study. From Eq. 4, the best-fitted capacitance curves were obtained at − 3.5 V under consideration of N_{bt} and τ_o as variable fitting parameters. The best-fitted curve was obtained at $N_{bt} = 1.5\times10^{19}$ cm$^{-3}{\cdot}$eV^{-1} and $\tau_o = 1\times10^{-12}$ s, as shown in Fig. 4a. Here, C_M denotes the capacitances measured at various applied frequencies at − 3.5 V and C_{tot} represents the fitted curve. The spatial distribution of N_{bt} as a function of both the applied V_{GS} and the probing distance into the $Al_{0.25}Ga_{0.75}N$ layer from the $Al_{0.25}Ga_{0.75}N$/GaN interface is shown in Fig. 4b. The N_{bt} values were extracted at various applied voltages at a particular applied frequency. The probing depth into the $Al_{0.25}Ga_{0.75}N$ layer from the interface was calculated by Eq. 10 using different τ_o values associated with the N_{bt} values. Because the border traps exhibit more dominant characteristics at lower frequencies, we employed a low frequency of 10 kHz to extract the probing depth. With an increase in V_{GS}, the Fermi level E_F tended to penetrate to a greater depth into the conduction band E_C. As a result, more electrons tended to tunnel into the deep-level traps. As all parameters except τ_o were fixed, τ_o showed an inverse relation with the probing depth.

1/f noise measurements were performed by varying the gate voltage V_{GS} and fixing the drain bias V_{DS} at 0.5 V. Figure 5a shows the normalized $S_{ID}/I_D{}^2$ (drain current noise spectral density) with respect to frequency up to 10^4 Hz under varying V_{GS} from the linear region. It is evident that as V_{GS} increased, and the device transitioned from weak inversion to strong inversion, noise level ($S_{ID}/I_D{}^2$) decreases. Plotting of the normalized

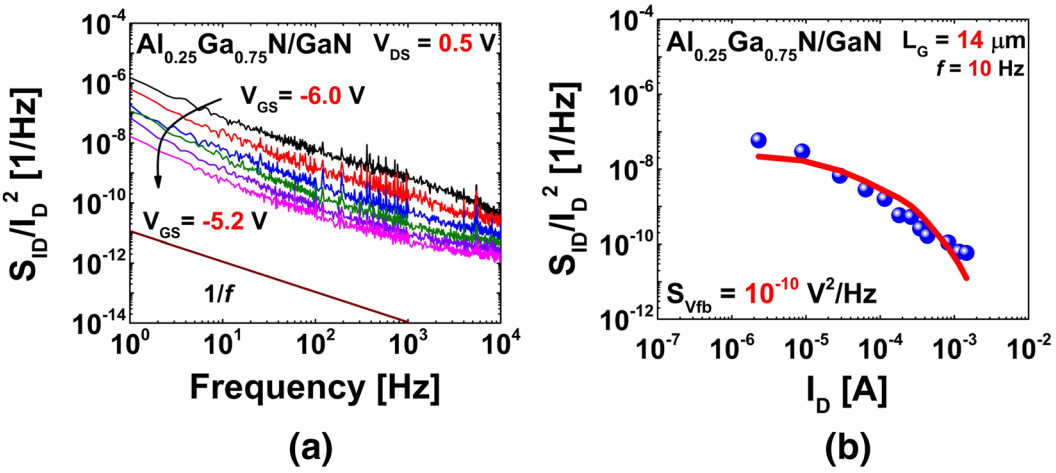

Figure 5. (**a**) Noise spectral density (S_{ID}/I_D^2) with respect to frequency at various gate bias (V_{GS}) points. (**b**) Noise spectral density (S_{ID}/I_D^2) and $(g_m/I_D)^2$ as functions of drain current I_D.

S_{ID}/I_D^2 as a function of I_D (drain current) provided results that were more explanatory. Figure 5b shows a plot of the normalized S_{ID}/I_D^2 (blue spheres) as a function of I_D at a frequency of 10 Hz. The channel carrier trapping phenomenon of the gate dielectric can be explained using the carrier number fluctuation (CNF) model by the following equations[21,35,36]:

$$\frac{S_{ID}}{I_D^2} = \left(\frac{g_m}{I_D}\right)^2 S_{Vfb} \tag{13}$$

$$S_{Vfb} = \frac{q^2 N_t kT\lambda}{WLC_d^2 f} \tag{14}$$

Here, S_{Vfb} denotes the flatband voltage power spectral density; kT, the thermal energy; WL, the channel area; C_d, the dielectric capacitance; f, the frequency; and N_t, the bulk/border trap density. λ denotes the tunneling attenuation distance of the dielectric, which is expressed as $\lambda = [4\pi(2\ m^*\Phi_B)^{1/2}/h]^{-1}$, where Φ_B is the dielectric barrier height[37]. According to the CNF model, the terms S_{ID}/I_D^2 and $(g_m/I_D)^2$ vary in similar ranges with the drain current or gate voltage. From Fig. 5b, it is evident that both S_{ID}/I_D^2 (blue spheres) and $(g_m/I_D)^2$ (red line) vary similarly over several decades under varying I_D. The S_{Vfb} value was calculated to be 10^{-10} $V^2{\cdot}Hz^{-1}$ from Eq. 13. Using Eq. 14, we then calculated the border trap density N_t to be around 1.3×10^{19} $cm^{-3}{\cdot}eV^{-1}$; this value is of a similar level to the values of the border trap density N_{bt} extracted from the distributed circuit model and well comparable to the data from literature of 10^{18}–10^{22} cm^{-3} eV^{-1}[20,36,38].

Conclusion

Unlike previous studies, which focused mainly on the insulator/AlGaN interface for trap extraction, the present study attempted to investigate the AlGaN/GaN interface for this purpose. We used modified versions of conventional MOS trap extraction methods to extract the interface trap density D_{it} and border trap density N_{bt} of the $Al_{0.25}Ga_{0.75}N$/GaN interface. We performed the extractions by considering the $Al_{0.25}Ga_{0.75}N$ layer to be comparable to the insulator of the MOS structure on account of the relatively high dielectric constant of the former. The D_{it} value extracted by the conductance method was in the range of 2.5×10^{12} $cm^{-2}{\cdot}eV^{-1}$ to 7.1×10^{12} $cm^{-2}{\cdot}eV^{-1}$, and the N_{bt} value extracted using the distributed circuit model was 1.5×10^{19} $cm^{-3}{\cdot}eV^{-1}$ with τ_o of 1×10^{-12} s. The border trap density N_t extracted using the CNF model via $1/f$ noise measurements was 1.3×10^{19} $cm^{-3}{\cdot}eV^{-1}$ (same level as the extracted value of N_{bt}), which confirmed the validity and reliability of our trap extraction method.

Data availability

The datasets generated during and/or analysed during the current study are available from the corresponding author on reasonable request.

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Author contributions

W.A. conducted most of the characterizations and wrote the manuscript including the figures. J.-W.S. and K.-Y.S. helped in device fabrication. J.-M.K., C.-Y.C. and K.-H.P. helped in the wafer growth processing. T.H., T.T., H.S., and H.M. provided epi structure and helped in overall quality check and review of the paper. T.-W.K. initiated the work and supervised the entire process. All authors analysed and discussed the results.

Competing interests
The authors declare no competing interests.

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