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# Reconfigurable Architecture for Multi-lead ECG Signal Compression with High-frequency Noise Reduction

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Electrocardiogram (ECG) is a record of the heart's electrical activity over a specified period, and it is the most popular noninvasive diagnostic test to identify several cardiac diseases. It is an integral part of a typical eHealth system, where the ECG signals are often needed to be compressed for long term data recording and remote transmission. Reconfigurable architecture offers high-speed parallel computation unit, particularly the Field Programmable Gate Array (FPGA) along with adaptable software features. Hence, this type of design is suitable for multi-channel signal processing units like ECGs, which usually require precise real-time computation. This paper presents a reconfigurable signal processing unit which is implemented in ZedBoard- a development board for Xilinx Zynq —7000 SoC. The compression algorithm is based on Fast Fourier Transformation. The implemented system can work in real-time and achieve a maximum 90% compression rate without any significant signal distortion (i.e., less than 9% normalized percentage of root-mean-square deviation). This compression rate is 5% higher than the state-of-the-art hardware implementation. Additionally, this algorithm has an inherent capability of high-frequency noise reduction, which makes it unique in this field. The confirmatory analysis is done using six databases from the PhysioNet databank to compare and validate the effectiveness of the proposed system.

The integrated use of information technology and electronic communication in the health sector is recognized as an eHealth system<sup>1</sup>. It is a technical platform that comprises diagnostic tools and microcomputer units. eHealth is especially a vital resource for the health care of the people from remote regions and developing countries as it helps the patients to consult specialist physicians using telecommunications. Even in developed countries, electronic health records are being kept for follow-up treatment. Therefore, electronic communication and data recording are the fundamental system components of an eHealth system.

Cardiovascular disease (CVD) is a generic term to indicate the disorders related to heart and blood vessels. According to the World Health Organization (WHO) CVDs are responsible for 31% of all worldwide deaths, taking approximately 18 million lives per year<sup>2</sup>. Regular monitoring of a patient's heart condition is the primary requirement for diagnosing the underlying cardiac diseases. A record of the electrical potential of heart muscle depolarization over a specified time is called the Electrocardiogram (ECG or EKG), and this is measured by placing multiple electrode pads (sensors<sup>3-5</sup>) on specified places of the chest. These electrodes are connected to an ECG machine for the signal processing and recording. The electrocardiogram is the most popular noninvasive diagnostic test to determine cardiac health<sup>6</sup>. It had been used as a diagnostic test in clinical medicine for more than 70 years<sup>7</sup>. At present, ECG is one of the routine tests for any complete medical evaluation, and it is an indispensable part of a modern eHealth system<sup>8</sup>. It should be noted that, while recording ECG, the measurement is done by determining the potential difference between predefined locations on the body surface. This generates distinct ECG vectors known as the 'leads'. Common clinical standard uses a 12-lead ECG system for assessing a patient's cardiac health<sup>9</sup>.

As a part of an eHealth system, ECG signal requires to be transmitted to a distant location for telediagnosis and stored for future treatment reference. Thus the necessity of ECG signal compression arises. Compression

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helps to reduce the required bandwidth for data transmission. It also saves space for storing the ECG data. This paper presents the design and implementation of an FPGA based reconfigurable system for ECG compression.

Various noises affect ECG signal during the data accusation<sup>10</sup> and transmission process<sup>11</sup>. The high-frequency noise is one of the primary reasons for ECG signal distortion<sup>12</sup>, and it mostly contains the powerline interference (50–60 Hz) and the electromyographic (EMG) noise (100–500 Hz)<sup>13</sup>. One of the added benefits of the proposed system is its built-in capability of high-frequency noise cancellation. Consequently, additional high-frequency noise filtering mechanism in the eHealth system will be redundant and the overall system complexity will be reduced.

The FPGA is essentially an integrated circuit (IC) which can be reconfigured for any assigned task, hence the name 'reconfigurable computing<sup>14</sup>. It is widely used for ASIC (Application Specific Integrated Circuit) prototyping and hardware verification<sup>15</sup>. Because of the unique capability of parallel computation<sup>16</sup>, FPGAs are significantly faster in the applications where simultaneous computation is needed for multiple processes<sup>17</sup>. In a typical electrophysiological monitoring unit, data accusation is often made by collecting signals from multiple channels. As mentioned earlier, a clinical ECG has a 12 lead standard. This means while processing the data it needs 12 concurrent signal processing. Therefore, FPGA is used as the computation unit in the proposed architecture.

The fundamental focus of an effective ECG compression is efficient transmission and data storage without losing critical diagnostic information. Many methods are found in the literature for the compression of the ECG signal. Based on the techniques, they can be classified as follows: (i) time domain compression, (ii) transform domain compression, (iii) compression by parameter extraction, and (iv) hybrid method. The original time-domain ECG signal features are scrutinized, and redundant data points are discarded in the time domain compression method<sup>18</sup>. As no significant data conversion or transformation is needed in this method, this scheme offers relatively fast processing<sup>19</sup>. The second compression method is the transform domain compression, and it operates by converting the original signal to frequency<sup>20</sup> or spatiotemporal<sup>21</sup> signal. In this method, the signal is processed and compressed after the transformation. Consequently, it takes longer processing time than the first method, though this method is capable of more efficient compression. Compression by parameter extraction is the third ECG compression method. This scheme requires a complex feature extraction from the given signal. Various learning methods are applied to determine the parameter characteristics, which are then used to compress the original signal and conserved thereafter for decompression<sup>8,22</sup>. Some contemporary feature extraction techniques include supervised dictionary learning<sup>23</sup>, object detection<sup>24,25</sup>, background information retrieval<sup>26,27</sup>, and deep learning<sup>28</sup>. Hybrid compression method combines the particulars from time-domain, transform-domain, and parameter extraction methods to create an efficient compression scheme<sup>29,30</sup>. The last two methods involve more computation than the first two methods. Hence, they require more processing time and resources.

Nonetheless, most of the above researches are mainly concentrated on the software level<sup>31,32</sup>. This paper is more focused on the system level implementation of a real-time ECG compression algorithm. Therefore, a fast signal processing method with low hardware resource requirement is perceived while conceiving the appropriate ECG compression algorithm. The proposed system employs a transform domain compression method based on Fast Fourier Transformation (FFT) technique. This system is hardware implemented and demonstrates a significant improvement in compression efficiency without any vital signal deformation. Moreover, it has a built-in high-frequency noise cancellation ability, which makes it unique from the other implemented systems. A comparative study of the proposed system with the other methods is presented in the "Result Analysis" section.

#### Methodology

The Fast Fourier Transform is a highly optimized form of the Discrete Fourier Transform (DFT), which takes a sequence of sampled data in the time domain and computes the frequency component of that data sequence. DFT is defined by the following equation<sup>33</sup>:

$$X(k) = \sum_{n=0}^{N-1} x(n) e^{-j2\pi kn/N}, \quad k = 0, 1, 2, ..., N-1$$
(1)

Here, each of the single frequency components, X(k) is calculated by considering each of the time domain samples, x(n). Hence,  $N^2$  addition and multiplication is needed to compute N number of samples. To recover the time domain components from frequency samples IDFT (Inverse DFT) is used, and it is defined<sup>33</sup> by:

.. .

$$x(n) = \frac{1}{N} \sum_{k=0}^{N-1} X(k) e^{j2\pi k n/N}, \quad n = 0, 1, 2, ..., N-1$$
(2)

Again, Eq. (2) requires  $N^2$  addition and multiplication to process N number of samples in spatio-temporal domain. This large number of mathematical operation often creates a computational burden. Hence, FFT and IFFT (Inverse FFT) algorithms are developed<sup>34</sup>. FFT reduces the calculation complexity of DFT by factorizing its matrix into sparse arrays in which the majority of the elements are zero<sup>35</sup>. For N number of points the required number of complex multiplication in the DFT is  $N^2$ , whereas in the similar case, only  $(N/2)log_2N$  complex multiplication is needed in the FFT algorithm<sup>33</sup>. As an example, if 128 number of point is considered, DFT and FFT involve 16,384 and 448 complex multiplication respectively. Thus, FFT improves the computational speed by a factor of 36.6 in this case<sup>34</sup>.

Using the FPGA as the signal processing hardware gives the unique capability to decompose the complete multichannel architecture into a series of structurally identical single channel core units.

Consequently, a composition of these elementary segments becomes the complete multichannel system as shown in Figs. 1 and 2. The concept of parallel computation in the FPGA can also be understood from this figure.



Figure 1. Core units.



Figure 2. Complete multichannel system architecture.



Figure 3. Compression Steps.

Twelve signals from the ECG signal accusation unit are fed into the FPGA based signal processing core, and these signals are simultaneously processed to produce the desired real-time outputs.

The proposed compression algorithm works in three steps. At first, the original time domain ECG signal is subjected to FFT for transforming it into the frequency domain. Next, the first level compression is done utilizing the 'symmetric property' of this frequency response. Finally, additional compression is performed by discarding the high-frequency noise components. Figure 3 demonstrates a simple block diagram to clarify the compression steps.

A bit accurate MATLAB program is developed, and a standard ECG signal from the MIT-BIH Normal Sinus Rhythm Database (collected from the PhysioBank<sup>36</sup> record: 16265, sampling frequency 128 Hz) is used to demonstrate the proposed method. As mentioned earlier, for simplicity, this primary model is designed for a single channel ECG compression and decompression. The complete multichannel scheme is implemented in hardware and described in the section 'FPGA Implementation'. Figure 4 shows an epoch of a single channel signal from the aforementioned ECG, displaying a time window of 1 second.

As mentioned earlier, the sampling frequency is 128 Hz. Therefore, this epoch of 1 second corresponds to 128 data samples in the time domain. As the first step of compression, FFT is used to transform this time domain signal to the frequency domain. Here, 128-point FFT is applied to the signal of Fig. 4, and the outcome is 128 complex samples in the frequency domain. This frequency response in absolute value is shown in Fig. 5.

It is mathematically established that applying FFT to a real signal results in a symmetric complex signal (with the real and imaginary parts)<sup>37</sup>. Since the input ECG is a real signal, the FFT output is a complex one, and as expected, it is symmetric in nature. The data in frequency domain sample number 65 through 128 are redundant to store in the memory because they can be regenerated by simply mirroring the rest of the data. Therefore, the first level of compression is performed by discarding half of the FFT data.

At this point, it should be noted that the ECG frequency components are dominant in the lower frequency range  $(<30 \text{ Hz})^{38}$ . Here, the sampling frequency is 128 Hz. Nyquist theorem dictates that the input signal can represent up to half of its sampling frequency<sup>33</sup>. Hence, the input signal can have frequency components up to 64 Hz. In this case, 128-point FFT is applied; hence it has a 0–64 Hz band, which is conveniently represented by the respective sample numbers. Therefore, for the second level of compression, data of the sample number 33 through 64 are dropped, as they are essentially the high-frequency (33–64 Hz) noise components. Thus the essential lower frequency components (0–32 Hz) prevail while the high-frequency (HF) noises (>32 Hz) are discarded in the compressed signal. These two-level compression are shown in Figs. 6 and 7 respectively.



Figure 4. Time-domain ECG of a normal sinus rhythm.



Figure 5. Frequency-domain (128-point FFT) output.



Figure 6. FFT output of the ECG signal.

To explain the compression ratio, let us take the above example in consideration. Here, the input time domain signal has 128 real number. At first, consider this numbers in an input bin A. The FFT output is 128 complex numbers. Putting the real and imaginary number in the separate bins will result in 2 bins B and C with 128



Figure 7. Compressed ECG in frequency domain.



Figure 8. Decompression Steps.

number in each of them, totaling 256 numbers in the memory. This means the resultant memory size is, in fact, taking double space compared to the input. However, after the first level of compression, the size of the bin B and C will be half, as these bins will now contain 64 numbers each. At this point the total output memory contains 128 numbers, which is the same as the input bin. Finally, the second level of compression is executed by dropping the high-frequency noise signals. This process will further size down bin B and C. Now, these bins hold 32 numbers each. Therefore, the final output bins will contain 64 numbers in total. The compression ratio (CR) is defined by<sup>39</sup>,

$$CR(\%) = \frac{\text{size of the input stream} - \text{size of the output stream}}{\text{size of the input stream}} \times 100$$
(3)

For this particular example, the size of the input and output stream is 128 and 64 respectively. In this case, the compression ratio is 50%. However, CR can be easily adjusted by modifying how much high-frequency components is to be discarded.

The decompression algorithm is somewhat a reverse technique of the compression method. Figure 8 demonstrates a simplified block diagram of the decompression process. Taking the compressed ECG signal from the preceding example, the main objective of decompression is to recover the data of the frequency sample number 33 through 128. As mentioned earlier, the discarded data of the sample number 33 through 64 are actually high-frequency noise components. Therefore, as the first step of decompression, the data corresponding the sample number 33 through 64 are substituted by zeros to ensure the HF noise reduction. The second step is mirroring the frequency components of sample number 1 through 64 to regenerate the data of the sample number 65 through 128. Finally, the frequency domain decompressed signal is transformed into the time domain using the IFFT. Figures 9 and 10 show the decompression process and the restored time-domain ECG signal.

#### **FPGA** Implementation

ZedBoard is an optimum cost-effective development board manufactured by Digilent. This board employs Xilinx Artix-7 FPGAs coupled with a dual-core ARM Cortex-A9 processor, which is specially optimized for digital signal processing (DSP) applications<sup>40</sup>. ZedBoard is used as the processing unit for implementing the proposed scheme in hardware level.

System Generator is one of the design tools for the implementation of DSP algorithms in Xilinx devices, and it is used to program the ZedBorad in this research. System Generator works as a toolbox for Simulink, a graphical programming environment of MATLAB. A simple diagram of the practical hardware design is shown in Fig. 11 and the screenshot of the practical system generator design is illustrated in Fig. 12.

It should be noted that this core processing unit consists of both compression (blue shaded portion of the Figs. 11 and 12) and decompression (green shaded portion of the Figs. 11 and 12) unit. If necessary, the practical arrangement in the eHealth system can be designed either as a compression unit (for transmission system) or as a decompression unit (for reception system).

The compression unit is composed of three subunits— one FFT module and two compression subunits. The input ECG signal is fed into the FFT unit, and it returns two FFT outputs as real and imaginary numbers. These real and imaginary parts are compressed in the following units. The output of these compression units are the desired compressed signal which can be stored or transmitted for farther use. In the design, these compressed



Figure 9. ECG decompression in frequency domain.



Figure 10. IFFT to retrieve the temporal ECG.





signals are used as the input of the decompression unit. Here, the decompression unit is also comprised of three subunits. Two of them are for decompressing the compressed frequency-domain ECG signal. The final subunit is the IFFT module, which converts the decompressed frequency-domain ECG signal to the desired time-domain ECG as the output. Figure 13 shows signals of different processing stages in the Xilinx Waveform Viewer.

Table 1 shows the hardware resources required in the implementation of a single channel ECG processing unit (i.e. the core unit) on Zedboard. This ECG processing unit comprises both compression and decompression subsystems. Comparing the number of used resources with the available resources on Zedboard, it is possible to identify the plausible maximum number of core unit implementation on a single Zedboard. Here, the core unit utilizes 34% of the available DSPs, featuring the largest percentage of available resource consumption. Hence, two ECG processing units (including both compression and decompression subsystems) can be implemented on one Zedboard. Consequently, six Zedboards will be required for the implementation of a twelve channel system with compression-decompression capability. However, for an eHealth transmission or recording system, only



Figure 12. Screenshot of the practical System Generator unit.



**Figure 13.** Different signals in the Xilinx Waveform Viewer: (**a**) ECG input, (**b**) real part of the ECG in frequency-domain, (**c**) imaginary part of the ECG in frequency-domain, (**d**) compressed real part of the ECG in frequency-domain, (**e**) compressed imaginary part of the ECG in frequency-domain, (**f**) decompressed real part of the ECG in frequency-domain, (**g**) decompressed imaginary part of the ECG in frequency-domain, (**h**) decompressed FPGA ECG output in time-domain.

	Unit								
Resource $\downarrow$	Compression	Decompression	Common	Total	Available				
BRAMs	1	2	0	3	140				
DSPs	9	66	0	75	220				
LUTs	2480	3172	113	5765	53200				
Registers	2915	4108	8	7031	106400				

Table 1. System resource utilization.

the capability of compression is adequate. In this case, a twelve channel ECG compression unit can be built using only one Zedboard. To built an eHealth reception or restoring system, only decompression ability is required. Therefore, four Zedboards will be needed to design a twelve channel ECG reconstruction unit.

In this research, the prototype uses Zedboard for hardware implementation. This development board is a low-cost option with a relatively low-end FPGA as the processing unit. Though employing this board offers a budget development prospect, this is also one of the limitations of the implemented system. The high-end boards provide advanced FPGAs with more hardware resources. Therefore, the processing unit can accommodate more core units than the proposed prototype. Furthermore, complex algorithms can be adopted if adequate hardware resources become available. This constitutes a scope for future development.

### **Result Analysis**

As mentioned earlier, the proposed system compresses the ECG signal in the frequency domain. This compression is done in two vital steps: discarding the symmetric data and removing the high-frequency components. The reconstruction of the discarded symmetric data does not involve any data loss as it can be done by simple data mirroring. However, as the high-frequency components are considered as noises and permanently discarded during the compression process, the restored ECG signal does not inherit the high-frequency components. Though



Figure 14. Superimposed input and output ECG traces.

this process attributes as a low pass noise filter, the removal of high-frequency components makes the decompressed ECG somewhat different from the original signal.

For a preliminary graphical comparison, the raw input and the recovered output ECG are superimposed in the Fig. 14. It can be readily comprehended from a thorough visual inspection that, these two ECG traces are practically indistinguishable. As the ECG compression should aim to maximize compression efficiency without the deterioration of the signal quality, both the compression efficiency and the signal quality are evaluated while analyzing the performance of the proposed system.

Compression efficiency indicates how much the processed data is compressed compared to the raw data. The most common parameter to evaluate the compression efficiency is to measure the "Compression Ratio (CR)"<sup>39</sup>. CR is defined by Eq. (3) in the "Methedology" section which can be rewritten in the form of Eq. (4) for further discussion.

$$CR(\%) = \left(1 - \frac{\text{size of the output stream}}{\text{size of the input stream}}\right) \times 100$$
(4)

It should be noted that in some literature, CR is also mentioned as the Data-volume Saving (DS) as it essentially indicates the percentage of data being saved by the compression<sup>41</sup>.

It goes without saying that the quality of the reconstructed ECG signal must be satisfactory to avoid misdiagnosis. There are several parameters to assess the quality of the decompressed ECG. Among them, the "Percentage Root mean square Difference (PRD)" is the most common and the "Normalized version of Percentage Root mean square Difference (PRDN)" is the most accurate<sup>39</sup>. PRD and PRDN are defined by the Eqs (5) and (6) respectively.

$$PRD(\%) = \sqrt{\frac{\sum_{n=1}^{N} [x(n) - \tilde{x}(n)]^2}{\sum_{n=1}^{N} [x(n)]^2}} \times 100$$
(5)

$$PRDN(\%) = \sqrt{\frac{\sum_{n=1}^{N} [x(n) - \tilde{x}(n)]^2}{\sum_{n=1}^{N} [x(n) - \bar{x}(n)]^2}} \times 100$$
(6)

Here, x(n) is the original signal,  $\tilde{x}(n)$  is the reconstructed signal and  $\bar{x}(n)$  is the mean of the original signal. According to<sup>39,42</sup> and<sup>43</sup>, if the value of PRDN is less than 9% then the quality of the reconstructed signals are considered as "very good".

The acceptable ECG sampling frequency range for legitimate clinical use is 100–1000 Hz<sup>44</sup>. Therefore, to cover this frequency range, six databases are used to assess the performance of the proposed system. These datasets are downloaded from the PhysioBank<sup>36</sup> and presented in the Table 2 with relevant references.

The compression ratio of the processed ECG can be controlled by simply adjusting how much high-frequency components to be discarded. However, dropping too much data will, of course, distort the resultant signal from the original one. Figure 15 shows the relationship between the Compression Ratio and the Normalized Percentage Root mean square Difference for various sampling frequency.

As expected, a higher percentage of CR gives a higher rate of PRDN. This case is more severe for the lower sampling frequency but much less prevailing for the higher one. This phenomenon can be explained by using the Nyquist theorem as mentioned in the "Methodology" section. The ECG signals with higher sampling frequency inherently possess greater high-frequency noise components in it. Hence, it is possible to discard much of these noisy data during the compression stage without declining the signal quality. Actually, this property is suitable for practical applications; as for similar signals, a lower sampling frequency already consumes fewer data. As the signals with higher sampling frequency occupy more data, it makes sense to compress it with greater compression efficiency. Figure 15 also indicates the 9% PRDN line, which is the boundary condition for being a "very good"

Database Name	Sampling Frequency, F <sub>S</sub>	Reference	
MIT-BIH NSR Database	128 Hz	Goldberger et al. <sup>36</sup>	
European ST-T Database	250 Hz	Taddei <i>et al</i> . <sup>46</sup>	
MIT-BIH Arrhythmia Database	360 Hz	Moody et al.47	
MAC ECG Database	500 Hz	Behravan <i>et al.</i> <sup>48</sup>	
ANSI/AAMI EC13 Test Waveforms	720 Hz	AAMI <sup>49</sup>	
ECG DMMLD Database	1000 Hz	Johannesen et al. <sup>50</sup>	

Table 2. Used databases for the performance evaluation.



Figure 15. CR vs. PRDN for different sampling frequency.



Figure 16. Maximum allowable CR (%) for different sampling frequency.

compressed signal. Considering this 9% PRDN as the higher limit of signal distortion we can find out the maximum allowable compression ratio for different sampling frequency as shown in Fig. 16.

At this point, it should be noted that, though discarding high-frequency components distorts the compressed signal from the original one, it acts as a high-frequency noise reduction process. This is an added benefit of the proposed compression system. Using FPGAs for hardware implementation plays another vital role in this research. As a reconfigurable device, the same FPGA units can be easily configured for different compression ratio for different sampling frequency when required. This indeed makes the eHealth system more flexible for global implementation.

To conclude the result analysis a comparative study between the proposed system and the previous works is presented in Table 3. In spite of being the most critical quality measurement parameter, PRDN is not specified in some of the papers. However, PRD is measured for all cases. Therefore, PRD is also included as a quality measurement parameter for this study. For this table the performance of the proposed system is measured for 720 Hz sampling frequency using ANSI/AAMI EC13 Test database.

A few of the previous works (and<sup>20,29,30,45</sup>) can compress the ECG at a higher rate than the proposed one. However, their signal quality is less than the new system, and these works are not implemented at the hardware level. Among the hardware implemented works, the proposed method has the highest compression ratio (at

Reference	Method Used	CR (%)	PRD (%)	PRDN (%)	Hardware Implementation	Real-Time Execution	Noise Reduction
Cox et al. <sup>18</sup>	Time Domain	83	31.0	—	No	No	No
Abenstein et al. <sup>19</sup>	Time Domain	80	11.0	_	No	No	No
Alam et al. <sup>21</sup>	Transform Domain	90	5.1	6.5	No	No	No
Ziran <i>et al.</i> <sup>20</sup>	Transform Domain	95	10.6	—	No	No	No
Adamo et al.51	Parameter Extraction	42	1.1	17.3	No	No	No
Elgendi et al. <sup>8</sup>	Parameter Extraction	78	0.5	—	No	No	No
Elgendi et al. <sup>22</sup>	Parameter Extraction	83	1.9	—	No	No	No
Wang et al. <sup>29</sup>	Hybrid	94	7.3	_	No	No	No
Ma et al. <sup>30</sup>	Hybrid	94	1.7	25.7	No	No	No
Lee et al.45	Hybrid	95	2.9	40.6	No	No	No
Lai et al. <sup>52</sup>	Transform Domain	81	0.2	3.7	Yes	Yes	No
Luo et al. <sup>53</sup>	Transform Domain	85	0.2	2.6	Yes	Yes	No
Proposed	Transform Domain	90	1.5	8.8	Yes	Yes	Yes

Table 3. Comparison of compression performance.

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least 5% improvement) while maintaining the accepted PRDN limit. It is the only implemented system which can reduce noises from the ECG while compressing it. The overall signal quality is actually improved during the compression process as the high-frequency noise is reduced. This makes the new system unique. The higher data volume savings with better signal quality ensures economical telemedicine and electronic health record system. Therefore, the proposed system is more suitable for upper-level applications like eHealth systems.

### Conclusion

This paper presents a novel reconfigurable system architecture for electrocardiographic signal compression. To the best of our knowledge, this is the first hardware implemented ECG compression system which can reduce the embedded high-frequency noise from the original signal while compressing it. This unique feature enhances the overall ECG signal quality for further diagnosis. Because of its high compression performance and superior signal quality, this system is ideal for the incorporation with a contemporary eHealth care system. Furthermore, similar methods and system designs can be utilized for compressing other signals, especially the signals with distinct frequency dependence. The FPGA design can be used for prototyping a dedicated application specific integrated circuit in the future. This will make the system suitable for wearable wireless ECG monitoring systems.

#### Data availability

The datasets analyzed during the current study are available in the PhysioBank repository, www.physionet.org/ physiobank/.

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# **Author contributions**

M.H.C. and R.C.C.C. designed the experiment. M.H.C. conducted the experiment and performed the statistical analysis. M.H.C. and R.C.C.C. conceived the study and drafted the manuscript. Both authors reviewed the manuscript.

## **Competing interests**

The authors declare no competing interests.

# **Additional information**

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