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Characterize the switching performance of a superconducting nanowire cryotron for reading superconducting nanowire single photon detectors

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Scalable superconducting nanowire single photon detector (SNSPDs) arrays require cryogenic digital circuits for multiplexing the output detection pulses. Among existing superconducting digital devices, superconducting nanowire cryotron (nTron) is a three-terminal device with an ultra-compact size, which is promising for large scale monolithic integration. In this report, in order to evaluate the potential and possibility of using nTrons for reading and digitizing SNSPD signals, we characterized the grey zone, speed, timing jitter and power dissipation of a proper designed nTron. With a DC bias on the gate, the nTron can be triggered by a few μA high and nanoseconds wide input signal, showing the nTron was capable of reading an SNSPD pulse at the same signal level. The timing jitter depended on the input signal level. For a 20 μA high and 5 ns wide input pulse, the timing jitter was 33.3 ps, while a typical SNSPD's jitter was around 50 ps. With removing the serial inductors and operating it in an AC bias mode. The nTron was demonstrated to be operated at a clock frequency of 615.4 MHz, which was faster than the maximum counting rate of a typical SNSPD. In additional, with a 50 Ω bias resistor and biased at 17.6 μA , the nTron had a total power dissipation of 19.7 nW. Although RSFQ circuits are faster than nTrons, for reading SNSPD or other detector arrays that demands less operation speed, our results suggest a digital circuit made from nTrons could be another promising alternative.

Superconducting nanowire cryotron (nTron) is a three-terminal device made from superconducting nanowires and it is capable of building superconducting digital circuits¹. It has several advantages, such as ultra-compact size, large fan-out number, and insensitiveness to magnetic noise. In particular, an nTron has large output impedance and can drive a CMOS transistor directly². It also has been demonstrated that an SFQ pulse can trigger an nTron, so does the output from a superconducting nanowire single-photon detector (SNSPD)^{1,2}. Besides, nTrons have been used in some hybrid cryogenic circuits, such as driving a CMOS memory³, and driving LEDs in a photonic neuromorphic computer⁴.

The interfacing performance of the nTrons is well utilized, suggesting that nTrons are promising in reading signals from superconducting detectors. Although a RSFQ can have clock frequency up to 100 GHz, most superconducting detectors are much slower. Thus, the speed of SFQ circuits are not fully taken advantage of. For example, the SNSPD is single photon counting detector and its counting rate is typically less than 100 million counts per second⁵. Moreover, in an SFQ circuit, any input signal has to be digitalized to SFQ pulses before logic processing, and any output SFQ pulse has to be amplified to a level that room temperature electronics can read. For a superconducting computer, this signal incompatibility is not a severe problem since the amount of digital processing is heavy and most signals could be exchanged inside an SFQ chip. However, for other applications where non-SFQ signals are massively received and the amount of digital processing is moderate, for instance, a digital readout circuit for a superconducting detector array, signal-conversion circuits use much resources^{6,7}.

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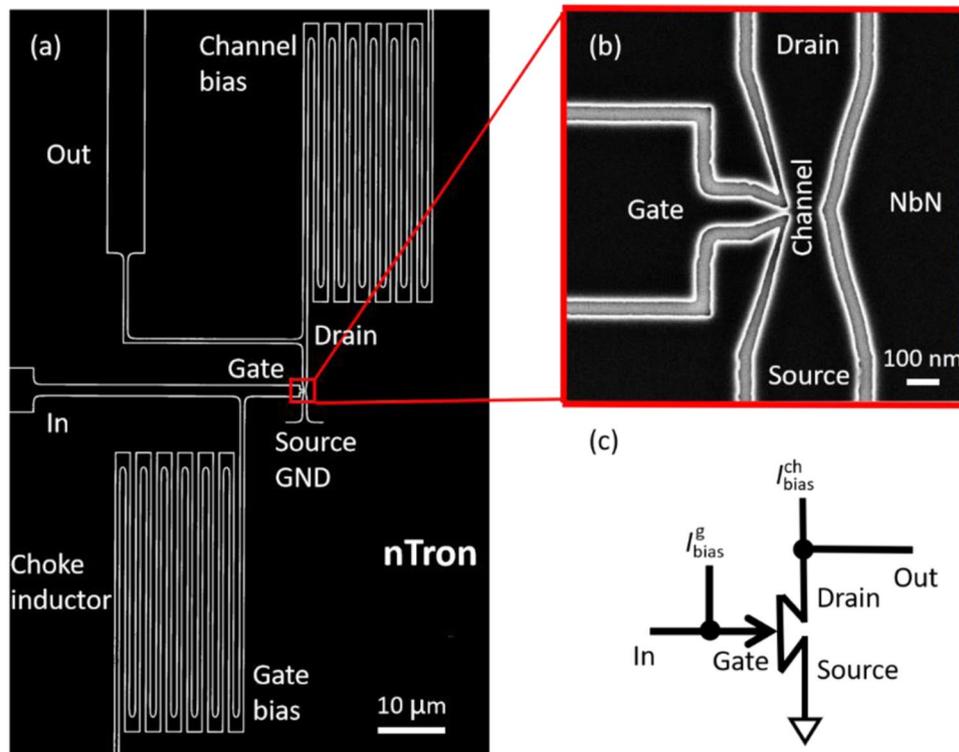


Figure 1. (a) Scanning electron microscope image of a typical nTron. An enlarged view of the choke area is shown in (b). (c) An equivalent circuit diagram for an nTron.

Therefore, although nTrons are relatively slower than RSFQ circuits, we think they are promising in reading superconducting detectors, in particular for SNSPDs. Recently, developing large SNSPD arrays is a challenge, where a scalable and power efficient cryogenic signal readout is the key technology. Although some multiplexing readout schemes based on time domain or frequency domain have been demonstrated for reading moderate sized SNSPD arrays^{8–10}, a focal plane detector array integrated with a compact and low power dissipation cryogenic readout circuit would be a solution for achieving large scale SNSPD arrays. Since an nTron is also a superconducting nanowire device, it uses the same fabrication processes and can be integrated on a single chip with SNSPDs. Moreover, the switching area of an nTron is confined in a choke so that the integration with an nTron readout circuit can be very compact.

In this report, we proposed an nTron geometry and characterized its grey zone, speed, timing jitter and power dissipation. The experimental results are compared with the signal requirements of a typical SNSPD for evaluating the potential and possibility of using nTrons for reading and digitizing SNSPD signals. We also discussed tradeoffs between these parameters, from which the scalability, cooling budget, operation speed, etc. of a potential nTron digital circuit could be derived.

nTron Geometry

The nTrons were patterned from a ~10 nm-thick niobium nitride (NbN) film deposited on a thermal oxide silicon substrate. As shown in Fig. 1(a), it had a gate input port, a gate bias port, a channel output port, and a channel bias port. We fabricated devices of different geometries. To focus on the purpose of reading SNSPDs, in this paper the device analyzed was optimized in width and shape as shown in Fig. 1(a). Because a typical SNSPD made from SNSPDs has a width of 100 nm and a corresponding output current of 10~20 μA , we designed the width of the gate nanowire into 50 nm, which came out to be ~20 nm after fabrication. The width of the channel nanowire was chosen to be 100 nm considering the tradeoff between the sensitivity and gain. To maximize the current density around the choke area to let the nTron be triggered sensitively, as the SEM picture shown in Fig. 1(b), the channel was patterned into a bow tie shape. The widths and shape were fixed for the nTrons analyzed in this paper. The devices that had less fabrication constrictions and high critical currents were selected from current-voltage measurements and then chosen for switching measurements.

In this report, we characterized two nTron devices. Both of them used the same geometry. But one nTron had serial bias inductors and the other one had not. For the nTron used in grey zone measurements, the corresponding critical currents were 8.6 μA and 52.0 μA measured at liquid helium temperature. The meandered nanowires connected in series on the gate bias port and channel bias port acted as choke inductors to separate DC bias and RF output. Each bias port was connected in series with a 17.2 k Ω off-chip resistor.

In the pulse measurements, we used an nTron without the serial inductors to minimize the overall inductance and replaced the bias resistors by 50 Ω resistors so that fast pulses can be applied with minimum reflections. The fast nTron was fabricated on a thinner film. Therefore, the gate critical current reduced to 6.0 μA and the channel

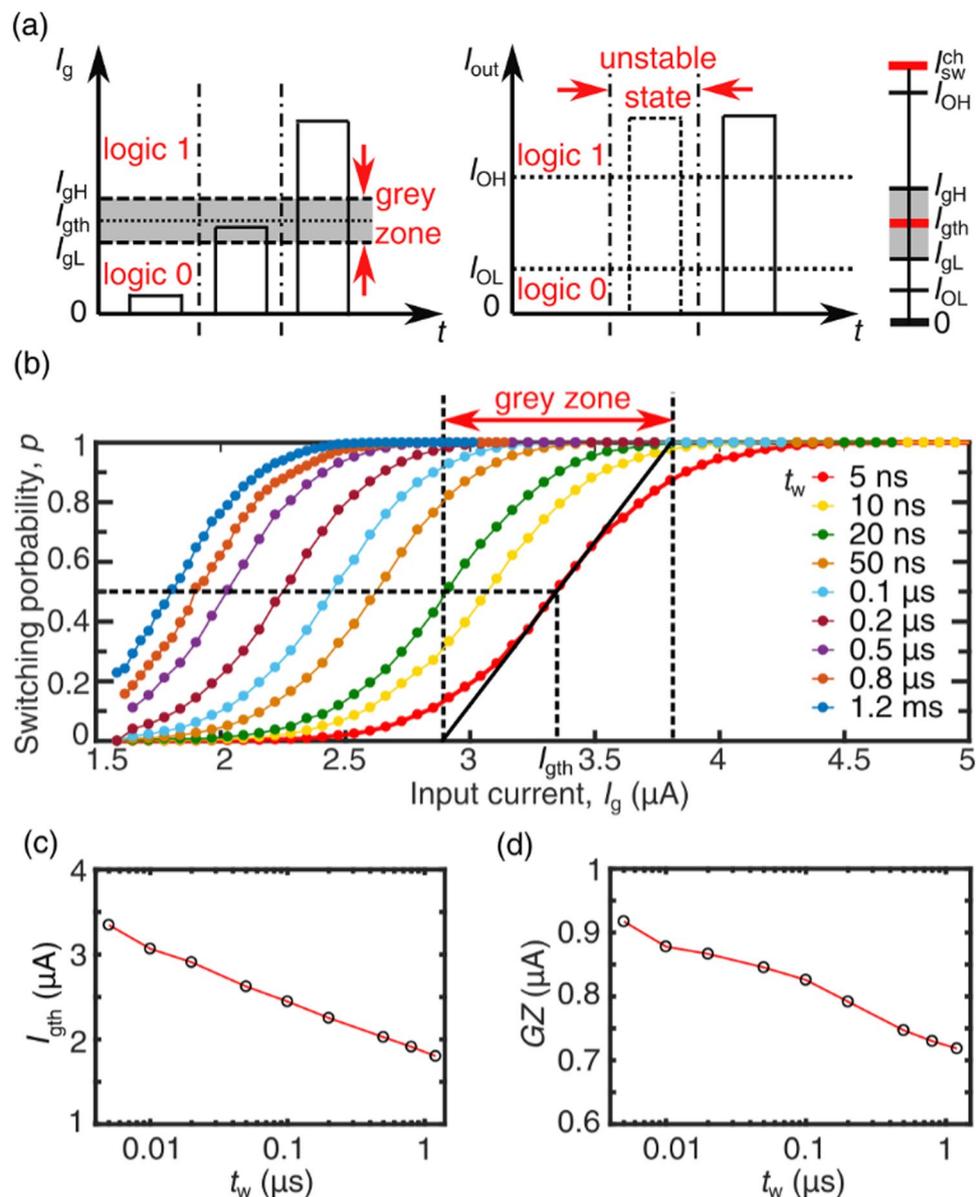


Figure 2. (a) A conceptual diagram to show the transient response of an nTron for different input currents, from which logic levels and grey zone can be visualized. The right bar shows logic values for an nTron. I_{sw}^{ch} is the switching current of the channel, defining the maximum output current. I_{OH} and I_{OL} are the high logic level and low logic level for output, while I_{gH} and I_{gL} are the high logic level and low logic level for gate input. (b) Switching probability of the nTron versus the input current I_g at different pulse widths t_w , while the channel bias and gate bias were fixed. (c) Threshold currents I_{gth} versus t_w . (d) Grey zone values GZ versus t_w .

critical current was $21.9 \mu A$. The input port and the output port each connected in series with an external 50Ω resistor on a PCB to match the impedance of 50Ω coaxial cables.

A circuit schematic diagram of the nTron is shown in Fig. 1(c), showing the bias, input and output ports. It is noticeable that, because the nTron has high output impedance, its output pulse can be read out directly after a room-temperature amplifier. Thus, we can prepare input pulses and get output signals off the nTron chip, enabling convenient characterizations without building another amplification stage.

Threshold Currents, Grey Zone and Gain

An nTron operates like a digital comparator when it is used to read out SNSPD pulses. Since an nTron has current gain, it will amplify the SNSPD pulse into a large output pulse. We can take SNSPD pulse as digital input as well. When nTrons are used in building digital circuits, the switching behavior determines the logic levels and bias margin. As shown in Fig. 2(a), the minimum amplitude of the input current pulse for triggering an nTron channel I_{gH} defines the lower level for the input logic 1, while the maximum amplitude of the input current pulse for not triggering an nTron channel I_{gL} defines the upper level for the input logic 0. Between I_{gL} and I_{gH} , there is an unstable region where an nTron switching stochastically due to thermal and quantum fluctuations¹¹. This unstable

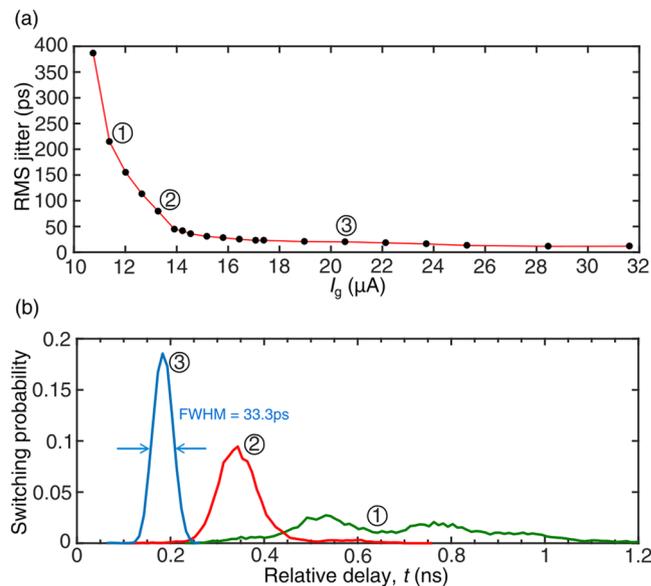


Figure 3. (a) The RMS Jitter vs. the input pulse amplitude I_g . The pulse width was fixed at 5 ns. (b) Switching probability normalized to the total counts at three different input levels marked at (a) for $I_g = 11.4 \mu\text{A}$, $13.3 \mu\text{A}$ and $20.6 \mu\text{A}$.

region is referred to as grey zone¹². Figure 2(b) shows the switching probabilities for the input pulse width t_w varying from 5 ns to 1.2 μs . For each point, we sent $N_{\text{in}} = 5 \times 10^5$ pulses to the gate and counted the number of switched pulses N_{tr} . The switching probability was defined as $N_{\text{tr}}/N_{\text{in}}$. The channel bias was $I_{\text{bias}}^{\text{ch}} = 43.0 \mu\text{A}$ and the gate bias was $I_{\text{bias}}^g = 5.8 \mu\text{A}$. We defined the pulse amplitude at switching probability $p = 0.5$ as the input threshold currents I_{gth} . The grey zone of GZ was defined as $GZ = 1/\rho$ where ρ was the slope of the switching probability curve at the input pulse amplitude equal to I_{gth} .

With data shown in Fig. 2(b), we can extract the dependences of I_{gth} and GZ on input pulse width. As shown in Fig. 2(c), a shorter input pulse required a higher I_{gth} . As an nTron channel's output impedance was much higher than a typical 50Ω load, the output current was proportional to its initial bias. With ignoring the leakage current through the channel, we can have the current gain of the nTron, which was $G = \frac{I_{\text{bias}}^{\text{ch}}}{I_{\text{gth}}}$. Therefore, a shorter gate input pulse also resulted in a lower current gain and thus a lower fan-out number. At $t_w = 5$ ns, corresponding to a frequency of 200 MHz, G was 13.0. With a wider pulse, for instance, $1/t_w = 833$ kHz, G increased to 23.9. We noticed that the GZ had a similar dependence on t_w . Because there was noise adding on input pulses, when a wider pulse was applied, it was more likely to trigger an nTron, resulting in a narrower transition of the switching probability curve and a lower GZ value. Similar to what have been done on JJs, we can model the nTron switching dynamics with taking into account an energy barrier for escaping¹¹.

Timing Jitter

Low timing jitter is one of SNSPD's advantages. Depending on the geometry, output signal-to-noise ratio, biasing current et. al, the timing jitter defined at full-width-at-half-magnitude varies from 3 ps to ~ 50 ps^{13,14}. Thus, an nTron should have intrinsic low timing jitter so that the low timing jitter of an SNSPD read after an nTron digital circuit can be maintained. To study the switching jitter of the nTron shown in Fig. 1(a), we sent a 5 ns wide pulse into the nTron gate with varying the pulse amplitude and collected the delay between the input pulse and the nTron output pulse. The channel bias was $I_{\text{bias}}^{\text{ch}} = 43.5 \mu\text{A}$ and the gate bias was removed. Since the delay distributions were not all in a Gaussian shape, we used the root-mean-square value of the delay to define the RMS jitter. For each data point, more than 10^4 pulses were collected by a high-speed oscilloscope for calculating the statistic values.

Figure 3(a) indicates the switching jitters for the input pulse amplitude varying from $10.7 \mu\text{A}$ to $31.6 \mu\text{A}$. There was a clear decay of the jitter for a higher input pulse. As the current of input pulse increased, the jitter of an nTron tended to be stable. For instance, the RMS jitter at input pulse of $20.6 \mu\text{A}$ was 33.3 ps. We also observed the trigger delay became shorter for a higher input pulse. As shown in Fig. 3(b), when the input pulse increased from $13.3 \mu\text{A}$ to $20.6 \mu\text{A}$, there was a 160 ps shift of the delay distribution. The profile of the delay distribution for high input pulses showed a Gaussian shape, while for low input pulse the distribution became wider and had multiple peaks, indicating a complex switching dynamics.

Both the timing jitter and the grey zone measurements indicated that the switching of an nTron started from probabilistic to deterministic as the input pulse increased. To understand such behavior of nTron needed a switching dynamic model with taking account fluctuations. In the first paper of nTron published in ref.¹, Adam McCaughan and Karl Berggren suggested a 2D electro-thermal model, which could be used to simulate the switching dynamics for nTrons of different geometries. Since the nTron gate was 20 nm while the coherent length

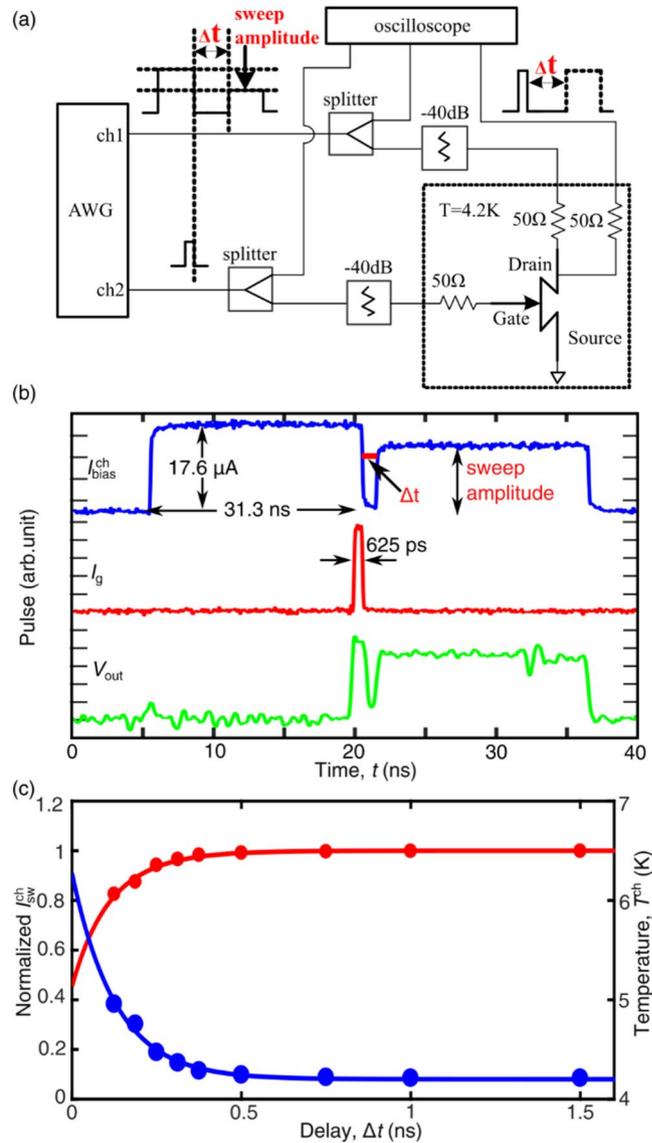


Figure 4. (a) Circuit diagram of the speed measurement setup. (b) Waveforms (blue for channel bias pulse; red for gate input pulse; green for output voltage pulse) for measuring the recovery time of an nTron. The nTron was fired at the first bias pulse. After a delay Δt a second bias pulse was used to measure the time-dependent switching current of the channel $I_{sw}^{ch}(\Delta t)$. (c) Recovery of I_{sw}^{ch} normalized to the static value $I_{sw}^{ch}(4.2\text{ K})$ (red trace) and recovery of the derived channel temperature T^{ch} (blue trace).

of NbN was about 10 nm, phase slippage and vortex dynamics in a nanowire can happen before a stable resistive domain was generated, which could be the sources for introducing wider grey zone and larger time jitter¹⁵. Based on the experimental results we have now, we cannot conclude a precise switching model for nTrons. However, the measured current threshold and timing jitter of the proposed nTron geometry can meet the requirement for reading an SNSPD-like pulse, i.e. 5 ns wide and 20 μA high.

Operation Speed and Power Dissipation

The grey zone measurements showed that the nTron can be triggered by nanoseconds wide pulses, implying a possible operation speed of hundreds of MHz. To have a better characterization of the operation speed, i.e. the maximum clock frequency, of an nTron digital circuit, we measured the recovery time of a fast nTron. As nTrons were made from NbN nanowires, which had high kinetic inductance, current charging and discharging caused an electrical recovery time¹⁶. To reduce the electric recovery time, we removed the serial inductors on the bias ports, and shortened the nanowire to have less inductance. When nTrons were integrated on a single chip, connection length can be further reduced to speed up the electric recovery.

Another recovery time was from thermal relaxation of the local hotspot generated on a fired nTron. The hotspot was a resistive area where the local Joule heating increased the hotspot temperature. The power of input pulse

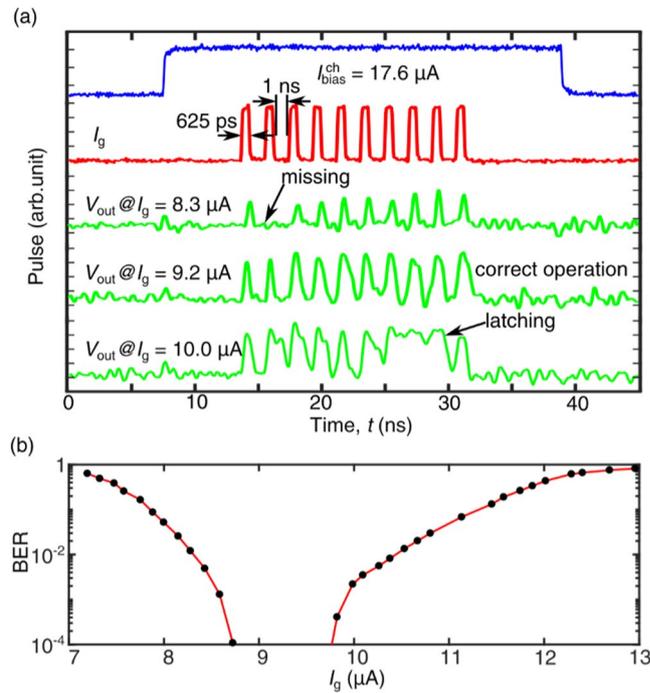


Figure 5. (a) Waveforms for operating the nTron at ten successive input pulses (red trace). The channel was biased with a long pulse (blue trace). The green traces are the output voltage pulses at three different inputs ($I_g = 8.3 \mu\text{A}$, $9.2 \mu\text{A}$ and $10.0 \mu\text{A}$). (b) The bit error rate (BER) versus the input pulse amplitude I_g .

can control the hotspot size and temperature. Thus, there was a tradeoff between the input signal power and the recovery time (i.e. the speed of nTron).

To measure the thermal recovery time of an nTron, we implemented a pump-probe like measurement. As shown in Fig. 4(a,b), two bias pulses with a varied delay Δt were sent to the nTron channel. The first bias pulse was 31.0 ns wide and $17.6 \mu\text{A}$ high. A gate pulse, which was 625 ps wide, was sent to trigger the nTron at the first bias pulse. We aligned the bias pulse and the input pulse to make them drop to zero simultaneously. Then, we sent a second channel bias pulse and swept its amplitude to find the switching current of the nTron channel of $I_{\text{sw}}^{\text{ch}}(\Delta t)$ as a function of Δt . As we connected a 50Ω resistor to the nTron gate to match the impedance of the coaxial cable, the input power sending to the nTron was $P_{\text{in}} = I_g^2 R$, where $R = 50 \Omega$. Before the gate nanowire switched, the input power was dissipated mostly on the resistor. Once the gate nanowire switched into a normal resistor, the gate impedance increased much higher than 50Ω . Thus, most power was dissipated on the nTron gate. Although some power was reflected, making the measurement of actual power dissipation of the gate nanowire difficult, by adjusting P_{in} we can control the maximum temperature that the gate nanowire reached after a switch, as shown in Fig. 4(c). The input power to the channel wire was calculated by the same method.

Figure 4(c) shows the recovery time of the nTron's channel switching current after a switching. We converted $I_{\text{sw}}^{\text{ch}}(\Delta t)$ to $T^{\text{ch}}(\Delta t)$ by solving Eq. (1)¹⁷, where T^{ch} was defined as an effective temperature of the channel with assuming a uniform temperature profile of the normal region of the channel.

$$I_{\text{sw}}^{\text{ch}} = I_{\text{c0}}^{\text{ch}} \left[1 - \left(\frac{T^{\text{ch}}}{T_c} \right)^2 \right]^{3/2} \left[1 + \left(\frac{T^{\text{ch}}}{T_c} \right)^2 \right]^{1/2}. \quad (1)$$

In Eq. (1), $T_c = 8.1 \text{ K}$ was the critical temperature of the NbN film and $I_{\text{c0}}^{\text{ch}} = 31.1 \mu\text{A}$ was the calculated critical current of the nTron channel at zero temperature. We fitted the data with an exponential decay $T^{\text{ch}} = T_{\text{max}} e^{-t/\tau_R}$, where T_{max} was the maximum temperature at which T^{ch} started to drop and τ_R was the thermal relaxation time constant. When the input pulse current was $31.3 \mu\text{A}$ and the corresponding input power P_g was 48.9 nW , the calculated T_{max} was 6.3 K and the fitting thermal relaxation time τ_R was 0.13 ns .

From the above analyses, there was a tradeoff between the operation speed and the input power dissipation. If the input signal was high, although an nTron can be switched deterministically with low timing jitter, the nTron was heated up and needed a longer time for cooling, limiting the operation speed. If input pulses came with an interval time shorter than the relaxation time or the channel current recharged faster than the relaxation time, an nTron would latch. As shown in Fig. 5(a), we biased the nTron channel at $17.6 \mu\text{A}$ ($0.8 I_{\text{sw}}^{\text{ch}}$) and sent 10 successive input pulses at a frequency of 615.4 MHz . When the pulse amplitude I_g was too low, the nTron was not able to fire determinately and a few output pulses were missing. Nevertheless, if I_g was too high, we noticed that the output pulse sometimes latched because previous thermal relaxations had not fully completed. When I_g was set at a

proper level, individual output pulses corresponding to each input pulse can be obtained. In Fig. 5(b), for each point, we collected 100k pulses and calculated the probability of errors. The Proper level of I_g can be gained when the bit error rate (BER) calculated by the number of nTron output pulses divided by the total input pulse number was less than 10^{-4} . We swept I_g and measured the bit error rate (BER) of the nTron output. As shown in Fig. 5(b), the margin of I_g for correct operations reduced to $\sim 1 \mu\text{A}$ although the operation speed increased to 615.4 MHz and the gate input power was $P_g = 4.2 \text{ nW}$ at $I_g = 9.2 \mu\text{A}$. The channel was biased at 17.6 μA through a 50 Ω resistor. Thus, the input power to the channel wire was 15.5 nW. The total power sending to the nTron was 19.7 nW.

Conclusions

In conclusion, we investigated the threshold currents, grey zone, speed and power dissipation of a typical nTron made from NbN films and measured at 4.2 K. We found those parameters related closely to each other and tradeoffs between them occurred. Experimentally, we demonstrated an nTron can be operated at a speed of 615.4 MHz with an input gate current of 9.2 μA and a total input power of 19.7 nW. The switching timing jitter of an nTron, included the measurement jitter caused by voltage noise, was 33.3 ps at a 5 ns wide and 20.6 μA high input pulse. Although the nTron's performance are less superior to JJs in an advanced RSFQ circuit, the nTron we characterized in this work is faster enough to read a relatively slow superconducting detector, for instance an SNSPD that usually have a maximum counting rate less than 100 Mcps¹⁸. The nTron's power dissipation is better than a cryogenic CMOS transistor, which usually dissipated mW power¹⁹. Thus, a mW cooling power could afford ~ 50 thousand nTrons, carrying out many digital circuits, e.g. a binary-coded decimal encoder or a counter.

It is worth to notice that the performance of an nTron depends on their design and geometry. If the size of the gate is much smaller, the gate critical current reduces so that the gate can be triggered at a low input current. Then, as the gate is narrow and thin, the local temperature of gate is higher with the same power dissipation on the gate. Meanwhile, an nTron made on substrates of high thermal conductivity, i.e. sapphire and MgO, will exhibit faster operation speed due to the short thermal recovery time. An nTron of wider channel can output more current, but the threshold current will increase as well. Understanding those dependences needs to study non-equilibrium dynamics of a superconducting nanowire, which is out of the scope of this work. Once the design of an nTron is made, characterization methods presented in work can be used for extracting its switching performance.

Recent works demonstrate that an nTron can be operated in a flux regime similar to shunted Josephson Junctions if we prevent the nanowire from heating to a hotspot^{20–22}. This could give an nTron a considerable improvement in speed and power dissipation. However, as we mentioned in the introduction, an nTron operated in hotspot regime has its own advantages and is promising in certain digital applications. We wish the measured characteristics and tradeoffs shown in this letter can help researchers to design and utilize nTrons properly.

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Author contributions

Q.Z. and L.K. conceived and led the project. K.Z., L.D.K. and S.C. fabricated the samples. K.Z., H.L. and Q.Z. performed measurements. X.T. and L.Z. helped with e-beam lithography. X.J. helped NbN films. J.C. helped with cryogenic setup. Q.Z. and K.Z. wrote the manuscript. Q.Z., L.K. and P.W. supervised the work.

Competing interests

The authors declare no competing interests.

Additional information

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