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Border Trap Extraction with Capacitance- Equivalent Thickness to Reflect the Quantum Mechanical Effect on Atomic Layer Deposition High-*k*/$In_{0.53}Ga_{0.47}As$ on 300-mm Si Substrate

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This study presents a model to calculate the border trap density (N_{bt}) of atomic layer deposition high-*k* onto $In_{0.53}Ga_{0.47}As$ on a 300-mm (001) Si substrate. This model considers the quantum confinement effect and band nonparabolicity. Capacitance-equivalent thickness (CET) was used to reflect the distance of the charge centroid from the oxide–semiconductor interface. The border trap values based on CET were found to be approximately 65% lower than the extracted values based on physical thickness in the $In_{0.53}Ga_{0.47}As$ material. In an investigation of two different post-metal annealing effects on border traps, the border trap was more effectively passivated by N_2-based forming gas annealing (FGA) compared with rapid thermal annealing (RTA), whereas a lower interface state density was observed in RTA-annealed samples compared with FGA-annealed samples. N_{bt} extraction at different bias voltages demonstrated that the applied frequencies travel deep into the oxide and interact with more traps as more the Fermi level passes the conduction band, thus creating tunneling with the carriers.

As a substitute for conventional SiO_2/n-type Si metal-oxide-semiconductor field-effect-transistors (MOSFETs), the combination of different higher dielectric constant (k) oxides along with $In_xGa_{1-x}As$ ($x > 0.5$) as a channel material has been extensively investigated for its potential equivalent oxide thickness (EOT) scaling and use in forthcoming logic-applicable devices that will require high-speed and depressed power consumption[1–5]. Among the different high dielectric constant (k) oxides, studies on Al_2O_3, HfO_2, La_2O_3, ZrO_2, and their nanolaminate and nano-mixture structures have already been reported[6–11].

$In_{0.53}Ga_{0.47}As$ is often used instead of silicon because of its high electron mobility, which results from its lower effective mass of electrons. However, because of this lower effective mass of electrons, $In_{0.53}Ga_{0.47}As$ suffers from low density of states (DOS)[12]. To be more precise, the DOS of $In_{0.53}Ga_{0.47}As$ is less than that of Si by approximately two order of magnitudes[13,14]. As a result, this insufficient DOS causes the Fermi level of $In_{0.53}Ga_{0.47}As$ to move inside the conduction band; otherwise, the benefit of its high mobility would be lost[4]. The band offset of high-k and $In_{0.53}Ga_{0.47}As$ substrate is comparatively smaller than that of a conventional SiO_2/Si interface.

Once the fermi level, E_F, has biased near the conduction band, the effective barrier height between the oxide and $In_{0.53}Ga_{0.47}As$, which is denoted as $E_{ox} - E_F$, is reduced. As a result, the trap inside the oxide starts the charge/discharge process with electrons from the semiconductor through tunneling[14]. These traps, which are positioned in the dielectric near the oxide–$In_{0.53}Ga_{0.47}As$ interface, are commonly known as *border traps*[15–17]. The idea of these traps was first introduced by Fleetwood[15]. Border traps are characterized by their location: the farther they are from the interface, the longer it takes for the majority carrier to fill them. Their charge exchange

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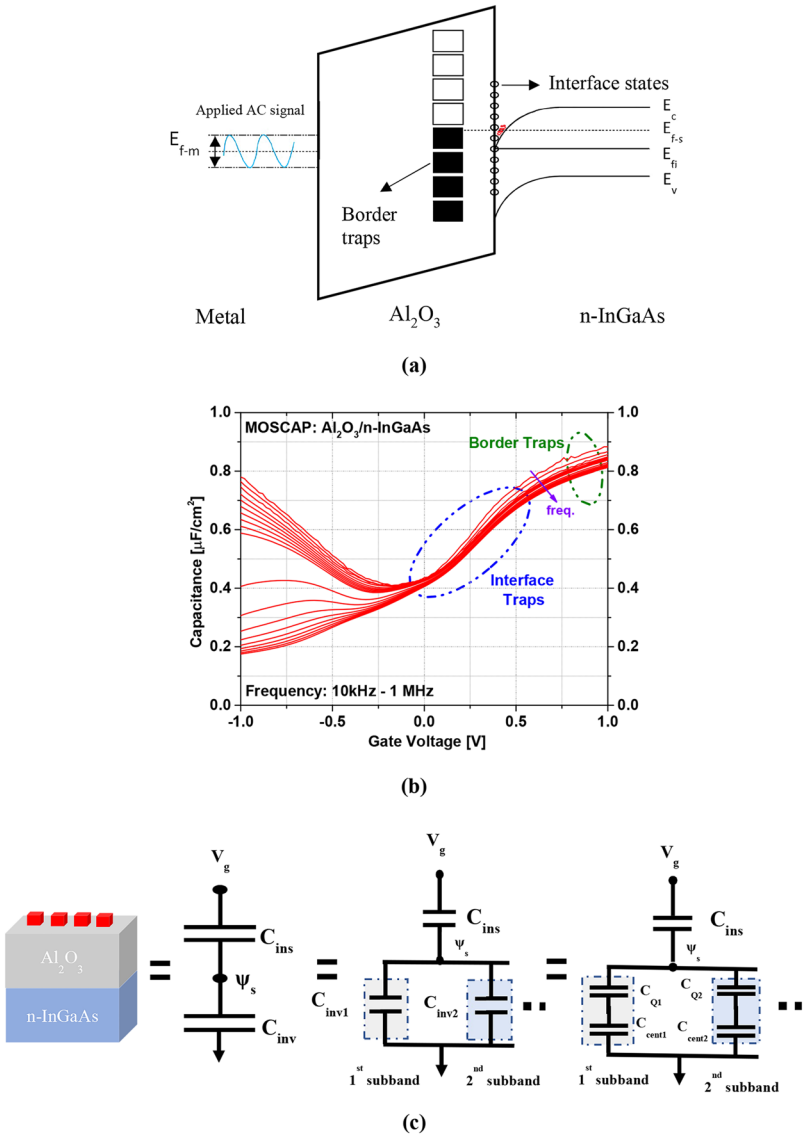

Figure 1. (**a**) Energy-band diagram of a metal/Al_2O_3/n-InGaAs MOS capacitor with the interface and border traps when an AC signal is applied. (**b**) Response regions of the interface and border traps in the capacitance-voltage (C-V) behavior of the Al_2O_3/n-InGaAs MOS capacitor. (**c**) Equivalent circuit diagram for the gate capacitance of the III–V MOSFET.

is also determined by the applied alternating current (ac) frequency. A lower frequency provides deep tunneling by decreasing the apparent thickness of the oxide, whereas the tunneling probability decreases at a higher frequency[16].

Figure 1a shows how the tunneling of electrons occurs from the semiconductor to oxide layer in response to an applied AC frequency with sufficient direct current (DC) bias voltage. However, the effect of these near-interfacial dielectric traps is a great stimulus for the on-state act of a MOSFET. Because the fermi level (E_F) is pinned inside the conduction band, border traps prevent the formation of sufficient carriers in the channel, which leads to reduced carrier mobility by phonon scattering and eccentricity of the threshold voltage[17,18]. These traps are also responsible for reduction of gate voltage control on the channel current, enhancing gate leakage current, a degradation of transconductance as well as for hysteresis[19,20]. The impact of border traps is more prominent in the accumulation region, where a dispersion is always observed in the capacitance-voltage (C-V) response of the metal-oxide-semiconductor (MOS) capacitor because of the transportable carrier exchange among the border traps and conduction band states via tunneling, as described previously[21–24].

Figure 1b illustrates the region where border traps are prominent as an active trap state in capacitance-voltage (C-V) with a frequency dependency from 10 kHz to 1 MHz. Unlikely, the typical interface state model cannot explain this dispersion because the time constant of these traps at accumulation is much smaller than that of the bulk oxide traps, within the typical measurement frequency range from 1 kHz to 1 MHz[25]. The electrical behavior of border traps is quite different from that of interface traps in several ways. Firstly, the interface traps are inactive

at the energy value of the accumulation region, where the frequency scattering occurs[22]. Secondly, compared with the time constant that is responsible for the interface trap's charging/discharging, the dispersion performance is less temperature dependent because of the border traps[26]. Finally, the chemical treatment has no effect on border traps but successfully diminishes the dispersion caused by interface traps[27].

Researchers have proposed several methods for modelling the dispersion of capacitance at accumulation and making electrical characterizations of border traps[22–25,28–31]. Among them, the distributed border trap model from Yuan *et al.* is the most well known[28,31]. In this model, the oxide thickness (t_{ox}) is segregated into immeasurable quantities of small fragments, with each part contributing an amount of oxide capacitance, ΔC_{ox}, connected in parallel with the admittance proportional to the border trap density; this parallel combination is connected in series with the semiconductor capacitance. The border trap density is then extracted by making a best-fit condition between the calculated capacitance and the conductance achieved from this model and experimental values. Usually, this oxide thickness is mainly the physical thickness (t_{ox}) or EOT, which is the result of either ellipsometry or transmission electron microscopy analysis.

When determining the semiconductor capacitance C_s, it is not clear that previous studies' consideration about the quantum mechanical effect[12,25,32–34]. For practical purposes, this capacitance is not only the oxide capacitance but also a series combination of inversion capacitance (C_{inv}), which includes quantum capacitance (C_Q) and centroid capacitance (C_{cent}), by assuming that the first electron sub-band in the channel is occupied[35,36]. Therefore, the total capacitance includes a series combination of insulator capacitance (C_{ins}), quantum capacitance (C_Q), and centroid capacitance (C_{cent}). The equivalent electrical circuit is shown in Fig. 1c. In a large-scale device, the series combination of C_Q and C_{cent} is larger than C_{ox}, so the gate capacitance approaches only C_{ox}. However, in small-scale devices, the oxide thickness is on a nanometer scale; thus, C_{ox} becomes commensurate with the other components of total capacitance[35].

Quantum capacitance (C_Q), which is proportional to the DOS of the channel material, physically originates from the Fermi-level penetration onto the conduction band. In the III–V channel material, a two-dimensional electron gas requires energy to be created in the semiconductor quantum well region because of low density-of-states (DOS). Therefore, the Fermi level moves above the conduction band to increase the charge in the quantum well. This movement requires energy and conceptually is equivalent to quantum capacitance. However, charges in the quantum well take a bell-shaped distribution rather than distributing themselves in a sheet form with zero thickness, which means that the physical distance of each charge is quite different from the metal gate. Moreover, the center of the charge distribution may be away from the insulator–semiconductor interface due to the confinement in the quantum well. These effects should be considered when modelling the total capacitance. When these factors are excluded, the overall capacitance is overestimated, so the extracted border trap density (N_{bt}) is inaccurate[32]. To improve the extraction of border trap density, total semiconductor capacitance (C_s) should be included with the quantum confinement effect and band nonparabolicity in the model. Additionally, because of the quantum mechanical confinement consequence of the carriers, the supplementary thickness of the conductive channel should be considered because the charge centroid in the conductive channel is located deeper beneath the interface of the dielectric and semiconductor, as described previously[37].

Capacitance-equivalent thickness (CET) reflects a more realistic set-up because it considers the above-mentioned effect. Therefore, border trap extraction using a CET metric is a more reliable way to obtain the accurate density of border traps. In this study, we used the CET metric for the extraction of N_{bt} in addition to using physical thickness and determined that border trap density is overestimated when the quantum mechanical effect is not considered. In addition, because a border trap is an oxide's native property, the parameters of oxide growth from atomic layer deposition (ALD) must have some effects on border trap formation. In this regard, we also examined the effects of ALD growth temperature on border traps. Moreover, several studies have passivated border traps using a variety of annealing processes[33,38]. Thus, we also examined the passivating effects of two types of annealing processes on border traps. Lastly, the interface trap density (D_{it}) was also extracted for samples that were differentiated with the passivation scheme.

Model Description

Gate capacitance model. The total capacitance of III–V MOS structures is modelled as a series combination of insulator capacitance (C_{ins}) and inversion capacitance (C_{inv}) by assuming no doping level underneath the channel as demonstrated in Fig. 1c. It consists of a parallel combination of contributions of each occupied electron subband in the channel. From the figure it is evident that, for each subband *i*, the inversion-layer capacitance (C_{inv_i}) consists of the quantum capacitance (C_{Q_i}) and the centroid capacitance (C_{cent_i}) which are connected in series. So, inversion-layer capacitance can be defined as

$$C_{inv\_i} = \frac{\partial(-Q_s)}{\partial\psi_s} = \frac{q\partial(-Q_s)}{\partial(E_F - E_C)} \tag{1}$$

where, ψ_s is the surface potential, E_F is the fermi level, E_C is the conduction band edge at the barrier-channel interface on the channel side, and Q_s is the total electron charge in the channel which is the sum of all the charges in each of the sub bands. This can be formulated as

$$Q_s = \sum_i Q_i = \sum_i \int_{E_i}^{\infty} \frac{\frac{m_{||}^* q}{\pi\hbar^2}}{1 + exp\left(\frac{E - E_F}{kT}\right)} dE \tag{2}$$

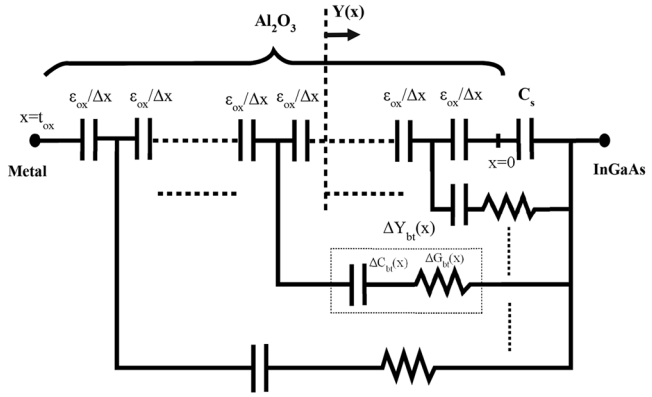

Figure 2. Equivalent electrical circuit representation of an MOS capacitor using the distributed bulk oxide trap model[28,31].

where, Q_i is the electron charge of subband *i* in the channel, E_i is the energy level of subband *i*, and $m_{\|}^*$ is the in plane effective mass of the channel material. The effective mass is a function of energy due to nonparabolicity of the band structure which can be expressed as follows[39].

$$m_{\|}^* = m_0^*(1 + \alpha E) = \frac{\hbar^2 k^2}{2E} \tag{3}$$

where, m_0^* is the effective mass at $k = 0$, E and k are the energy and wave number of the charge carrier, ħ is the reduced Plank's constant and α is the nonparabolicity parameter.

Now, we can define quantum capacitance for any subband (C_{Q_i}) as the derivative of electron charge in subband *i* with respect to energy difference between E_F and E_i. Mathematically,

$$C_{Q\_i} = \frac{q\partial(Q_i)}{\partial(E_F - E_i)} = \frac{q\partial\left(-\int_{E_i}^{\infty} \frac{\frac{m_{\|}^* q}{\pi\hbar^2}}{1 + exp\left(\frac{E - E_F}{kT}\right)} dE\right)}{\partial(E_F - E_i)} = \frac{\frac{m_{\|}^* q^2}{\pi\hbar^2}}{1 + exp\left(\frac{E_i - E_F}{kT}\right)}. \tag{4}$$

Similarly, centroid capacitance of subband *i* (C_{cent_i}) can be defined as the derivative of electron charge in subband *i* with respect to energy difference between E_i and E_C.

$$C_{cent\_i} = \frac{q\partial(-Q_i)}{\partial(E_i - E_C)} = C_{Q\_i} \cdot \frac{\partial(E_F - E_i)}{\partial(E_i - E_C)} \tag{5}$$

Then C_{inv_i} can be formulated as

$$C_{inv\_i} = \sum_i \left(\frac{1}{C_{Q\_i}} + \frac{1}{C_{cent\_i}}\right)^{-1} \tag{6}$$

So, if the location of each subband energy level (E_i) and the fermi level (E_F) are known with respect to conduction band edge, then all the capacitance component can be evaluated.

Border trap extraction model. For a quantitative analysis of border trap density, we followed the distributed border trap model as mentioned previously. This model enumerates the border traps by analyzing the frequency dispersion at an accumulation region at any specific bias voltages. The whole oxide capacitance is modelled onto an abundant number of small capacitive components, ΔC_{ox}, where each component characterizes the capacitance of a very small piece of oxide thickness. The induced charge storage and energy loss from the border traps are modelled by a series of connected capacitance (ΔC_{bt}) and conductance (ΔG_{bt}) for any portion of oxide thickness. This admittance due to border traps is connected in parallel to the oxide capacitance. This parallel combination is then connected in series with the semiconductor capacitance. Figure 2 shows the equivalent electrical circuit of the model. The whole model can be described by a first-order non-linear ordinary differential equation, as follows:

$$\frac{dY}{dx} = -\frac{Y^2}{j\omega\varepsilon_{ox}} + \frac{q^2 N_{bt} \ln(1 + j\omega\tau)}{\tau} \tag{7}$$

with the boundary condition at $x = 0$, $Y = j\omega C_s$ where Y is the total admittance at any distance *x* from the oxide–semiconductor interface; $\omega = 2\pi f$ is the angular ac frequency, where *f* is the measurement frequency and C_s is the semiconductor capacitance corresponding to a specific surface potential ψ_s.

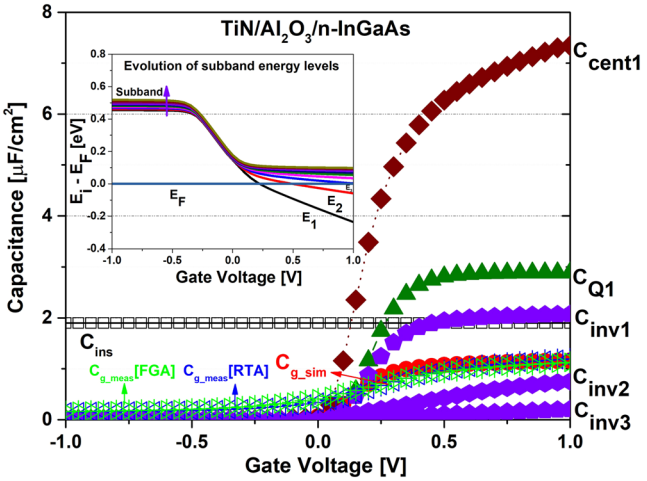

Figure 3. Evolution of sub-band energy levels with respect to Fermi level (inset), experimental C_g, and modeled C_g components of an ALD-processed sample.

The other important parameters of this model are described as follows: q is the elementary electron charge in Coulombs; $\varepsilon_{ox} = \varepsilon_r \cdot \varepsilon_0$ is the permittivity of any dielectric film, where ε_r is the relative permittivity of the oxide layer and ε_0 is the permittivity of the air; C_{ox} is the oxide capacitance per cm^2, which is defined as ε_{ox}/t_{ox}, where t_{ox} is the thickness of the oxide layer in centimeters; N_{bt} is the volume concentration of border traps in the oxide at a distance x from the oxide–semiconductor interface at any energy level, expressed as eV^{-1} cm^{-3}; and τ is the average time in seconds for electron capturing of an empty trap. τ maintains an exponential relationship with the distance x, which is the distance of the trap within the oxide from the interface. τ can be described as follows:

$$\tau = \tau_o e^{2kx} \; with \; k = \frac{\sqrt{2m * E_b}}{\hbar} \tag{8}$$

Here, τ_0 is the capture/emission time constant of the trap having the same energy level of τ. k is the attenuation coefficient of the tunneling process, which can be described by the effective mass of dielectric film (m*), the barrier height between the conduction band of oxide and semiconductor (E_b), and the reduced Plank's constant (ħ). Moreover, τ_0 can be described more specifically as:

$$\tau_o = (n_s v_{th} \sigma)^{-1} \tag{9}$$

Here, v_{th} is the thermal velocity of any electron at any temperature T, n_s is the semiconductor surface's electron density, and σ is the border trap's capture cross-sectional area. As described elsewhere[13], at the accumulation region where the Fermi level is near the conduction band, a good approximation is to consider n_s as equal to the DOS (N_c) of the conduction band. Moreover, the border traps that are deeply inside of the oxide do not respond at any applied frequency ω having a time constant τ that is greater than $1/\omega$; however, the traps closer to the interface with a smaller τ are more willing to respond. Using the condition $\omega\tau = 1$, the probing depth at any applied frequency for a border trap can be calculated as follows:

$$X_p = \frac{1}{2k} \ln \frac{1}{2\pi f \tau_o} \tag{10}$$

Here, f is the measurement frequency.

Results and Discussion

Figure 3 shows the evolution of the sub-band energy levels and all capacitance component modelling, along with experimental data from an Al_2O_3 ALD-deposited sample. For our modelling, we solved the self-consistent solution of the one-dimensional Poisson and Schrodinger equations using the Nextnano simulation tool[40]. This tool provides the values of sub-band energy (E_i) and conduction band energy (E_C) with respect to the fermi level energy (E_F). The inset of Fig. 3 shows the evolution of the sub-band energy levels (E_i) with respect to the fermi level (E_F) at the applied bias voltage range. From the figure, it is evident that the fermi level penetrates the first and second energy levels while being very close to the third energy level. Thus, both the first and second sub-bands of the quantum well are populated by electrons in the operational voltage range.

Figure 3 also illustrates the measured capacitance of rapid thermal annealing (RTA) and forming gas annealing (FGA)-processed samples with modelled gate capacitance and its components. The model extraction was done by considering the conduction band effective mass of $In_{.53}Ga_{.47}As$ to be $0.043m_0$ (m_0 = electron mass at rest) by considering a non-parabolicity effect as reported in literature[41] as well as optimizing other material parameters according to their physical structures[13]. The extracted gate capacitances were well harmonized with the modelled data. The insulator capacitance was calculated by considering the ideal dielectric constant (k), which is 9, and the measured oxide thickness. However, in the experimental cases, the gate capacitance approached approximately

Sample	RTA-Processed Samples			FGA-Processed Samples		
Parameter	200 °C	250 °C	300 °C	200 °C	250 °C	300 °C
t_{ox} [nm]	4.2006	3.867	3.5128	4.2006	3.867	3.5128
CET [nm]	2.67	2.469	2.31	2.95	2.62	2.4
ε_r	6.93	6.71	6.26	5.87	6.24	6.07
m*	0.23	0.23	0.23	0.23	0.23	0.23
E_b [eV]	3.65	3.65	3.65	3.65	3.65	3.65
k [nm^{-1}]	4.5	4.5	4.5	4.5	4.5	4.5
C_s [$\mu F/cm^2$]	1.08	1.143	1.22	1.08	1.143	1.22
τ_0 [s] (Using t_{ox})	1×10^{-11}	1×10^{-12}	1×10^{-12}	1×10^{-12}	1×10^{-12}	1×10^{-13}
τ_0 [s] (Using CET)	3×10^{-11}	1×10^{-11}	1×10^{-12}	1×10^{-12}	1×10^{-11}	1×10^{-13}
N_{bt} [$cm^{-3}\,eV^{-1}$] (Using t_{ox})	1.28×10^{20}	1.1×10^{20}	1×10^{20}	9.6×10^{19}	9.75×10^{19}	7.6×10^{19}
N_{bt} [$cm^{-3}\,eV^{-1}$] (Using CET)	4×10^{19}	4.1×10^{19}	3.09×10^{19}	2.98×10^{19}	3.58×10^{19}	2.72×10^{19}

Table 1. Summary of parameters used for the extraction of border trap density.

63% of C_{ins} for the RTA-processed sample. The same condition is also valid for FGA processed samples as depicted in the Fig. 3. This capacitance deprivation mostly results from the effects of inversion capacitance. As demonstrated, C_{inv1} is quite comparable with the insulator capacitance; in addition, C_{Q1} is more dominant than C_{cent1} because of the smaller effective mass of the $In_{0.53}Ga_{0.47}As$ channel. It is also clear that the capacitance dominance of any sub-band energy depends on its electron population density. Therefore, C_{inv2} is much smaller than C_{inv1} and C_{inv3} is negligible according to the fermi level penetration into the sub-band, as shown in the inset of Fig. 3.

For the extraction of border traps, the parameters of "Eq. (7)" were executed as follows. The oxide capacitance was calculated by dividing the oxide permittivity by the oxide thickness. The oxide relative permittivity was calculated according to the formula in "Eq. (11)" for every case, using the maximum capacitance value at a frequency of 10 kHz from the measured C-V data. To calculate the attenuation coefficient, the electron effective mass in Al_2O_3 was considered to be 0.23 m_0 based on the literature[33], where m_0 is the electron mass at rest; in addition, the barrier height between the oxide and semiconductor conduction band edge was calculated using the electron affinity rule. The semiconductor capacitance C_s was taken at the extraction voltage of the border traps using a one-dimensional Poisson-Schrodinger solver simulation tool (Nextnano) by simultaneously considering quantum confinement and non-parabolic band effects[40]. CET was calculated according to "Eq. (12)" in the Methods section using the capacitance value from 100 kHz at the border trap extraction voltage. Both N_{bt} and τ_0 were used as fitting parameters to achieve the best-fit curve for capacitance from the model by solving "Eq. (7)" with the measured data. A list of parameters that were used for the modelling is presented in Table 1.

Figure 4 shows the N_{bt} extraction fitting curves at 1 V using physical thickness t_{ox} for both the RTA- and FGA-processed cases. In both cases, the samples deposited at 200 °C show the lowest capacitance compared with the 250 °C and 300 °C deposited samples. This variation in capacitance values is mainly due to the difference in thickness between the samples deposited at different temperatures. As mentioned previously, the 200 °C processed samples showed the greatest thickness and henceforth the lowest capacitive value. The opposite case was observed for the 300 °C deposited samples. In another interesting observation, the FGA-processed samples showed somewhat lower capacitance in three different deposition cases compared with their respective RTA-processed samples. However, in the RTA-processed samples shown in Fig. 4a, there was more distortion of capacitance at the lower frequencies of the measurement window (10 kHz to 1 MHz) than at the higher ones. This disturbance in capacitance may be attributed to the noise associated with lower frequency measurements[42]. On the contrary, the FGA-processed samples did not suffer from this limitation.

In both cases at higher frequencies of the measurement window, the experimental data diverged from the fitting curve and displayed a different slope of capacitance versus $\log(\omega)$. This change in the gradient of the capacitance versus $\log(\omega)$ at higher frequencies is consistent at the measurement frequency range, which may be attributed to the distribution of border traps. A high concentration of traps (in the range of $10^{21}\,cm^{-3}\,eV^{-1}$) was reported at <1 nm from the oxide–semiconductor interface. Notably, this high density of traps that are positioned at <1 nm from the Al_2O_3/InGaAs interface are also found at the lower frequencies of measurement[33]. However, the extracted border trap densities of the 200 °C, 250 °C, and 300 °C deposited RTA samples were $1.28 \times 10^{20}\,cm^{-3}\,eV^{-1}$, $1.1 \times 10^{20}\,cm^{-3}\,eV^{-1}$ and $1 \times 10^{20}\,cm^{-3}\,eV^{-1}$, respectively. For FGA samples, the extracted border trap densities were $9.6 \times 10^{19}\,cm^{-3}\,eV^{-1}$, $9.75 \times 10^{19}\,cm^{-3}\,eV^{-1}$ and $7.6x \times 10^{19}\,cm^{-3}\,eV^{-1}$, respectively. The value of τ_0 in these extractions was in the range of 10^{-12} s, which is attributed to the lower capture cross-sectional areas of the traps.

Figure 5 shows the N_{bt} extraction for the same samples by considering the quantum mechanical effect. In this case, the physical thickness was replaced by the CET, and these CET values were extracted for all six cases. Both N_{bt} and τ_0 were used as fitting parameters as before, while keeping the other parameters unchanged. Both the disturbance in capacitance at lower frequencies and the distortion of the gradient of capacitance versus $\log(\omega)$ also existed in this case. The simulated curves obtained from the model showed a better fit than previous cases. The N_{bt} values extracted for RTA samples were $4 \times 10^{19}\,cm^{-3}\,eV^{-1}$, $4.1 \times 10^{19}\,cm^{-3}\,eV^{-1}$, and $3.09 \times 10^{19}\,cm^{-3}\,eV^{-1}$ for the deposition conditions of 200 °C, 250 °C, and 300 °C, respectively. For the FGA samples, the N_{bt} values were $2.98 \times 10^{19}\,cm^{-3}\,eV^{-1}$, $3.58 \times 10^{19}\,cm^{-3}\,eV^{-1}$, and $2.72 \times 10^{19}\,cm^{-3}\,eV^{-1}$, respectively. τ_0 was also in the same range as earlier. However, the N_{bt} values extracted using CET were much lower than the values obtained by using

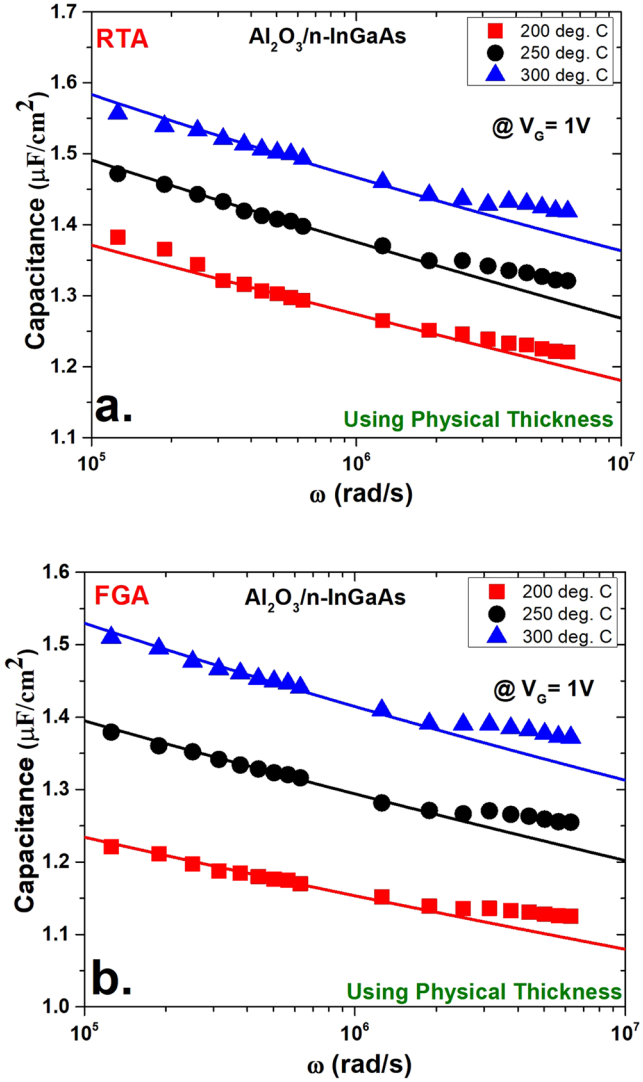

Figure 4. Model fitting of the capacitance versus frequency curves for the measured data (solid symbols) and calculated data from distributed border trap model (solid lines) using physical thickness (t_{ox}) at an applied DC gate bias of 1 V. The fitting was performed for three different deposition conditions of Al_2O_3 on n-InGaAs. Shown here are the (**a**) RTA conditions and (**b**) FGA conditions.

physical thickness, t_{ox}. This comparison is illustrated in Fig. 6a,b. The N_{bt} values by CET were approximately one third of (~65% lower than) the values by t_{ox}. The overestimation of N_{bt} values using physical thickness may be because the additional thickness of the oxide layer due to quantum confinement in the $In_{0.53}Ga_{0.47}As$ layer is not considered. Because the charge centroid is shifted, it causes the oxide–semiconductor interface to shift a finite thickness. As a result, the interface traps, which may contribute to energy loss, are excluded.

Figure 7a,b compare the extracted N_{bt} values of both RTA- and FGA-processed samples at three different deposition temperatures, as described previously. In both cases, the FGA-processed samples showed lower values of N_{bt} than did the RTA-treated samples. This indicates that defect passivation is more effective during the FGA process. In addition, more hydrogen (H_2) is incorporated to passivate the dangling bonds, which is the reason for the border traps within the amorphous Al_2O_3 dielectric in the FGA process[38]. However, the RTA-processed samples showed comparatively lower D_{it} values than did the FGA-processed samples. Therefore, RTA treatment passivated the interface traps, whereas border traps are treated by FGA effectively. Furthermore, N_{bt} was observed to be the lowest for the 300 °C deposited sample comparing with the 200 °C and 250 °C deposited samples for both RTA- and FGA-processed cases. This lower N_{bt} indicates structural differences in the film stoichiometry at 300 °C, which leads to more hydrogen (H_2) incorporation during FGA, as reported elsewhere[38]. Therefore, the probability of hydrogen (H_2) bonding to defects is increased.

Figure 8 shows the N_{bt} spatial distribution as a function of gate voltage, as well as the distance of the probing depth from the interface into the oxide. The values of N_{bt} were extracted at different applied DC voltages, whereas the values of τ_0 were used to determine the probing depth into the oxide at any measurement frequency. Because border traps are more responsive at lower frequencies and the physical distance into the oxide up to where the

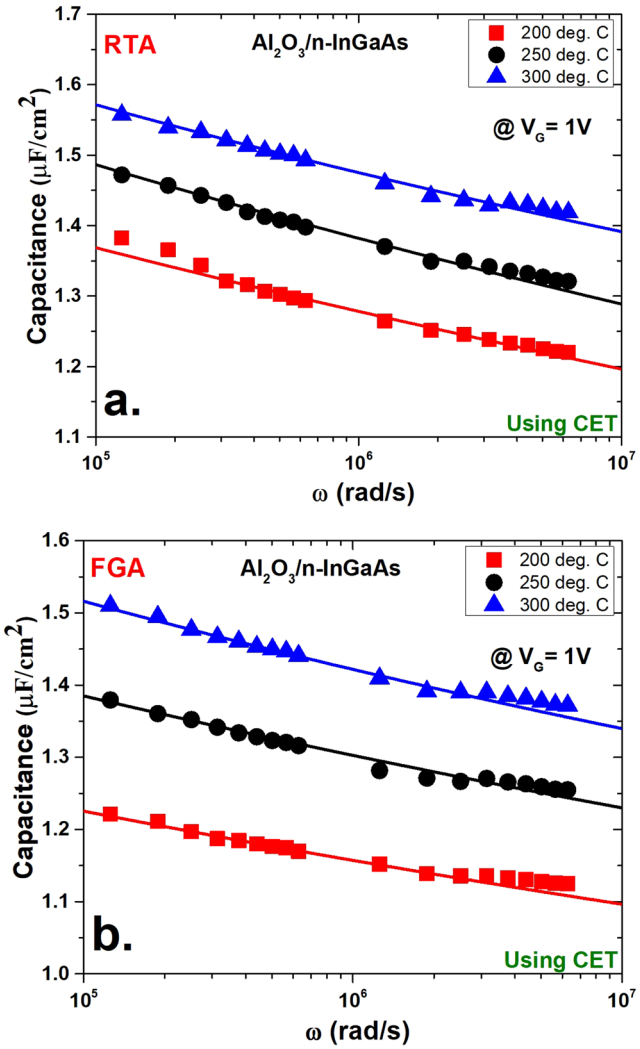

Figure 5. Model fitting of the capacitance versus frequency curves for the measured data (solid symbols) and calculated data (solid lines) as in Fig. 4 using capacitance-equivalent thickness (CET) at an applied DC gate bias of 1 V. Shown here are (**a**) RTA conditions and (**b**) FGA conditions.

traps respond is inversely proportional to the applied frequency, we used the lowest frequency of the measurement window (i.e., 10 kHz) to calculate the response region. The N_{bt} distribution increases as the applied voltage is increased. With the applied voltage increase, the Fermi level penetration into the conduction band also increases; in addition, the effective barrier height decreases, which makes the majority of carriers more likely to tunnel into the deep traps. When the applied voltage increases, traps with smaller electron capture cross-sectional areas in the deep oxide layer respond. Because all parameters, excluding τ_0, are the same at different extraction voltages, a smaller τ_0 results in a larger tunneling distance.

Conclusion

We extracted the border trap density of an Al_2O_3 oxide layer deposited at three different temperatures to n-$In_{0.53}Ga_{0.47}As$ on a 300-mm Si substrate by considering the quantum mechanical effect. Because quantum confinement and charge centroid effects are more prominent in relatively small-scale devices, these effects must be considered to model N_{bt} in the oxide layer.

We calculated the density of border traps using both physical thickness and CET while keeping other parameters constant. The N_{bt} values extracted using CET were approximately 65% lower than N_{bt} values obtained by physical thickness. The samples were also processed by different annealing treatments. FGA-annealed samples showed comparatively lower N_{bt} values than did than RTA-processed samples, although the RTA-processed samples had lower D_{it} values. The FGA treatment helps to passivate the border traps, whereas the interface traps are passivated by RTA. Moreover, samples deposited at 300 °C showed moderately low border trap concentrations because of their different stoichiometric structure, which allowed for more H_2 incorporation during FGA. The relationship between tunneling distance and border trap concentration with respect to border trap extraction voltage was also studied. With an increase of applied voltage as the Fermi level penetrated into the conduction

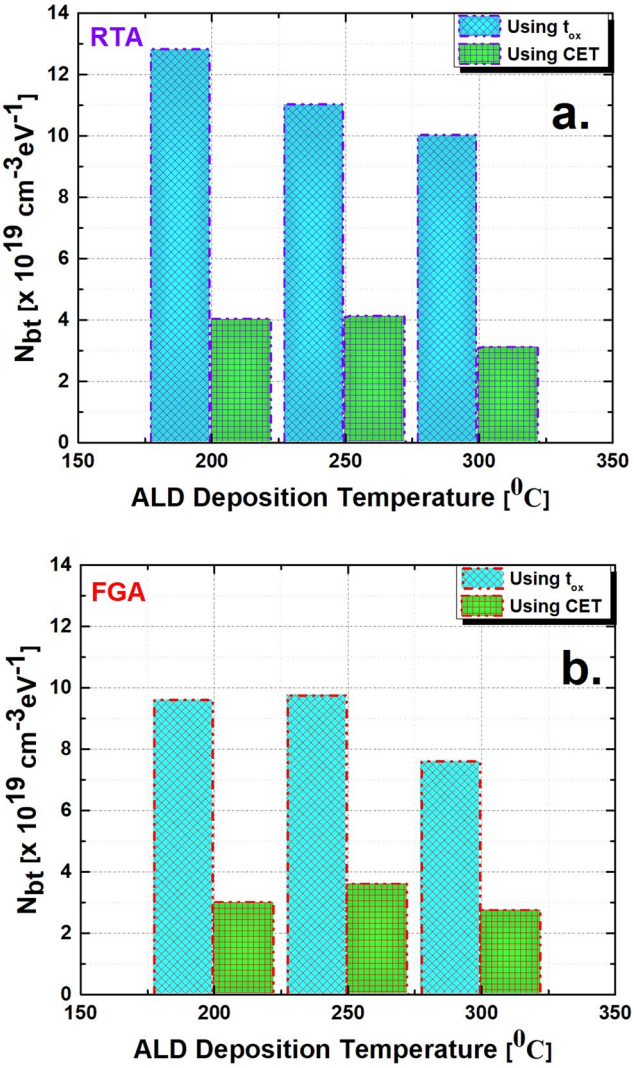

Figure 6. Extracted border trap density (N_{bt}) difference between the physical thickness (t_{ox}) and capacitance-equivalent thickness (CET)-based extraction. The comparisons were made for all three deposition conditions. Shown here are (**a**) RTA conditions and (**b**) FGA conditions.

band, the tunneling distance was observed to be deeper from the response of more traps with relatively small electron capture areas.

Methods

Sample preparation and measurements. An $In_{0.53}Ga_{0.47}As$ n-type heterostructure was created by metal-organic chemical vapor deposition (MOCVD) according to the procedure described here. First, two strain-relaxation buffer epitaxies of GaAs and InP were grown on a typical 300-mm n-type Si (001) substrate following the Volmer-Weber growth mode, with a carrier concentration of $2 \times 10^{18}\,cm^{-3}$ on each layer and thicknesses of 350 nm and 800 nm, respectively. Then, an upper structure was formed, which consisted of a 110-nm Si-doped n-$In_{0.53}Ga_{0.47}As$ layer with an electron density of $5 \times 10^{17}\,cm^{-3}$ as the bottom layer and another 160-nm Si-doped n-$In_{0.53}Ga_{0.47}As$ layer with an electron density of $1 \times 10^{17}\,cm^{-3}$ as the upper layer.

A total of six samples of ALD Al_2O_3 with a configuration of 30 cycles on $In_{0.53}Ga_{0.47}As$ were prepared. They were deposited at three different growth temperatures of 200 °C, 250 °C, and 300 °C, while two samples were arranged at any specific temperature. Prior to deposition of the dielectric, the $In_{0.53}Ga_{0.47}As$ substrates were treated with several wet cleaning processes to remove any native oxide or other contaminants. At the start, the substrates were cleaned with acetone and isopropyl alcohol for 5 minutes each. Then, they were treated with a solution of diluted hydrochloric acid (HCl) and deionized (DI) water, maintaining a ratio of 1:10 at room temperature for 30 s to eliminate any native oxide. Subsequently, they were cleaned with deionized water for 2 minutes and dried in a nitrogen (N_2) environment to displace the water from the wafer surface so that no water mask could form.

After the solution treatment, the substrates were transported to an ALD chamber within a minimal time interval. Before starting the actual deposition, 10 cycles of trimethylaluminium (TMA) preclean were performed because it was reported to be beneficial for passivating the interface trap density due to a self-cleaning effect[20,42,43].

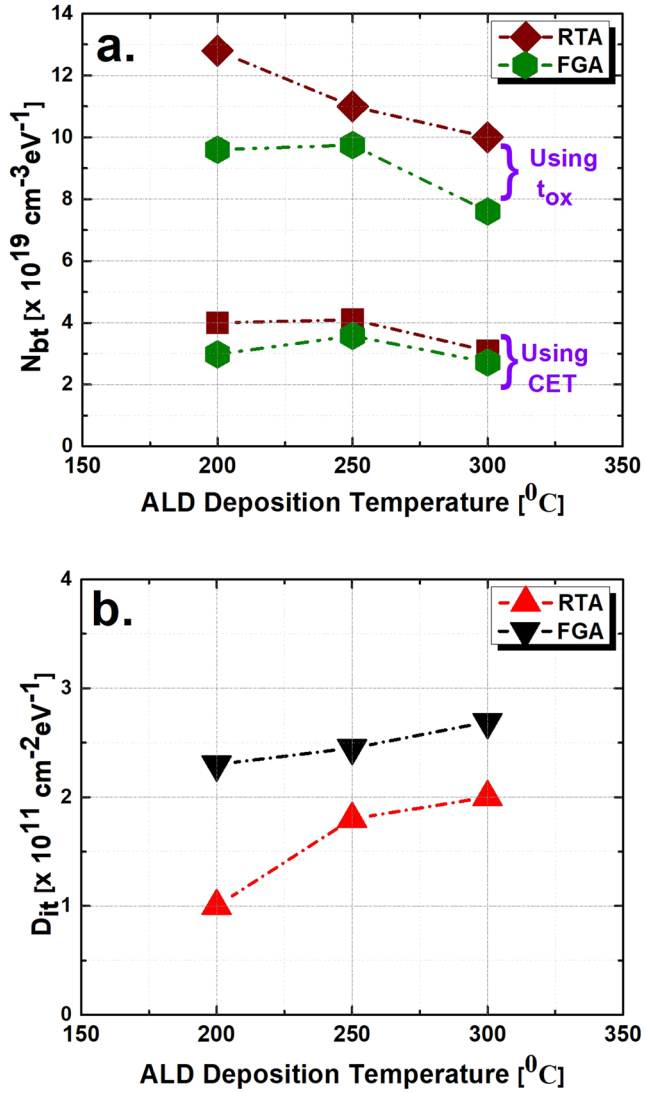

Figure 7. (**a**) Extracted border trap density (N_{bt}) and (**b**) interface trap density (D_{it}) comparisons between two different annealing processes of Al_2O_3/n-InGaAs samples according to their different deposition temperatures.

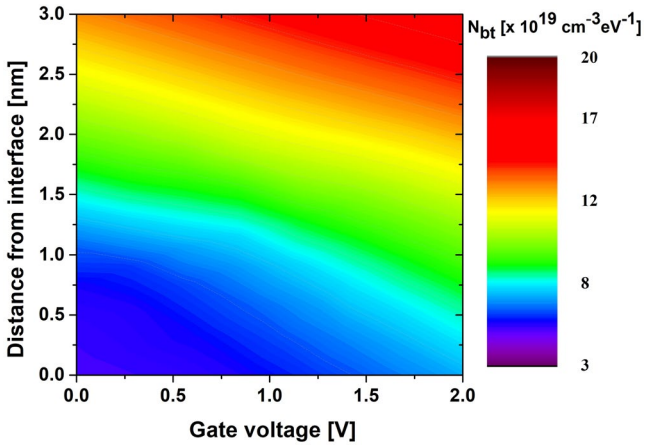

Figure 8. Spatial distribution of border trap density (N_{bt}) as a function of applied gate voltage, as well as the location in an Al_2O_3 dielectric from the Al_2O_3/n-InGaAs interface.

Then, the Al_2O_3 dielectric was deposited by ALD using TMA and water (H_2O) as the metal precursor and oxidant, respectively. The deposition process began with a TMA pulse onto the $In_{0.53}Ga_{0.47}As$ surface and then was followed with a water pulse. The pulse time was 0.1 s in both cases. Between the TMA pulse and water pulse, a purge duration of 20 s was maintained. Nitrogen (N_2) was used for both the purge and carrier gas, with a flow rate of 300 sccm. Both the TMA and water reservoirs were at room temperature.

The physical thickness (t_{ox}) of the ALD-deposited Al_2O_3 layers was quantified by ellipsometry at an incident angle of 70°. The thicknesses were found to be 4.2006 nm, 3.867 nm, and 3.5128 nm for the 200 °C, 250 °C, and 300 °C deposition cases, respectively. Therefore, for MOS capacitor formation after Al_2O_3 deposition, an ALD 5-nm TiN layer was deposited on top of the dielectric. Then, a metal layer of Ti/Au (200/2000 Å) was deposited by electron-beam (E-beam) evaporation for frontside metal contact by a lift-off process. The same metal layer was again deposited for backside metal contact. Reactive-ion etching based on SF_6/Ar Gas (30/10 sccm) was used to etch the TiN layer.

After the MOS capacitor formation, one set of samples deposited at three different temperatures was processed by RTA for 2 minutes at 350 °C in nitrogen (N_2) ambient, whereas another set was annealed at 300 °C in forming gas (N_2:H_2 = 96%:4%) for 30 minutes. The C-V curves at a frequency range from 10 kHz to 1 MHz were measured at room temperature using a Keithley 4200A-SCS parameter analyzer by applying a gate voltage. The effective relative permittivity (ε_r) and *CET* were calculated according to the following equations:

$$\varepsilon_r = \frac{C_{\max} t_{ox}}{\varepsilon_0} \tag{11}$$

Here, C_{max} is the maximum capacitance per unit area and t_{ox} is the oxide thickness.

$$CET = \frac{3.9\varepsilon_0}{C_{accum}} \tag{12}$$

Here, C_{accum} is the accumulation capacitance per unit area. The interface trap density (D_{it}) was calculated through the conductance method by measuring the parallel conductance (G_p/ω_{max})[44].

References

1. Del Alamo, J. A. Nanometre-scale electronics with III–V compound semiconductors. *Nature* **479**, 317–323 (2011).
2. Lin, H. C., Wang, W. E., Brammertz, G., Meuris, M. & Heyns, M. Electrical study of sulfur passivated $In_{0.53}Ga_{0.47}As$ MOS capacitor and transistor with ALD Al_2O_3 as gate insulator. *Microelectronic Engineering*, https://doi.org/10.1016/j.mee.2009.03.112 (2009).
3. Lin, D. *et al.* Enabling the high-performance InGaAs/Ge CMOS: a common gate stack solution. In *IEEE International Electron Devices Meeting* (*IEDM*) 1–4, https://doi.org/10.1109/IEDM.2009.5424359 (IEEE, 2009).
4. Taoka, N. *et al.* Impact of Fermi Level Pinning inside Conduction Band on Electron Mobility of $In_xGa_{1-x}As$ MOSFETs and Mobility Enhancement by Pinning Modulation. In *International Electron Devices Meeting* 27.2.1–27.2.4, https://doi.org/10.1109/IEDM.2011.6131622 (IEEE, 2011).
5. Heyns, M. *et al.* Advancing CMOS beyond the Si roadmap with Ge and III/V devices. In *International Electron Devices Meeting* 3, 13.1.1–13.1.4 (IEEE, 2011).
6. Hu-Dong, C. *et al.* Effect of the Si-doped $In_{0.49}Ga_{0.51}P$ barrier layer on the device performance of $In_{0.4}Ga_{0.6}As$ MOSFETs grown on semi-insulating GaAs substrates. *Chinese Physics B* **22**, 077306 (2013).
7. Chang, Y. C. *et al.* Atomic-layer-deposite HfO_2 on $In_{0.53}Ga_{0.47}As$ Passivation and energy-band parameters. *Applied Physics Letters* **072901**, 1–4 (2008).
8. Zadeh, D. H. *et al.* $La_2O_3/In_{0.53}Ga_{0.47}As$ metal–oxide-semiconductor capacitor with low interface state density using TiN/W gate electrode. *Solid State Electronics* **82**, 29–33 (2013).
9. Chobpattana, V., Mates, T. E., Zhang, J. Y. & Scaled, S. S. ZrO_2 dielectrics for $In_{0.53}Ga_{0.47}As$ gate stacks with low interface trap densities. *Applied Physics Letters* **104**, 182912 (2014).
10. Mahata, C. *et al.* Comparative Study of Atomic-Layer-Deposited Stacked (HfO_2/Al_2O_3) and Nanolaminated ($HfAlO_x$) Dielectrics on $In_{0.53}Ga_{0.47}As$. *ACS: Applied Material and Interfaces* **5**, 4195–4201 (2013).
11. Feng, X. *et al.* The Study of Electrical Properties for Multilayer La_2O_3/Al_2O_3 Dielectric Stacks and $LaAlO_3$ Dielectric Film Deposited by ALD. *Nanoscale Research Letters* **12**, 10–13 (2017).
12. Dou, C. *et al.* Determination of energy and spatial distribution of oxide border traps in $In_{0.53}Ga_{0.47}As$ MOS capacitors from capacitance–voltage characteristics measured at various temperatures. *Microelectronics Reliability* **54**, 746–754 (2014).
13. Vurgaftman, I., Meyer, J. R. & Ram-Mohan, L. R. Band parameters for III–V compound semiconductors and their alloys. *Journal of Applied Physics* **89**, 5815–5875 (2001).
14. Sze, S. M. *Physics of Semiconductor Devices*. (Wiley-Interscience, 1983).
15. Fleetwood, D. M. "Border Traps" in MOS Devices. *IEEE Transactions On Nuclear Science* **39**, 269–271 (1992).
16. Gan, J. Extraction of Border Trap Density in InAs Nanowire Transistors. (M.Sc Thesis in Nanoscience,Lund University, SWEDEN, 2012).
17. Lin, D. *et al.* Beyond interface: the impact of oxide border traps on InGaAs and Ge n-MOSFETs. In *International Electron Devices Meeting* 28.3.1–28.3.4, https://doi.org/10.1109/IEDM.2012.6479121 (IEEE, 2012).
18. Huang, J. *et al.* InGaAs MOSFET Performance and Reliability Improvement by Simultaneous Reduction of Oxide and Interface Charge in ALD $(La)AlO_x/ZrO_2$ Gate Stack. In *IEEE International Electron Devices Meeting* (*IEDM*) 1–4, https://doi.org/10.1109/IEDM.2009.5424357 (IEEE, 2009).
19. Fleetwood, D. M. Border traps and bias-temperature instabilities in MOS devices. *Microelectronics Reliability* **80**, 266–277 (2018).
20. Krylov, I., Ritter, D. & Eizenberg, M. The physical origin of dispersion in accumulation in InGaAs based metal oxide semiconductor gate stacks. *Applied Physics Letters* **117**, 174501 (2015).
21. Yu, B. *et al.* Effect and extraction of series resistance in Al_2O_3 - InGaAs MOS with bulk-oxide trap. *Electronics Letters* **49**, 3–4 (2013).
22. Chen, H. *et al.* Interface-State Modeling of Al_2O_3 - InGaAs MOS From Depletion to Inversion. *IEEE Transactions on Electron Devices* **59**, 2383–2389 (2012).
23. Brammertz, G. *et al.* A Combined Interface and Border Trap Model for High-Mobility Substrate Metal–Oxide–Semiconductor Devices Applied to $In_{0.53}Ga_{0.47}As$ and InP Capacitors. *IEEE Transactions on Electron Devices* **58**, 3890–3897 (2011).
24. Zhang, C., Xu, M., Ye, P. D. & Li, X. A Distributive-Transconductance Model for Border Traps in III–V/High-k MOS Capacitors. *IEEE Electron Device Letters* **34**, 735–737 (2013).

25. Lu, H.-H., Xu, J.-P., Liu, L., Lai, P.-T. & Tang, W.-M. Equivalent distributed capacitance model of oxide traps on frequency dispersion of C-V curve for MOS capacitors. *Chinese Physics B* **25**, 118502 (2016).
26. Kim, E. J. *et al*. Atomically abrupt and unpinned $Al_2O_3/In_{0.53}Ga_{0.47}As$ interfaces: Experiment and simulation. *Journal of Applied Physics* **106**, 124508 (2009).
27. Ahn, J. *et al*. Arsenic decapping and pre-atomic layer deposition trimethylaluminum passivation of Al_2O_3/InGaAs (100) interfaces. **103**, 071602 (2013).
28. Yuan, Y. *et al*. A Distributed Bulk-Oxide Trap Model for Al_2O_3 InGaAs MOS Devices. *IEEE Transactions on Electron Devices* **59**, 2100–2106 (2012).
29. Preier, H. Contributions of surface states to mos impedance. *Applied Physics Letters* **10**, 361–363 (1967).
30. Mui, D. S. L., Reed, J., Biswas, D. & Morkoç, H. A new circuit model for tunneling related trapping at insulatorsemiconductor interfaces in accumulation. *Journal of Applied Physics* **72**, 553 (1992).
31. Yu, Y. *et al*. A Distributed Model for Border Traps in Al_2O_3 - InGaAs MOS Devices. *IEEE Electron Device Letters* **32**, 485–487 (2011).
32. Babadi, A. S., Lind, E. & Wernersson, L. E. Modeling of n-InAs metal oxide semiconductor capacitors with high - κ gate dielectric. *Journal of Applied Physics* **116**, 214508 (2014).
33. Lin, J. *et al*. Examining the relationship between capacitance-voltage hysteresis and accumulation frequency dispersion in InGaAs metal-oxide-semiconductor structures based on the response to post-metal annealing. *Microelectronic Engineering* **178**, 204–208 (2017).
34. Galatage, R. V. *et al*. Accumulation capacitance frequency dispersion of III–V metal-insulator- semiconductor devices due to disorder induced gap states. *Journal of Applied Physics* **116**, 014504 (2014).
35. Jena, K., Swain, R. & Lenka, T. R. Impact of oxide thickness on gate capacitance – Modelling and comparative analysis of GaN-based MOSHEMTs. *Pramana—Journal of physics* **85**, 1221–1232 (2015).
36. Pal, H. S., Cantley, K. D., Shahid, S. & Lundstrom, M. S. Influence of Bandstructure and Channel Structure on the Inversion Layer Capacitance of Silicon and GaAs MOSFETs. *IEEE Transactions On Electron Devices* **55**, 904–908 (2008).
37. Yoshio Nishi, R. D. *Handbook of Semiconductor Manufacturing Technology*. (CRC Press, 2007).
38. Tang, K. *et al*. Border trap reduction in Al_2O_3/InGaAs gate stacks. *Applied Physics Letters* **107**, 202102 (2015).
39. Maiorano, P. *et al*. Non-parabolic band effects on the electrical properties of superlattice FETs. In 2013 *14th International Conference on Ultimate Integration on Silicon* (*ULIS*) 93–96, https://doi.org/10.1109/ULIS.2013.6523499 (IEEE, 2013).
40. Birner, S. The nextnano software for the simulation of semiconductor heterostructures. *Topological nanodevice modeling* 85586 Available at, https://www.nextnano.de/downloads/publications/abstracts/Abstract_TopologicalNanodeviceModeling_2014_Delft_Birner.pdf (2014).
41. Sirtori, C., Capasso, F., Faist, J. & Scandolo, S. Nonparabolicity and a sum rule associated with bound-to-bound and bound-to-continuum intersubband transitions in quantum wells. *Physical Review B* **50**, 8663–8674 (1994).
42. Trinh, H., Chang, E. Y., Wong, Y., Chang, C. & Yu, C. Self-cleaning Effects on Atomic Layer Deposition (ALD) of Al_2O_3 on InGaAs with Several Surface Treatments. In *Extended Abstracts of the 2009 International Conference on Solid State Devices and Materials* 478–479 (2009).
43. Gao, J., Li, W., Mandal, S. & Chowdhury, S. A study of the effect of surface pretreatment on atomic layer deposited Al_2O_3 interface with GaN. In *Proceedings of the SPIE* 10381 (2017).
44. Engel-Herbert, R. H., Hwang, Y. & Stemmer, S. Comparison of methods to quantify interface trap densities at dielectric/III–V semiconductor interfaces. *Journal of Applied Physics* **108**, 124101 (2010).

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Author Contributions

Md. Mamunur Rahman conducted most of the experiments and wrote the manuscript including preparing figures. Jun-Gyu Kim helped in capacitor fabrication, metal deposition and electrical characterization. Dae-Hyun Kim supervised the work and reviewed the manuscript. Tae-Woo Kim initiated the work, gave the main idea and supervised the entire process. All authors analysed and discussed the results.

Additional Information

Competing Interests: The authors declare no competing interests.

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