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Large current modulation and tunneling magnetoresistance change by a side-gate electric field in a GaMnAs-based vertical spin metal-oxide-semiconductor field-effect transistor

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A vertical spin metal-oxide-semiconductor field-effect transistor (spin MOSFET) is a promising low-power device for the post scaling era. Here, using a ferromagnetic-semiconductor GaMnAs-based vertical spin MOSFET with a GaAs channel layer, we demonstrate a large drain-source current I_{DS} modulation by a gate-source voltage V_{GS} with a modulation ratio up to 130%, which is the largest value that has ever been reported for vertical spin field-effect transistors thus far. We find that the electric field effect on *indirect* tunneling via defect states in the GaAs channel layer is responsible for the large I_{DS} modulation. This device shows a tunneling magnetoresistance (TMR) ratio up to ~7%, which is larger than that of the planar-type spin MOSFETs, indicating that I_{DS} can be controlled by the magnetization configuration. Furthermore, we find that the TMR ratio can be modulated by V_{GS} . This result mainly originates from the electric field modulation of the magnetic anisotropy of the GaMnAs ferromagnetic electrodes as well as the potential modulation of the nonmagnetic semiconductor GaAs channel layer. Our findings provide important progress towards high-performance vertical spin MOSFETs.

Reducing the power consumption in integrated circuits is an important issue that we have to tackle in the 21st century. Making volatile components non-volatile is one of the most promising approaches to this issue; various non-volatile technologies, such as reconfigurable logic circuits¹, non-volatile power gating² and magnetic random access memory, are applicable to low-power-consumption electronics. A spin metal-oxide-semiconductor field-effect transistor (spin MOSFET)^{3,4}, in which source and drain electrodes are ferromagnetic materials, is a key component for realizing those applications because of the several advantages inherent in spin MOSFETs: The most important advantage of spin MOSFETs over other spintronics devices such as all-spin-logic devices^{5,6} is the high amplification capability, which is crucially important for restoring propagating signals between transistors, and thus indispensable for the application to large scale integrated circuits. Also, spin MOSFETs are compatible with existing well-matured semiconductor technologies, which makes integration with semiconductor devices very easy. Spin MOSFETs can have the same advantages of scaling circuits as those of general transistors, which is very important for miniaturization of the device from the view point of energy consumption. For practical operation of spin MOSFETs, both large current modulation by applying a gate electric field and large magnetoresistance

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Figure 1. (a) Schematic illustration of the vertical spin MOSFET investigated in this study. The backside of the substrate is the source electrode, the comb shaped Au/Cr layer is the drain electrode and the Au/Cr layer above the HfO₂ layer is the gate electrode. (b,c) Schematic device operation of our vertical spin MOSFET when a gate voltage V_{GS} is not applied (b) and when a negative gate voltage is applied (c). The orange arrows represent a drain-source current I_{DS} .

(MR) by magnetization reversal are required. At present, lateral and vertical types of spin MOSFETs have been proposed. The lateral spin MOSFETs, in which a current flows parallel to the substrate plane and is controlled by a gate electric field applied from the top of the channel, have a large current modulation capability ($5 \times 10^6\%$ ⁷, 400% ⁸ and $10^7\%$ ⁹); however, the problem is the small MR ratio (0.1% ⁷, 0.005% ⁸ and 0.027% ⁹). Meanwhile, epitaxial magnetic heterostructures were grown using various ferromagnets and semiconductors and some magnetotransport properties were studied^{10–15}. Thus, a vertical spin field-effect transistor (FET), in which a current flows perpendicular to the film plane and is controlled by a gate voltage applied from the side surface of the channel, is promising for large MR. Previously, we reported ferromagnetic-semiconductor GaMnAs-based vertical spin FETs that exhibit large MR ratios (60% ¹⁶ and 5% ¹⁷). A GaMnAs-based heterostructure is one of the most ideal material systems, because we can obtain high-quality single-crystalline GaMnAs/nonmagnetic semiconductor (GaAs)/GaMnAs trilayers and thus can suppress spin relaxation at the interfaces^{18–21}. However, in those vertical spin FETs, the current modulation ratio by the gate voltage was small (0.5% ¹⁶ and 20% ¹⁷). Thus, vertical spin FETs with a large current modulation are strongly required. In addition, to further improve the performance of the vertical spin FETs, we need more profound understanding of the gate electric field effect on the spin-dependent transport.

In vertical spin FETs, as shown by our electric field simulations later, the gate electric field influences the electric potential profile only within 10 nm from the side surfaces of the intermediate channel layer, which limits the current modulation. Thus, the lateral size of vertical FETs should be decreased as much as possible for obtaining high-performance vertical spin FETs. In this study, to enhance the current modulation and to understand the electric field effect on the spin-dependent transport, we reduced the lateral size (=width of the mesas as explained later) of the GaMnAs-based vertical spin MOSFET to ~ 500 nm. We have successfully obtained a large current modulation by the gate electric field with a modulation ratio up to 130%, which is the largest value that has been ever reported for vertical spin FETs^{16,17}. Furthermore, using the electric field simulations, we find that *indirect* tunneling mainly contributes to the observed large current modulation. These new findings are important steps to further improve the performance of the vertical spin FETs.

Results

Samples. Our vertical spin MOSFET has a thin GaAs channel (9 nm) and ferromagnetic-semiconductor GaMnAs source and drain electrodes [Fig. 1(a)] (See the Methods section). To increase the current modulation, we reduced the width of the mesas down to ~ 500 nm. As a gate insulator, a 40-nm-thick HfO₂ film was used since it has a large relative permittivity, which also contributes to the increase of the current modulation. In this device, tunneling of holes occurs between the source and drain, because GaAs is a potential barrier with a height of ~ 100 meV for holes in the GaMnAs layers^{22,23}, as shown in Fig. 1(b). When the gate-source voltage $V_{GS} < 0$ V ($V_{GS} \geq 0$ V), the tunneling current flowing at the side surfaces of the mesas is increased (decreased), as shown in Fig. 1(c).

MOSFET operation and its analyses. To investigate the MOSFET characteristics of this device, we measured the drain-source current I_{DS} as a function of the drain-source voltage V_{DS} for various V_{GS} [Fig. 2(a)].

Figure 2. (a) Drain-source current I_{DS} as a function of the drain-source voltage V_{DS} with the gate-source voltage V_{GS} ranging from -20 V to 20 V with a step of 5 V at 3.8 K. (b) I_{DS} modulation ratio as a function of V_{DS} with various V_{GS} at 3.8 K. (c) Drain-source current ($-I_{DS}$) (left axis) and the I_{DS} value normalized at $V_{GS} = 0$ V (γ) (right axis) as a function of V_{GS} with $V_{DS} = -10$ mV at 3.8 K. (d) Calculated I_{DS} normalized by the one at $V_{GS} = 0$ V (γ_{calc}) as a function of $E_V^{(S)}$. (e, h) Calculated valence band top energy E_V with respect to the Fermi level when $E_V^{(S)} = 0.75$ eV (e) and $E_V^{(S)} = 0.15$ eV (h). Here, the Fermi level corresponds to 0 eV. The vertical axis expresses the hole energy. The inset in (e) and (h) shows the structure used in our calculation. Here, the x axis represents the distance from the side surface of the mesa and the y axis denotes the distance from the interface between the bottom GaMnAs layer and the intermediate GaAs layer. The calculation was performed in the region surrounded by the dashed line. In (e, h), only the region of $0 \text{ nm} \leq x \leq 15 \text{ nm}$ is shown because it is sufficient to see how the gate electric field influences the valence band maximum energy in the GaAs layer. (f, g) E_V vs. y at $x = 1 \text{ nm}$ (f) and 15 nm (g) when $E_V^{(S)} = 0.75 \text{ eV}$. (i, j) E_V vs. y at $x = 1 \text{ nm}$ (i) and 15 nm (j) when $E_V^{(S)} = 0.15 \text{ eV}$.

Nonlinear I_{DS} - V_{DS} characteristics were observed for each V_{GS} (black curves), indicating that tunneling transport is dominant. Furthermore, I_{DS} was largely controlled by V_{GS} . We note that the gate leakage current and electric field effect on parasitic resistances (the resistances of the top/bottom GaMnAs layers, GaAs:Be layer and Au/Cr electrodes), which may induce unintended modulation of I_{DS} , were negligibly small (see Supplementary Note 1). When $V_{GS} = 20$ V, the I_{DS} modulation ratio by V_{GS} , which is defined by $[I_{DS}(V_{GS}) - I_{DS}(V_{GS} = 0 \text{ V})]/I_{DS}(V_{GS} = 0 \text{ V}) \times 100$ (%), is around -20% [see the blue points in Fig. 2(b)]. On the other hand, when $V_{GS} = -20$ V, it reached $\sim 130\%$ [see the red points in Fig. 2(b)]. This I_{DS} modulation ratio ($\sim 130\%$) is the largest among the values reported for vertical spin FETs thus far^{16,17}.

To understand the modulation of the band alignment in detail, we measured I_{DS} as a function of V_{GS} at $V_{DS} = -10$ mV [Fig. 2(c)]. I_{DS} normalized at $V_{GS} = 0$ V (γ) was changed from 1 to 1.28 when V_{GS} was changed from 0 V to -3 V [see the right axis in Fig. 2(c)], meaning that I_{DS} was increased by 28% when V_{GS} was changed from 0 V to -3 V. As shown below, this large modulation of I_{DS} cannot be understood by the electric field effect on *direct* tunneling. To obtain the potential distribution and to calculate I_{DS} normalized at $V_{GS} = 0$ V (γ_{calc}), we performed electric field simulation varying the electric potential at the side surface of the mesa and investigated the effect of the side-gate electric field [Fig. 2(e, h)] (see Supplementary Note 2). Here, we define $E_V^{(S)}$ as the valence band top energy E_V at the side surface (interface between the side-gate electrode and the GaAs channel) with respect to the Fermi level E_F in terms of hole energy. The potential profile of E_V when $E_V^{(S)} = 0.75$ eV is shown in Fig. 2(e), which corresponds to the case of $V_{GS} = 0$ V, because E_F at the side surface of the GaAs channel is pinned at the middle of the band gap²⁴. With decreasing $E_V^{(S)}$ from 0.75 eV, the electric potential near the side surface of the mesa is decreased [Fig. 2(f, i)], whereas the electric potential in the inner region of the mesa ($10 \text{ nm} \leq x$) is not influenced [Fig. 2(g, j)]. As shown in Fig. 2(d), γ_{calc} remains almost unchanged between Fig. 2(e) ($\gamma_{calc} = 1$ when $E_V^{(S)} = 0.75$ eV) and (h) ($\gamma_{calc} = 1.028$ when $E_V^{(S)} = 0.15$ eV) because GaAs is a potential barrier for holes in both cases. On the other hand, when $E_V^{(S)} < 0.15$ eV, because E_V of the GaAs channel at the side surface becomes lower than E_V inside the mesa, γ_{calc} starts to increase with decreasing $E_V^{(S)}$ [Fig. 2(d)]. This feature is different from the experimental data shown in Fig. 2(c); when V_{GS} is changed from 0 V to -10 V, γ starts to increase at $V_{GS} = 0$ V. We can see the significant difference in the curve shapes of Fig. 2(c) and Fig. 2(d). This analysis indicates that the electric field effect on the *direct* tunneling current *cannot* reproduce the experimental I_{DS} - V_{GS} characteristic.

Figure 3. (a) Drain-source resistance R_{DS} as a function of the in-plane external magnetic field μ_0H applied along the $[110]$ direction at 3.8 K. Here, the drain-source voltage V_{DS} was -5 mV and the gate-source voltage V_{GS} was 0 V. The black circles correspond to the major loop and the red circles correspond to the minor loop. The black (red) arrows are the sweep directions in the major (minor) loop. The magnetization states in the major loop are indicated by the white arrows above the graph. (b) TMR ratio as a function of the gate-source voltage V_{GS} at 3.8 K. Here, the drain-source voltage V_{DS} was fixed at -5 mV and the external magnetic field H was applied along the $[110]$ direction. The TMR ratio is the maximum value obtained in the major loop at each V_{GS} . (c–e) Magnetic-field-direction dependences of the TMR ratios at $V_{DS} = -10$ mV with $V_{GS} = 0$ V (c), -5 V (d) and -10 V (e).

Instead, the main origin of the large modulation ratio observed in our device is the electric field effect on the indirect tunneling current²⁵.

The indirect tunneling current is probably caused by a large amount of Mn atoms ($\sim 10^{18} \text{ cm}^{-3}$), which are diffused to the intermediate GaAs layer from the top and bottom GaMnAs layers and form defect states in the band gap of GaAs. Furthermore, GaAs grown at low temperature (200°C) is known to have a large amount of arsenic antisite defects ($10^{18} - 10^{19} \text{ cm}^{-3}$)^{26,27}. In fact, the $I_{DS} - V_{DS}$ characteristics of our device show a strong temperature dependence (see Supplementary Note 3), which indicates that indirect tunneling via defect states takes place. (If I_{DS} were dominated only by the direct tunneling current, no temperature dependence would be observed.) Therefore, the electric field effect on indirect tunneling via defect states is the most probable origin for the large I_{DS} modulation ratio. To enhance the I_{DS} modulation ratio, we have to solve the Fermi level pinning problem at the surface of GaAs, i.e., because the Fermi level is severely pinned at the middle of the band gap at the surface of GaAs, it is very difficult to move the valence band maximum toward the Fermi level of the GaMnAs layers by the application of V_{GS} . The Fermi level pinning in GaAs is thought to originate from defect states formed at the interface between GaAs and gate insulators. Thus, reducing the interface state density between GaAs and gate insulators is a key to enhancing the current modulation ratio by V_{GS} .

Tunneling magnetoresistance and its change by V_{GS} . To investigate the spin-dependent transport of our device, we measured the drain-source resistance R_{DS} as a function of μ_0H applied along the $[110]$ direction in the film plane with $V_{DS} = -5$ mV and $V_{GS} = 0$ V [Fig. 3(a)]. Here, R_{DS} is defined by V_{DS}/I_{DS} , μ_0 is the permeability of a vacuum and H is an in-plane external magnetic field. In the major loop (black circles), clear tunnel magnetoresistance (TMR) was observed, indicating that I_{DS} can be controlled by the magnetization configuration. The TMR ratio, which is defined by $[R_{DS}(\mu_0H) - R_{DS}(\mu_0H = 0 \text{ mT})]/R_{DS}(\mu_0H = 0 \text{ mT}) \times 100$ (%), reached $\sim 7\%$ at $\mu_0H = 20$ mT, where $R_{DS}(\mu_0H)$ is the drain-source resistance at H in the major loop. This value is more than 70 times larger than the MR ratios obtained in the lateral spin MOSFETs^{7–9}. In the major loop, the negative MR was observed at $\mu_0H < 0$ mT ($\mu_0H > 0$ mT) when μ_0H was swept from positive to negative (negative to positive) probably because of a multi-domain structure in the top and bottom GaMnAs layers. We also observed a clear minor loop (red circles), indicating that the antiparallel magnetization configuration is stable even at $\mu_0H = 0$ mT. (In the minor loop, R_{DS} increases with increasing μ_0H from -20 mT to 10 mT, probably because the magnetizations of the top and bottom GaMnAs layers are not completely antiparallel at the peak of R_{DS} (at $\mu_0H = -20$ mT in the major loop) and they become close to the perfect antiparallel configuration with increasing μ_0H to 10 mT in the minor loop.)

To investigate the influence of V_{GS} on the spin-dependent transport, we measured the V_{GS} dependence of the TMR ratio [Fig. 3(b)]. Here, the TMR ratio corresponds to the maximum value obtained in the major loop at each V_{GS} . The TMR ratio tends to increase as V_{GS} is changed from 0 V to -10 V. In our device, the gate electric field can modulate the electronic states of the top/bottom GaMnAs layers as well as those of the intermediate GaAs layer, both of which can modulate TMR. Applying V_{GS} causes the change in the hole density of the GaMnAs layers near the side surfaces of the mesas, which can change the spin polarization and magnetic anisotropy¹⁷. To understand the modulation of the magnetic anisotropy by V_{GS} in our device, we measured TMR applying H in various in-plane directions with an angle θ with respect to the $[100]$ axis in the counterclockwise rotation when $V_{GS} = 0$, -5 and -10 V [Fig. 3(c–e)] (see Measurements section). The observed TMR ratios showed dominant uniaxial anisotropy along the $[\bar{1}10]$ direction in addition to biaxial anisotropy along the $\langle 100 \rangle$ directions for any V_{GS} [see the four red peaks in Fig. 3(c–e)]. With changing V_{GS} from 0 V to -10 V, the easy axes of our device were slightly rotated toward the $[010]$ direction (the red-colored region is extended toward the $[010]$ direction). In spintronics devices, changing the magnetization directions is necessary to write information, which accompanies the power consumption. The controllability of the magnetic anisotropy by the gate voltage is more advantageous in spintronics devices than other methods such as optical control of the magnetic properties²⁸ because we can expect the reduction of the power consumption required for writing information, since the application of the gate voltage does not accompany joule heating. Furthermore, the coercive force of the top GaMnAs layer, which has a larger coercivity than the bottom GaMnAs layer, increases as V_{GS} is changed from 0 V to -10 V (the red-colored region slightly expands outward). These results indicate that the magnetic anisotropy constants are modulated by applying negative V_{GS} , which can also contribute to the modulation of the TMR ratio. In addition, V_{GS} modifies the valence band maximum energy in the GaAs layer. As we discussed in the previous section, the modulation of the indirect tunneling current via defect states is the most probable mechanism for the obtained large modulation of I_{DS} . The TMR induced by indirect tunneling via defect states depends on many factors such as energy levels of defect states, band width of defect states, life time of carries and so on. The modulation of the electric potential can influence the indirect tunneling and thus TMR. Therefore, the electric field effect both on the top/bottom GaMnAs layers and on the intermediate GaAs layer contributes to the modulation of the observed TMR ratio. Although only the side surfaces of the mesas are influenced by V_{GS} , the MR and the magnetic anisotropy of our device are clearly modulated. This phenomenon can be understood as follows. When negative V_{GS} is applied, the current flowing at the side surface of the mesas is increased and becomes dominant in I_{DS} . When negative V_{GS} is applied, the magnetic properties of the side surface of the top and bottom GaMnAs layers are also modulated. These facts indicate that the modulation of the magnetic properties of the top and bottom GaMnAs layers, which takes place only at the edge regions of the mesas, is preferentially reflected to the measured spin-dependent transport properties in our device. Therefore, the MR and the magnetic anisotropy of our device are modulated although only the edge regions of the mesas are influenced by V_{GS} .

Surprisingly, the V_{GS} dependence of the TMR ratio shown in Fig. 3(b) is completely opposite to the one obtained in our previous study, *i.e.* the TMR ratio *decreased* as negative V_{GS} is applied in our previous study¹⁶. This may be caused by the difference of the easy axes between the present device and the previous one (the biaxial anisotropy was dominant in our previous work) or by the different direction of an external magnetic field (along the direction with an angle 10° from the $[100]$ direction toward the $[1\bar{1}0]$ in our previous work).

Summary

In summary, we have investigated the electric field effect on the spin-dependent transport properties in a GaMnAs-based vertical spin MOSFET. We obtained a large current modulation ratio up to 130%, which is the largest value that has ever been reported thus far for the vertical spin FETs^{16,17}. By comparing the experimental data with the calculated results, we concluded that this large I_{DS} modulation does not originate from the modulation of direct tunneling between the source and the drain but from the modulation of the indirect tunneling current via defect states in the intermediate GaAs layer. The TMR ratio tends to increase as negative V_{GS} is applied, which is attributed to the electric field effect both on the top/bottom GaMnAs layers and on the intermediate GaAs layer. These results provide an important insight into the device physics for realizing high-performance vertical spin MOSFETs.

Methods

Growth. The heterostructure composed of, from the top to the bottom, Ga_{0.94}Mn_{0.06}As (10 nm)/GaAs (9 nm)/Ga_{0.94}Mn_{0.06}As (3.2 nm)/GaAs:Be (50 nm, hole concentration $p = 5 \times 10^{18} \text{ cm}^{-3}$) on a p^+ -GaAs (001) substrate by low-temperature molecular beam epitaxy. The growth temperatures of the top Ga_{0.94}Mn_{0.06}As, GaAs, bottom Ga_{0.94}Mn_{0.06}As and GaAs:Be layers were 195°C , 180°C , 200°C and 520°C , respectively. The Curie temperatures of the top and bottom GaMnAs layers were estimated to be ~ 53 K and 20 – 30 K, respectively. (For the details, see the Supplementary Note 4). Post-growth annealing was not carried out.

Process. After the growth, we partially etched the grown films and buried the etched area with a 100-nm-thick SiO₂ layer for the separation of the drain electrode and the substrate. Then, a comb-shaped Au (40 nm)/Cr (5 nm) layer, whose width of the comb teeth is ~ 500 nm and length of them is $50 \mu\text{m}$, was formed by electron-beam lithography and a lift-off technique. We chemically etched the area that is not covered by the Au/Cr layer and then the magnetic tunnel junctions only beneath the comb teeth area of the Au/Cr drain electrode remained after the etching. Since the narrow-line-shaped mesas are formed by chemical wet etching, the influence of defects at the side surfaces of the GaAs layer induced by the *nanofabrication* of the mesas can be neglected. We formed a 40-nm-thick HfO₂ film as a gate insulator using atomic layer deposition at a substrate temperature of 150°C and deposited a gate electrode composed of Au (50 nm)/Cr (5 nm) by electron-beam deposition.

Measurements. After the device was bonded with Au wires and indium solder, we measured the spin-dependent transport properties of our spin MOSFET with varying V_{GS} and H at 3.8 K. Here, the experimental data of our vertical spin MOSFET are collected from 20 mesas that are connected by the drain electrode in the comb-shaped chip. To measure the θ dependence of TMR, we applied a strong magnetic field of 1 T in the opposite direction of θ to align the magnetization directions and we decreased H to zero. Then, we started to measure R_{DS} while increasing H from zero in the direction of θ . The measurements were performed at every 10° step of θ . We note that our experimental data are reproducible.

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Author Contributions

Sample preparation: T. Kanaki, H.Y., T. Koyama., and D.C.; measurements: T. Kanaki and H.Y.; data analysis: T. Kanaki and H.Y.; writing and project planning: T. Kanaki, S.O., and M.T.

Additional Information

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