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Improved Linearity with Polarization Coulomb Field Scattering in AlGaN/GaN Heterostructure Field-Effect Transistors

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The single-tone power of the AlGaN/GaN heterostructure field-effect transistors (HFETs) with different gate widths was measured. A distinct improvement in device linearity was observed in the sample with a larger gate width. The analysis of the variation of the parasitic source access resistance showed that, as the gate bias is increased, the polarization Coulomb field scattering can offset the increased polar optical phonon scattering and improve the device linearity. This approach is shown to be effective in improving the device linearity of AlGaN/GaN HFETs.

During the last decade, AlGaN/GaN heterostructure field-effect transistors (HFETs) have been extensively developed in the area of RF power electronics due to their high electron mobility and high breakdown electric field[1–3]. Device linearity is a crucial requirement for power amplifiers in wireless base stations, satellite communications, and radar applications. Linear distortion, which has hindered maximizing the advantages of AlGaN/GaN HFETs, has most recently been attracting extensive attention, given the increasingly thorough and widespread application of AlGaN/GaN HFETs in power amplifiers[4–7].

Polarization Coulomb field (PCF) scattering, caused by the non-uniform distribution of the polarization charges at the AlGaN/GaN interface, is a particular scattering mechanism in AlGaN/GaN HFETs[8–10]. PCF scattering has been found to be capable of affecting the parasitic source access resistance and the device transconductance[10,11], which are relevant to the device linearity. However, sufficient evidence of the effect of PCF scattering on device linearity is lacking in both experiments and theoretical studies. Previous studies have reported that PCF scattering can be changed by the material component and device structure[9,10]. This means that studying the effect of PCF scattering on device linearity may contribute to improving the linearity at the device level.

In this research, two types of AlGaN/GaN HFETs with different gate widths were fabricated. Then, the single-tone power was measured for the two samples. By analyzing the gain and input power at the 1-dB compression point, the effect of PCF scattering on the device linearity was explored.

Results and Discussion

The on-wafer RF power performances were tested by using a single-tone continuous-wave signal at 2.7 GHz. At a drain voltage of 20 V, the device matching was optimized for the maximum output power. The gate biases were chosen as −2 V, −1.5 V, −1 V, and −0.5 V, respectively. The match condition was correlated with the device structure and the chosen direct current quiescent points (DCQPs). Therefore, the detailed match parameters under different DCQPs were different for two samples, as shown in Table 1. Here, Γ_S and Γ_L refer to the source matching point and the load matching point, respectively. Figure 1 shows the output power (P_{OUT}), gain (G_T), and power added efficiency (PAE) as a function of the input power (P_{IN}) for the two samples. The G_T variation range for Sample 2 is obviously smaller than that for Sample 1. A flatter gain curve implies better device linearity. This means that Sample 2, which has a larger gate width, has better linearity. To further compare the linearity between

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V_{GS} (V)	V_{DS} (V)	Sample 1 ($W_G = 546\,\mu$m)				Sample 2 ($W_G = 780\,\mu$m)				Δ (%)
		I_{DS} (A/mm)	Γ_S	Γ_L	$P_{IN\text{-}1dB}$ ($\times 10^{-2}$ W/mm)	I_{DS} (A/mm)	Γ_S	Γ_L	$P_{IN\text{-}1dB}$ ($\times 10^{-2}$ W/mm)	
−2	20	0.041	$0.030 + j0.742$	$0.246 + j0.133$	3.33	0.039	$-0.280 + j0.661$	$0.171 + j0.141$	4.62	38.71
−1.5	20	0.110	$-0.131 + j0.697$	$0.326 + j0.120$	2.33	0.103	$-0.311 + j0.564$	$0.194 + j0.076$	3.49	50.00
−1	20	0.165	$-0.269 + j0.670$	$0.336 + j0.051$	2.24	0.154	$-0.331 + j0.469$	$0.194 + j0.076$	5.57	148.37
−0.5	20	0.212	$-0.275 + j0.657$	$0.261 + j0.067$	2.23	0.199	$-0.317 + j0.463$	$0.120 + j0.079$	3.55	58.89

Table 1. The detailed match parameters and the input power at 1-dB compression point $P_{IN\text{-}1dB}$ under different DCQPs for two samples.

the two samples, the input power at the 1-dB compression point $P_{IN\text{-}1dB}$ was extracted from Fig. 1, as shown in Table 1. The difference in $P_{IN\text{-}1dB}$ between the two samples can be written as

$$\Delta = \frac{P_{IN\text{-}1dB}(\text{Sample 2}) - P_{IN\text{-}1dB}(\text{Sample 1})}{P_{IN\text{-}1dB}(\text{Sample 1})} \times 100\%. \quad (1)$$

Under every fixed gate bias, the $P_{IN\text{-}1dB}$ for Sample 2 is significantly larger than that for Sample 1; Δ is at least 38.71% and can reach up to 148.37% (at $V_{GS} = -1$ V).

The linearity in power amplification is well known to be a complex phenomenon. The charge trapping in the surface state, gate-drain capacitance, self-heating effect, device transconductance, and parasitic source access resistance can affect the device linearity[7,10,12–16]. Because both samples were fabricated on the same material and with the same device technology, the charge trapping in the surface state and the gate-drain capacitance should be the same. The DC current-voltage (*I-V*) characteristics and the transfer characteristics were measured for the two samples, as shown in Fig. 2. The currents are almost the same for the two samples; therefore, the influence of the self-heating effect on the linearity of the two samples should be consistent. Because of the polarization Coulomb field scattering, the gate width can affect the parasitic source access resistance (R_S) and transconductance (g_m) under the unit gate width[17]. Because the ohmic contact resistance R_C (in the normalized unit "Ω·mm") is constant, R_S here is exclusive of R_C and refers only to the gate-source channel resistance. Considering that both samples have the same device size, except for their different gate widths, the intrinsic transconductance (g_{m0}) under the unit gate width for the two samples should be the same. An analysis of the expression $g_m = 1/(1/g_{m0} + R_S + R_C)$ indicates that the R_S variation can affect g_m, and then influence the gain and the device linearity[7,10]. Therefore, the improved linearity can be explained by considering the variation of R_S.

R_S is determined by the scattering mechanisms in the gate-source channel. The main scattering mechanisms in the gate-source channel include polar optical phonon (POP), deformation potential (DP), piezoelectric (PE), interface roughness (IFR), dislocation (DIS), and polarization Coulomb field (PCF) scatterings. Among these, the two major mechanisms are POP and PCF scatterings, which can be changed with the increase of the gate voltage.

When the electron drift velocity is sufficiently increased, the POP and electron temperatures start to increase; the POP scattering is enhanced with the increase of the electron temperature, inducing an increase in R_S[10]. For a clearer presentation, the POP scattering and the electron temperature as a function of V_{GS} at $V_{DS} = 20$ V can be calculated. Initially, the electron drift velocity v_e in the gate-source channel can be obtained from the *I-V* characteristic by applying $I_{DS} = n_{2D} \cdot q \cdot v_e$. With the obtained v_e, the electric field E_{GS} in the gate-source channel can be determined by the dependence of the electron drift velocity on the electric field[18]. Then, the dissipated power per electron UI_{DS}/N_e in the gate-source channel can be calculated, as shown in Fig. 3(a). Here, $U = E_{GS} \cdot L_{GS}$ is the voltage applied along the gate-source channel, L_{GS} is the gate-source distance, and $N_e = n_{2D} \cdot L_{GS} \cdot W_G$ is the number of electrons in the gate-source channel. Finally, based on the relationship between the electron temperature and the dissipated power per electron[18], the electron temperature T_e can be obtained, as shown in Fig. 3(b). As the gate bias is increased, the electron temperature is increased, and it remains at almost the same value for the two samples. This means that the influence of self-effect on R_S is the same for the two samples[17]. The R_S determined by the POP scattering R_S^{POP} can be calculated as follows[9]

$$R_S^{POP} = \frac{L_{GS}}{n_{2D} q \mu_{POP}} = \frac{L_{GS} m^*}{n_{2D} q^2} \cdot \frac{1}{\tau_{POP}} = \frac{L_{GS} m^*}{n_{2D} q^2} \cdot \frac{e^2 \omega_{POP} m^* N_B(T_e) G(k_0)}{2\varepsilon^* k_0 \hbar^2 P_{POP}(y)}, \quad (2)$$

where m^* is the electron effective mass in GaN, $\varepsilon^* = \varepsilon_0/(1/\varepsilon_h - 1/\varepsilon_s)$, ε_0 is the vacuum dielectric permittivity, ε_h is the high-frequency dielectric constant of GaN, ε_s is the static dielectric constant of GaN, $y = \pi\hbar^2 n_{2D}/m^* k_B T_e$, k_B is the Boltzmann constant, $\hbar\omega_{POP}$ is the POP energy, $k_0 = (2m^*(\hbar\omega_{POP})/\hbar^2)^{1/2}$ is the POP wave vector, $N_B(T_e) = 1/\exp(\hbar\omega_{POP}/k_B T_e) - 1$ is the Bose-Einstein function, $G(k_0) = b(8b^2 + 9k_0 b + 3k_0^2)/(8(k_0 + b)^3)$ and $P_{POP}(y) = 1 + (1 + e^{-y})/y$. As shown in Fig. 4(a), when the gate voltage is more than −2.5 V, the increased POP scattering causes R_S to increase as the gate voltage is increased.

PCF scattering originates from the non-uniform distribution of the polarization charges at the AlGaN/GaN interface[8–10]. Before the device processing or without the gate bias, the polarization charges at the AlGaN/GaN interface are uniform. On one hand, to form the ohmic contacts, Ti/Al/Ni/Au was deposited and then rapidly thermally annealed at 850 °C. During the annealing process, the ohmic contact metal atoms can diffuse into the AlGaN barrier layer and change the barrier layer strain[9,19]. On the other hand, because of the converse piezoelectric effect, the gate bias can also change the strain of the AlGaN barrier layer under the gate region[9,20]. The strain variation of the AlGaN barrier layer causes the variation of the polarization charges. Then, the distribution of the polarization charges becomes non-uniform. Compared with the uniformly distributed polarization charges, the

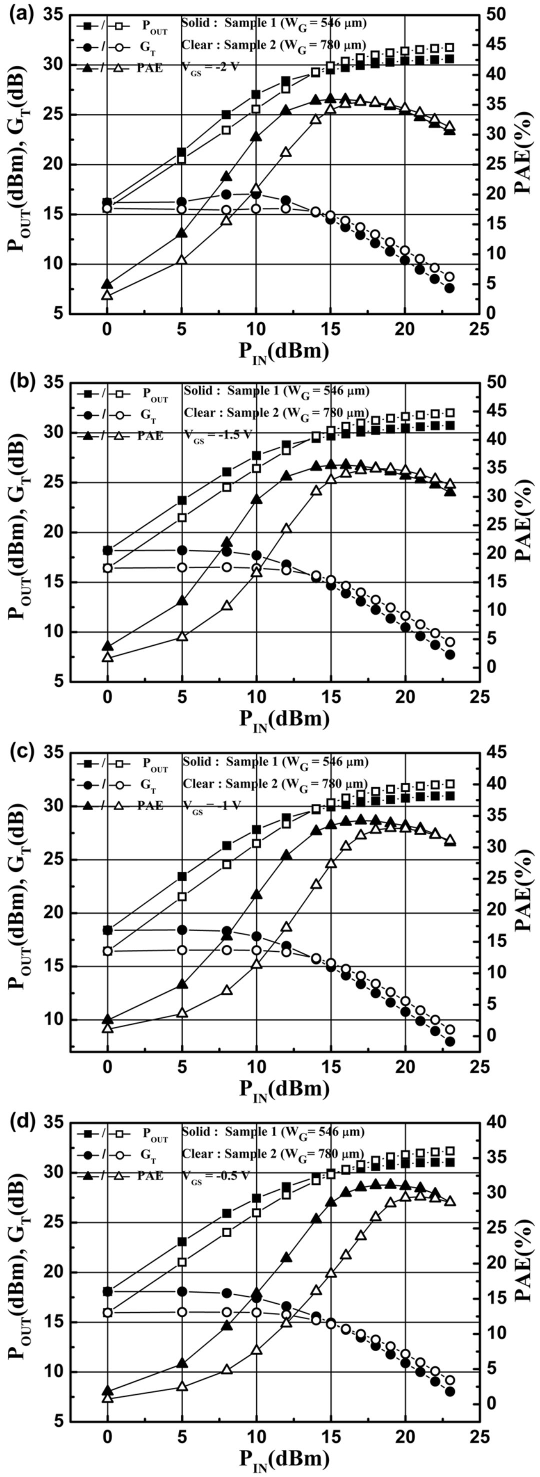

Figure 1. The output power P_{OUT}, gain G_T, and power added efficiency PAE as a function of the input power P_{IN} for the two samples with $V_{DS} = 20$ V at gate-source voltages of (**a**) −2 V, (**b**) −1.5 V, (**c**) −1 V, and (**d**) −0.5 V, respectively.

non-uniformly distributed ones can generate an additional scattering potential, which can scatter the channel electrons. The additional polarization charges are defined as the difference between the non-uniformly distributed polarization charges and the uniformly distributed ones. After the device processing, the additional polarization charges near the ohmic contact area do not change, and their influence on the PCF scattering is constant. The additional polarization charge $\Delta\sigma$ under the gate region can be calculated as[10,20]:

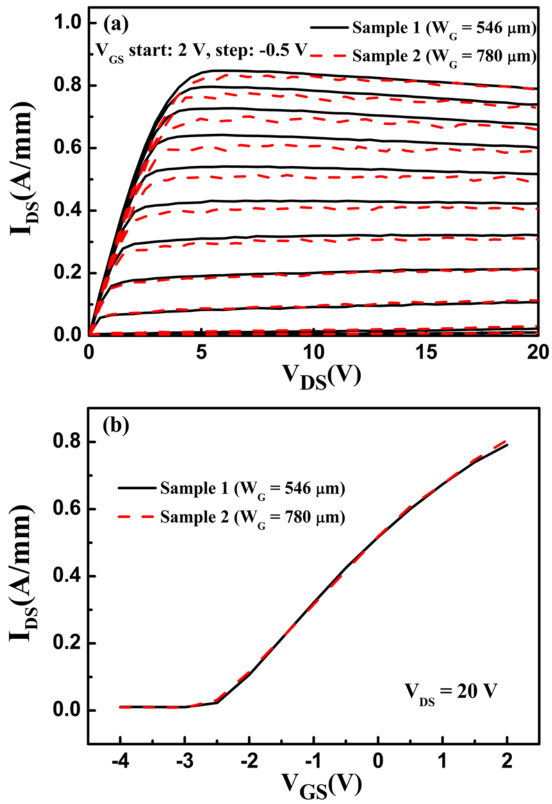

Figure 2. (**a**) The DC *I-V* characteristics and (**b**) the transfer characteristics for the two samples.

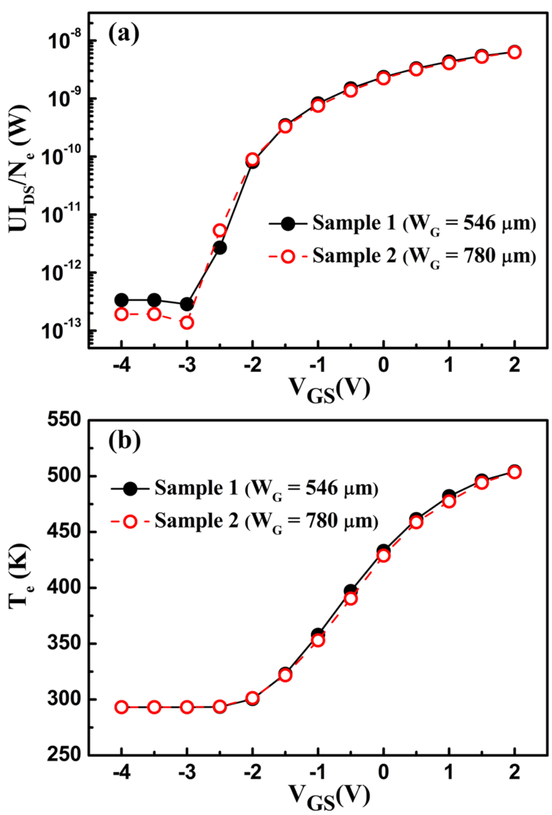

Figure 3. (**a**) The dissipated power per electron UI_{DS}/N_e and (**b**) the electron temperature T_e in the gate-source channel as a function of the gate-source voltage for the two samples.

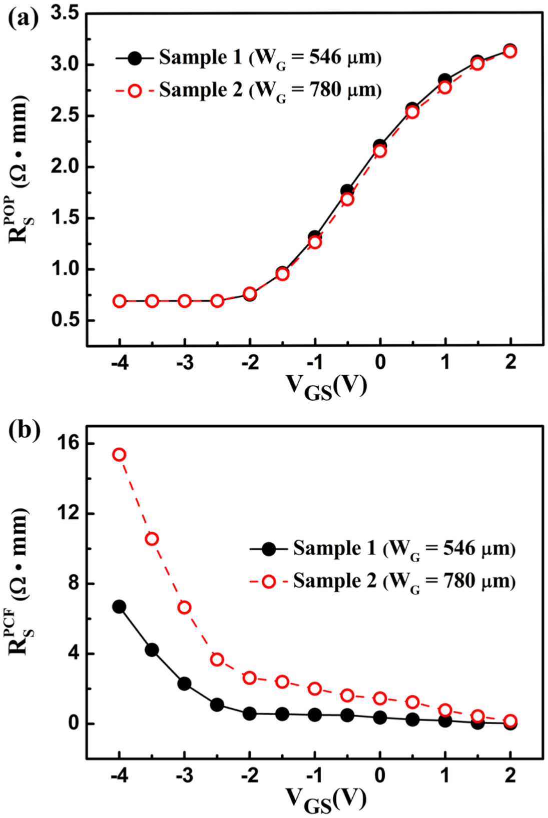

Figure 4. The R_S determined by (**a**) the polar optical phonon scattering R_S^{POP} and (**b**) the polarization Coulomb field scattering R_S^{PCF}.

$$\Delta\sigma = \frac{e_{33}^2}{C_{33}} \cdot \frac{V_{GS} - V_{ch}}{d_{AlGaN}}, \tag{3}$$

where e_{33} is the piezoelectric coefficient, C_{33} is the elastic stiffness tensor of AlGaN, V_{ch} is the potential in the channel, and d_{AlGaN} is the thickness of the AlGaN barrier layer. As shown in (3), $\Delta\sigma$ is relevant to V_{GS}. The larger $\Delta\sigma$ is, the stronger the PCF scattering. As V_{GS} is increased, $\Delta\sigma$ decreases and the PCF scattering weakens. The PCF scattering is stronger in the sample with a larger width[17]. Therefore, under the same gate voltage, Sample 2 has a larger PCF scattering than Sample 1. The R_S determined by the PCF scattering R_S^{PCF} can be obtained[11], as shown in Fig. 4(b). R_S^{PCF} clearly shows a monotonic decline as the gate bias is increased. Because Sample 2, which has a larger width, has a stronger PCF scattering, its R_S^{PCF} is larger compared with Sample 1.

As the gate bias is increased, the POP scattering is increased and the PCF scattering is decreased; together, these determine the variation of R_S. The decreased PCF scattering can effectively offset the increased POP scattering, decrease the variation of R_S, and then improve the linearity. This causes Sample 2, which has a larger PCF scattering, to have better linearity. The R_S values for different scattering mechanisms were calculated[11,21], as shown in Fig. 5(a) and (b). The POP, DP, and PE scatterings are enhanced with the increased gate bias, leading to the increase in R_S. Among these three mechanisms, POP scattering is the major one. Conversely, PCF scattering is the only mechanism that is decreased with the increased gate bias. The decreased PCF scattering can offset the increased scatterings, causing the R_S value to have a small variation. For a clear comparison, Fig. 5(c) shows the total R_S for the two samples. As shown in Fig. 2(b), the threshold voltage for the two samples is −2.5 V, therefore the V_{GS} in the range of −2.5 V to 2 V is effective. During the effective gate bias range, the R_S for Sample 2 is flatter than that for Sample 1, which means that Sample 2 has a smaller R_S variation. Based on $g_m = 1/(1/g_{m0} + R_S + R_C)$, a smaller R_S variation implies a smaller g_m variation and better device linearity. Hence, Sample 2 shows better linearity.

In addition, when the gate bias is more negative, the PCF scattering is stronger than the POP scattering, and R_S is decreased with the increased gate bias. As the gate bias is increased, the POP scattering is rapidly increased with the increase of the electron temperature. When $V_{GS} = -1$ V was chosen as the DCQP, the offset effect between the PCF and the POP scattering was the most suitable for the power output. Therefore, when $V_{GS} = -1$ V, the offset range for POP and PCF scattering is the largest, and the improvement in linearity is most apparent (corresponding to $\Delta = 148.37\%$). This further confirmed that PCF scattering exerts a vital influence on the device linearity by affecting R_S.

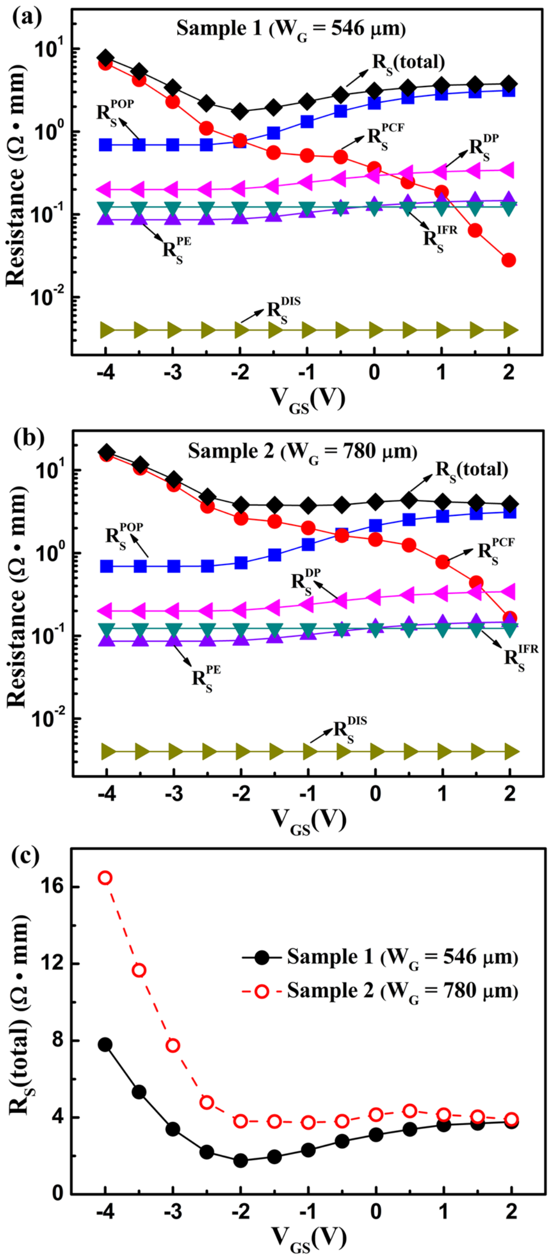

Figure 5. (**a**) The R_S determined by the polar optical phonon scattering R_S^{POP}, polarization Coulomb field scattering R_S^{PCF}, deformation potential scattering R_S^{DP}, piezoelectric scattering R_S^{PE}, interface roughness scattering R_S^{IFR}, and dislocation scattering R_S^{DIS}; the total gate-source resistance values R_S (total) for (**a**) Sample 1 and (**b**) Sample 2, and (**c**) the total gate-source resistance values R_S (total) as a function of the gate-source voltage for the two samples.

Conclusion

The single-tone power of the AlGaN/GaN HFETs with different gate widths was measured, and the improvement in linearity was determined. The results indicate that PCF scattering can offset the increased POP scattering as the gate bias is increased, as well as enhance the linearity of the devices. Thus, the approach is effective in improving the device linearity of AlGaN/GaN HFETs.

Methods

Sample fabrication. The AlGaN/GaN heterostructure was grown by molecular beam epitaxy (MBE). The epitaxial structure was grown on a sapphire substrate consisting of, from the bottom to the top, a 40-nm-thick AlN buffer layer, a 2-μm-thick GaN channel layer, a 1-nm-thick AlN interlayer, and a 20-nm-thick $Al_{0.2}Ga_{0.8}N$ barrier layer. The Hall measurement yielded a two-dimensional electron gas (2DEG) sheet electron density (n_{2D}) of 8×10^{12} cm^{-2} and an electron mobility (μ) of 2000 cm^2/V·s at room temperature. The device fabrication started with mesa isolation, which was formed by inductively coupled plasma reactive ion etching (ICP-RIE) with the use of a BCl_3/Cl_2 gas mixture. Ti/Al/Ni/Au (300/1500/500/600 Å) was evaporated and annealed at 850 °C for 30 s in nitrogen atmosphere to form the drain and source ohmic contacts. The space between the drain and source ohmic contacts was 6 μm. Transmission-line matrix measurements showed that the specific contact resistivity of the ohmic contacts was $2 \times 10^{-5}\ \Omega\cdot cm^2$. Ni/Au (600/2000 Å) two-finger gate with 1-μm gate length (L_G) was fabricated and located in the middle of the drain and source ohmic contacts. Finally, the devices were passivated by using a 100-nm-thick SiN layer deposited by PECVD. Devices with gate width (W_G) of 546 μm (2 × 273 μm) and 780 μm (2 × 390 μm) were marked as Samples 1 and 2, respectively.

Measurements. The on–wafer RF power performance of uncooled devices were tested by using a Maury load-pull system. The *I-V* characteristics were measured with the use of an Agilent B1500A semiconductor parameter analyzer.

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Author Contributions

P.C. and Z.L. contributed to the research design, experiment measurements, data analysis, and manuscript preparation. Y.L. fabricated the device. H.L. and A.C. carried out mathematical calculation. C.F. provided scientific advice. All authors reviewed this manuscript.

Additional Information

Competing Interests: The authors declare that they have no competing interests.

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