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## **OPEN** Remarkably High Mobility **Thin-Film Transistor on Flexible Substrate by Novel Passivation** Material

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High mobility thin-film transistor (TFT) is crucial for future high resolution and fast response flexible display. Remarkably high performance TFT, made at room temperature on flexible substrate, is achieved with record high field-effect mobility ( $\mu_{FF}$ ) of 345 cm<sup>2</sup>/Vs, small sub-threshold slope (SS) of 103 mV/dec, high on-current/off-current ( $I_{ON}/I_{OFF}$ ) of  $7 \times 10^6$ , and a low drain-voltage (V<sub>D</sub>) of 2V for low power operation. The achieved mobility is the best reported data among flexible electronic devices, which is reached by novel HfLaO passivation material on nano-crystalline zinc-oxide (ZnO) TFT to improve both I<sub>ON</sub> and I<sub>OFF</sub>. From X-ray photoelectron spectroscopy (XPS) analysis, the non-passivated device has high OH-bonding intensity in nano-crystalline ZnO, which damage the crystallinity, create charged scattering centers, and form potential barriers to degrade mobility.

The flexible electronics is the key technology for bendable light weight display<sup>1–7</sup>. Similar to traditional rigid displays, the higher mobility TFT<sup>1-24</sup> is demanded for next generation higher density, faster speed, and lower power flexible display<sup>6</sup>. The amorphous InZnGaO (IGZO)  $TFT^{5-10}$  is a potential candidate for flexible electronics due to the low off-current ( $I_{OFF}$ ) from its large energy bandgap and high mobility of overlapped s-orbitals. However, the major issue for IGZO TFT is the rare Indium quantity in Earth's crust and its high price. Alternatively, crystallized ZnO TFT is another candidate due to its better crystallinity than amorphous structure, similar with the much higher mobility of poly-Si than amorphous-Si TFTs. However, no high mobility poly-ZnO TFT was reported to date. In this paper, we demonstrate a high performance nano-crystallized ZnO TFT on low-cost Polyethylene naphthalate (PEN) flexible substrate processed at room temperature. Remarkably high  $\mu_{FE}$  of 345 cm<sup>2</sup>/Vs was achieved in nano-crystalline ZnO TFT on flexible substrate with a high dielectric constant (high- $\kappa$ ) gate oxide<sup>25-29</sup>. This  $\mu_{FE}$  value is even higher than IGZO and ZnON TFTs made on rigid glass<sup>22, 23</sup> that is also the record highest value for devices on flexible substrate<sup>1-7</sup>. The high mobility is further supported by the low interface trap density from the small SS of only 103 mV/dec. Besides, high  $I_{ON}/I_{OFF}$  of 7 × 10<sup>6</sup> and a low V<sub>D</sub> of 2 V were measured to reach low switching power of  $C_G V_D^2 f / 2$ , where  $C_G$  and f are the gate capacitance and operation frequency, respectively. This remarkably high mobility TFT is achieved using novel HfLaO passivation on nano-crystalline ZnO. For comparison, the control non-passivated device has a  $\mu_{FE}$  of 43 cm<sup>2</sup>/Vs. To understand such large mobility improvement, the X-ray photoelectron spectroscopy (XPS) was performed. The non-passivated ZnO showed a strong OH bonding signal. The formed HO-Zn-OH compound via moisture absorption will break the Zn-O bonding in ZnO crystal to form dangling bonds and charged scattering centers to lower the mobility strongly. In contrast to other passivation methods<sup>14-21</sup>, the LaO-based dielectric has important advantage of moisture absorption to lower the OH bonding formation as evident from the XPS data<sup>25–29</sup>. The remarkably high  $\mu_{FF}$  HfLaO/ZnO TFT suggests the excellent opportunity for both flexible and rigid display applications.

### Results

The fabricated devices on flexible PEN substrate is shown in the photo of Fig. 1. Figure S1(a,b) show the capacitance-voltage (C-V) and current-voltage (J-V) characteristics of Al/high- $\kappa$  metal-gate capacitor fabricated on the same flexible PEN substrate, respectively. A high capacitance density of  $0.35 \,\mu\text{F/cm}^2$  was measured that lead to an equivalent-oxide-thickness (EOT) of 9.9 nm. A still low leakage current of  $1.4 \times 10^{-5}$  A/cm<sup>2</sup> was measured at 1.5 V, even processed at room temperature. This is due to the merit of high- $\kappa$  dielectrics, especially the

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Figure 1. Device photo of fabricated TFTs on flexible PEN substrate.

higher  $\kappa$  TiO<sub>2</sub> dielectric. The TiO<sub>2</sub> has higher  $\kappa$  value for low voltage operation. To improve the interface<sup>30</sup>, extra SiO<sub>2</sub> dielectric was inserted between ZnO and TiO<sub>2</sub>. To improve the leakage current via the low conduction band offset ( $\Delta E_C$ ) of TiO<sub>2</sub>, stacked TiO<sub>2</sub>/HfO<sub>2</sub> were applied<sup>31</sup>.

Figure 2(a–c) show the transistor's drain-source current versus drain-source voltage ( $I_{DS}$ - $V_{DS}$ ) and  $I_{DS}$  versus gate-source voltage ( $I_{DS}$ - $V_{GS}$ ) characteristics of ZnO/high- $\kappa$ /metal-gate TFTs with and without HfLaO passivation. The ZnO TFTs without passivation show reasonable performance of  $I_{ON}/I_{OFF}$  of 2 × 10<sup>5</sup>, SS of 112 mV/dec, and a V<sub>T</sub> of 0.78 V. Here the gate leakage current is lower than  $I_{OFF}$  due to the thick stacked gate dielectric. The ZnO TFTs after HfLaO passivation shows more than one order of magnitude higher  $I_{ON}$  and 4 times lower  $I_{OFF}$ , with large  $I_{ON}/I_{OFF}$  of 7 × 10<sup>6</sup>, small SS of 103 mV/dec, and a low V<sub>T</sub> of 0.13 V. These good device integrities were achieved at a low V<sub>D</sub> of 2 V that is crucial to lower the switching power by orders of magnitude than existing TFT devices. Besides, the steep SS can also turn on the transistor faster for a lower voltage and power operation.

The  $\mu_{EF}$ - $V_{GS}$  characteristics is plotted in Fig. 3 from the measured  $I_{DS}$ - $V_{GS}$  characteristics. For control non-passivated devices, an acceptable peak  $\mu_{FE}$  of 43 cm<sup>2</sup>/Vs is obtained for room-temperature-processed ZnO TFT. The TFT devices after HfLaO passivation has remarkably high  $\mu_{FE}$  of 345 cm<sup>2</sup>/Vs; this is the highest value for TFT on flexible substrate<sup>1-7</sup> and is even higher than the reported IGZO and ZnON TFTs fabricated on rigid substrate<sup>22, 23</sup>. The much improved  $\mu_{FE}$  for HfLaO-passivated device is owing to the higher  $I_{ON}$  and the lower  $I_{OFF}$ . It is important to notice that the  $\mu_{FE}$  decreases monotonically with decreasing gate length<sup>32, 33</sup>:

$$\mu \approx \mu_0 \frac{L}{L + \mu_0 W C_{ox} R_{SD} (V_{GS} - V_{th})} \tag{1}$$

where  $R_{SD}$  is the source/drain series resistance,  $\mu_{FE}$  is the apparent field-effect mobility and  $\mu_0$  is the true field effect mobility. At long gate length, the  $\mu_{FE}$  is approaching to  $\mu_0$ ; thus, the long 48  $\mu$ m gate length device was used.

To understand the mechanism of such large mobility improvement, material and structure analysis were performed. Figure 4(a) shows the secondary ion mass spectrometry (SIMS) depth profile, where a ZnO channel, HfO<sub>2</sub>, TiO<sub>2</sub>, and thin SiO<sub>2</sub> gate dielectric stack were recognized. The device structure of Al contact, ZnO channel, high- $\kappa$  gate dielectric stack, and TaN metal-gate were also observable from the cross-sectional transmission electron microscopy (TEM) image shown in Fig. 4(b). The ZnO active layer forms columnar nano-crystalline structure with a size of ~10–20 nm. The formed crystalline structure is further evidenced from the X-ray diffraction (XRD) spectra shown in Fig. 4(c). Highly oriented phases of XRD peaks were measured, even though the ZnO was deposited by sputtering at room temperature. The full-width at half-maximum (FWHM) of XRD spectra are comparable with the data of ZnO published in literature<sup>34, 35</sup>, while the IGZO has an amorphous structure<sup>36</sup>.

Figure 5(a,b) show the XPS spectra without and with HfLaO passivation, respectively. The atomic composition of nano-crystalline structure is identified to be  $Zn^{2+}-O^{2-}$ , as measured from the XPS spectra. It is important to notice that significant amount of OH bonding signal was also measured for non-passivated device. The OH bonding in nano-crystalline ZnO was originated from the moisture absorption of ambient air, even though dry process steps were used to fabricate the devices. Similar strong moisture absorption is well known in IGZO to cause degradation.

The chemical reaction of ZnO and H<sub>2</sub>O is expressed as:

$$ZnO + H_2O \rightarrow Zn(OH)_2$$
 (2)

In addition to surface, the tiny H<sub>2</sub>O molecule can also react with grain boundaries through the thin 20-nm ZnO. Here the grain boundaries are highly reactive due to their high defect density. Once the Zn(OH)<sub>2</sub> was formed, it damaged the Zn-O bonded nano-crystal and created dangling bonds that further form charged states in the ZnO bandgap. The decreased XPS OH signal and related charged defects are also supported from the high positive charge density ( $\Delta Q_p$ ) of 2 × 10<sup>12</sup> cm<sup>-2</sup>, which was obtained from the V<sub>T</sub> shift ( $\Delta V_T$ ) between HfLaO-passivated and non-passivated ZnO devices shown in Fig. 3(b), from the  $\Delta Q_p = C_G \times \Delta V_T$ . Such positive



**Figure 2.**  $I_{DS}$ - $V_{DS}$  and characteristics of ZnO/high- $\kappa$ /TaN TFT on flexible PEN (**a**) without and (**b**) with HfLaO passivation. (**c**)  $I_{DS}$ - $V_{GS}$  characteristics of ZnO/high- $\kappa$ /TaN TFT on flexible PEN without and with HfLaO passivation.



**Figure 3.** The  $\mu_{FE}$ - $V_{GS}$  characteristics of ZnO/high- $\kappa$ /TaN TFT on flexible PEN without and with HfLaO passivation.

Channel Materials	Channel layer thickness (nm)	Gate Insulator Materials	SS (V/ decade)	$\mu_{EF}$ (cm <sup>2</sup> /V·s)	I <sub>ON</sub> /I <sub>OFF</sub>	Operating Voltage (V)
Flexible ZnO [1]	10	Al <sub>2</sub> O <sub>3</sub>	_	~32	~108	8
Flexible MoS <sub>2</sub> [2]	~2.6	hBN	_	~40	>104	80
Rigid ITO/ IGZO [22]	5/70	SiO <sub>2</sub>	~0.25	104	>107	15
Rigid ZnON [23]	50	SiN <sub>x</sub> /SiO <sub>2</sub>	0.8	~115	>106	20
Flexible This Work	20	HfO <sub>2</sub> /TiO <sub>2</sub> /SiO <sub>2</sub>	0.103	345	$7 \times 10^{6}$	2

**Table 1.** Device performance comparison among flexible ZnO, MoS<sub>2</sub>, and HfLaO-passivated ZnO TFTTs (this work). The IGZO and ZnON TFTs on rigid glass substrate were also added for comparison.

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charges and dangling bonds also found in the interim  $SiO_x$  region between  $SiO_2$  and Si body, the origin of positive fixed oxide charges in  $SiO_2/Si$  metal-oxide-semiconductor field-effect transistor (MOSFET) shown in text book. On the other hand, the OH bonding signal in XPS spectra of Fig. 5(b) is much lowered for HfLaO passivated ZnO device. It is well known the high- $\kappa$  gate dielectric will absorb the moisture<sup>25–29</sup>, especially the La<sub>2</sub>O<sub>3</sub>, which in turn reduce the Zn(OH)<sub>2</sub> formation.

The high-density positive  $\Delta Q_p$  further causes Fermi-level closer to valance band, increases the ZnO depletion region, and lower the n-type ZnO conduction, as shown in the schematic diagrams of Fig. 6. The electron wave-function in a MOSFET typically distributes over 20 nm<sup>30</sup>; therefore the high-density  $\Delta Q_p$  will also increase electron scattering rate and decrease mobility. However, the passivation does not affect the gate EOT, because the EOT of a TFT only counts the dielectric next to the gate. Because proper passivation blocks the reaction between H<sub>2</sub>O and ZnO, the OH bonding in HfLaO/ZnO is much reduced to lower  $\Delta Q_p$  and potential barriers at grain boundaries. This in succession leads to much higher mobility, because the ZnO has overlapped s-orbitals for conduction.

Table 1 compares the device performance of various materials on flexible and rigid substrates. The mobility of HfLaO-passivated ZnO TFT is higher than the IGZO and ZnON TFTs on rigid substrate<sup>22, 23</sup> that is also the record highest value for TFTs on flexible substrate<sup>1–7</sup>. This is possible because the poly-crystalline material always has better material quality and higher mobility than amorphous structure, and the mobility improvement can be as large as ~100 times for poly-Si versus amorphous-Si TFTs. The very high mobility ZnO TFT with excellent SS, large  $I_{ON}/I_{OFF}$  and low V<sub>D</sub> are vital for both DC and AC power saving. The simple process and low material cost of nano-crystalline ZnO device should have strong impact on next generation display, as long as OH bonding related charge traps and grain boundary potential barriers are improved by proper passivation. The achieved high mobility on amorphous material is also the enabling technology for high-speed 3D brain-mimicking chip<sup>24</sup>.

In conclusion, very high mobility, excellent SS, large  $I_{ON}/I_{OFF}$ , low  $V_D$ , and low power operation were achieved in ZnO TFT device that is crucial for display and 3D IC. The excellent device integrity is due to the novel passivation scheme with simple process.



**Figure 4.** (a) SIMS depth profile of ZnO on  $HfO_2/TiO_2/SiO_2$  stacked gate dielectrics, (b) Cross-sectional TEM and (c) XRD spectra of ZnO/high- $\kappa$ /TaN structure on flexible PEN substrate.



**Figure 5.** XPS spectra of ZnO/high- $\kappa$ /TaN structure on flexible PEN substrate (**a**) without and (**b**) with HfLaO passivation. Here the passivated HfLaO was removed for XPS measurement.



Figure 6. Schematic ZnO/high- $\kappa$ /TaN energy bands and nano-crystalline-ZnO band structures on flexible PEN without (left) and with (right) HfLaO-passivation.

#### Methods

The bottom-gate ZnO/high-ĸ/metal-gate TFTs were made on flexible polyethylene naphthalate (PEN) substrate. In addition to its low cost, the PEN substrate has good properties of a low linear thermal expansion coefficient, surface smoothness, and optical clarity. A 300-nm smoothing SiO<sub>2</sub> layer was first deposited on PEN substrate. Then the 60-nm TaN gate metal, tri-layer gate dielectrics of 50-nm HfO<sub>2</sub>, 40-nm TiO<sub>2</sub> and 4-nm-SiO<sub>2</sub>, and a 20-nm ZnO active layer were deposited by physical vapor deposition (PVD). Then the Al source/drain (S/D) electrodes was formed. Finally, the device was passivated by 20 nm thick HfLaO dielectric with opened S/D probing window. The TaN gate electrode was deposited by sputtering at a power of 800 W, Ar/N<sub>2</sub> of 100/10 sccm, and a pressure of  $3 \times 10^{-3}$  torr. The gate dielectric stacks were deposited by electron-gun evaporation at 5 KV, and the deposition rates were 0.24/0.2/0.1 Å/sec, respectively. The ZnO channel were deposited by sputtering at a power of 100 W, Ar/O<sub>2</sub> of 20/5 sccm, and 1 Å/sec deposition rate. The Al source-drain was deposited by thermal evaporation deposition. The HfLaO was deposited by electron-gun evaporation at a deposition rate of 0.15 Å/sec. Before deposition, the chambers were pumped down to  $3 \times 10^{-6}$  torr. The low deposition rate is important to reach good quality. No post-deposition annealing was used that is the merit of this work. The gate size of fabricated TFT is 48-μm × 505-μm. To investigate the large mobility improvement, X-ray diffraction (XRD), secondary ion mass spectrometry (SIMS), cross-sectional transmission electron microscopy (TEM), and X-ray photoelectron spectroscopy (XPS) were used to analyze the material property. Very low etching rate of 0.2 Å/sec was used in the XPS measurement due to the thin 20 nm HfLaO passivation layer.

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#### **Author Contributions**

C.W. Shih did the experiments; Albert Chin wrote the main manuscript text. All authors have given approval to the final version of the manuscript.

#### Additional Information

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The results of this research have important financial interests for both Display, ultra-low power 3D IC and CTFT.

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