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ELECTRONICS

Welcome to the holodeck

> It is possible to realize electroholography with current technology by making the calculation algorithm circuitized and highly parallelized

Holograms are 3D reconstructions of objects or images, and have long been a key element of science fiction. In the real world, holographic 3D image systems could mark the future of how humans interact with the virtual world. However, challenges in generating the required computing power with high speed have hampered the realization of video holography thus far. Now, Ito and colleagues, writing in *Nature Electronics*, demonstrate that an array of large-scale field-programmable gates (FPGAs) can be used to generate video frame-rate holograms in real time.

The computational power required to display a 3D hologram is about 10^6 times higher than for a typical 2D display. Moreover, real-time processing of a holographic 3D image, which requires an enormous amount of information, demands parallel and distributed computer systems. "The biggest problem is the computational complexity. It is impossible to create holographic videos even on current high-speed computers," explains Ito. "Additionally, in conventional parallel computation, the computation speed conversely decreases with the number of parallel calculations."

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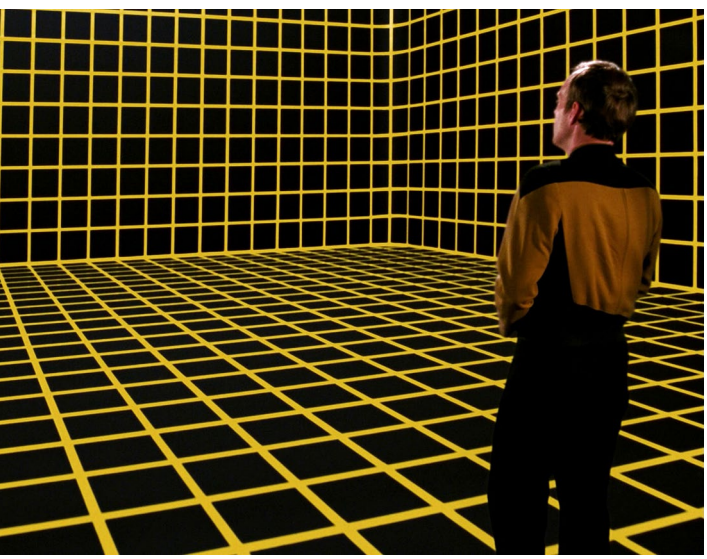

Ito and colleagues report their 8th prototype of a holography computing board, HORN-8 (HOlographic ReconstructioN), which integrates large-scale holographic calculation circuits and parallel processing technology. The HORN-8 board is composed of seven computational and one communication FPGA and the circuits are densely packed, allowing for the use of short wires and, thus, enabling parallel computation and fast speed.

In this system, the 3D image is represented by a point cloud model, that is, the image is described by a specific number of object points in space. The hologram is then generated by calculating the light waves propagating between the object points, with each hologram pixel being independently calculated. Using this setup, the HORN-8 board can process more than 35,000 calculations in parallel and, owing to a new cosine calculator, does not need memory. Importantly, the system can operate at high speed. "The most important outcome of our research is that the 'communication bottleneck' problem of parallel computing can be mitigated and the calculation speed increases with the number of calculation circuits," says Ito. "Therefore, it is possible to realize electroholography with current technology by making the calculation algorithm circuitized and highly parallelized."

The HORN-8 board can be applied to display 3D holograms. The researchers demonstrate the real-time generation of a $10{,}000 \times 10{,}000$ pixel hologram in 100 milliseconds. Moreover, in 125 seconds, a 100 million pixel hologram can be reconstructed at a pixel pitch of 1 μm from a 10 million-point object by dividing the object data into blocks, although not in real time.

However, the computational speed achieved with the HORN-8 is not yet applicable for real-time videos and there are currently no high-definition large-scale systems available to display the holograms. Additionally, to achieve high parallelism, the size of the system needs to be further reduced. "We are currently developing the HORN chip, which integrates the calculation circuit and a high-definition electronic display device," says Ito. The researchers envision the implementation of the HORN chip in head-mounted displays for virtual reality systems, which is an important milestone on the road to realizing video holography.

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ORIGINAL ARTICLE Sugie, T. et al. High-performance parallel computing for next-generation holographic imaging. *Nat. Electron.* https://doi.org/10.1038/s41928-018-0057-5 (2018)
FURTHER READING Chu, D. Video-rate holograms power up. *Nat. Electron.* https://doi.org/10.1038/s41928-018-0060-x (2018)