Testing memory downsizing limits

The constantly growing needs for data storage call for new memory technologies and downscaling strategies.

Our digital society continuously generates a massive amount of data that is subsequently processed and stored. Quantitatively speaking, some of the latest estimations predict that in a few years from now, nearly 2 MB of data will be created every second for every person on Earth. In data storage terms, this would mean even more physical space needed for memory. To slow down this costly expansion, the manufacturers have resorted to their preferred coping strategy — downscaling. The success of this approach, which so far has enabled decades of steady memory shrinking, primarily stems from the extensive use of advanced nanofabrication techniques, such as photolithography, high-aspect-ratio etching and thin-film deposition.

The physical separation of memory and computing inherent in the von Neumann architecture, as well as different functionality and design of logic and memory cells, has driven the two technologies apart in terms of the evolution of their design and technological nodes so far. Data storage devices based on CMOS (complementary metal-oxide semiconductors) were never meant to be as small as FinFETs, yet Flash, the most common type of non-volatile memory, has become the most aggressively scaled technology among electronic devices¹. Although state-of-the-art NAND and NOR devices based on floating gate transistors were thought to be restricted to node sizes of 20 nm and 45 nm, respectively, advances in nanofabrication combined with the multi-level cell approach and vertical layer stacking opened up opportunities to realize an even smaller cell pitch and significantly boost memory density. However, even the current 64-layer 3D NAND technology² merely delays the end of the Flash era, as further downscaling will inevitably result in larger cell-to-cell interference, higher channel resistance and lower data retention.

Despite the ongoing optimization of the current 3D memory design, the semiconducting industry has been actively exploring alternative memory technologies. Among thickness-limited ferroelectric random access memory (FeRAM), power-thirsty magnetic RAM (MRAM), and phase-change RAM (PCRAM) with serious stability issues, resistive RAM (RRAM), albeit far from mature, is generally considered a worthwhile memory technology with promising all-round

Fig. 1 | Transmission electron micrograph of a 3×3 memristor crossbar array with a device area of $2 \times 2 \text{ nm}^2$ and a 6-nm half-pitch. Scale bar, 10 nm. Reproduced from ref. ⁴.

performance characteristics. In particular, memristor-based³ RRAM is more than just a memory device in that it offers a totally new ‘transistorless’ low-power electronics concept that in the ideal world could help to overcome the von Neumann bottleneck, and could bring memory and logic physically closer together, similar to the intimately connected synapses and neurons in the human brain.

Thus far, a simple memristor crossbar architecture has been used to demonstrate non-volatile memory, artificial neural networks and brain-like computing platforms. However, little effort has been dedicated to testing the downscaling limits of this memristor architecture. In *their paper* in this issue of *Nature Nanotechnology*, Pi et al.⁴ develop a nanofabrication method to create crossbar arrays based on a titanium oxide/hafnium oxide switching layer with a feature size of 2 nm and 6-nm half-pitch. The information density in a single layer is comparable to that in the state-of-the-art 64-layer 3D NAND.

The main achievement of their nanofabrication approach lies in the realization of a ‘nanofin’ structure. The nanofins that serve as contacts in the memristor arrays feature a 2-nm Pt thin film deposited on a Ge wetting layer of comparable thickness. The Pt/Ge layers are evaporated onto a SiO_2 trench with a high

height-to-width aspect ratio (up to 1,500). Subsequent patterning and deposition of two Cu contact pads and an alumina isolation layer complete the fabrication process, which has to be repeated several times to produce a multi-fin array. Remarkably, the resistance of the fabricated nanofin is smaller than that of a 2-nm-wide Cu wire and several orders of magnitude lower than the resistance of a carbon nanotube of comparable diameter. This feature is especially notable as it solves the issue of high electrode resistance that typically limits the device performance at the nanoscale. According to the authors, the Pt nanofins with a scaling limit of just 1 nm can be produced with 100% fabrication yield. Moreover, the demonstrated high-density electronic circuit has low leakage current and negligible device crosstalk, one of the major concerns for 3D NAND. Apart from showing non-volatile switching behaviour, the researchers were able to program nine pixels in a 3×3 memristor array (Fig. 1) to store information such as letters and images by individually addressing each intersection in the crossbar array.

The extreme downscaling has some negative effects on the memristor performance, but proper optimization should solve the problem. Also, although the fabrication process for the nanofin crossbar arrays is compatible with other semiconductor technologies, it is still too complex and time-consuming, with the multiple deposition sequences posing a serious engineering challenge to the upscaling of the technology. Despite many unresolved issues, which naturally occur at this early stage of research, the result demonstrates the downscaling potential of the crossbar architecture at scales smaller than the cutting edge of semiconductor manufacturing and its promise for applications in high-density, low-power data storage and processing. □

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References

1. IEEE International Electron Devices Meeting (IEDM), 1.1.1–1.1.8 (2016).
2. Lee, S. et al. in *Proc. IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, 340–342 (IEEE, 2018).
3. Strukov, D. B., Snider, G., Stewart, D. & Williams, R. S. *Nature* **453**, 80–83 (2008).
4. Pi, S. et al. *Nat. Nanotech.* <https://doi.org/10.1038/s41565-018-0302-0> (2018).