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Nanomeshed Si nanomembranes

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One of the main challenges in stretchable electronics is to achieve high-performance stretchable semiconductors. Here, we introduce an innovative concept of nanomeshed semiconductor nanomembrane which can be regarded almost as intrinsically stretchable to conventional microelectronic layouts. By making a silicon film into homogeneous nanomeshes with spring-like nano traces, we demonstrated a high electron mobility of 50 $cm^2/V{\cdot}s$, and moderate stretchability with a one-time strain of 25% and cyclic strain of 14% after stretching for 1000 cycles, further improvable with optimized nanomesh designs. A simple analytic model covering both fractional material and trace sidewall surfaces well predicted the transport properties of the normally on silicon nanomesh transistors, enabling future design and optimizations. Besides potential applications in stretchable electronics, this semiconductor nanomesh concept provides a new platform for materials engineering and is expected to yield a new family of stretchable inorganic materials having tunable electronic and optoelectronic properties with customized nanostructures.

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INTRODUCTION

Stretchable electronics have emerged as promising platforms for many important areas such as bio-mimetics, health monitoring, biomedical therapeutics, and soft robotics.[1–6] Due to their low modulus, these stretchable platforms can either serve as artificial electronic organs or form more conformal and compatible interface with irregular, shape-evolving or soft objects.[7–9] Compelling examples of such applications include electronic skin demonstrations from various stretchable active matrices[10–12] and multifunctional balloon catheters for cardiac electrophysiological mapping and ablation therapy.[13–16] Historically, core material elements in conventional high-performance electronics are inorganic single crystals such as silicon (Si) or compound semiconductors, which arguably laid the foundation for modern society.[17–19] However, those materials are usually rigid. Great efforts have made these semiconductors in thin film structures and render them flexible, but they are still brittle, making it difficult to achieve stretchable devices. Seeking stretchable electronic components, especially stretchable semiconductors with high performance, therefore, has been one of the critical challenges in achieving next-generation stretchable electronics.

In the past decade, there has been significant progress in realizing stretchable semiconductors, mainly from two complementary ways. One approach involves designing novel microstructural layouts in standard materials, as exemplified by configuring inorganic semiconductor based circuits into microscale island-bridge layout.[20–23] The other centers in developing intrinsically stretchable components such as organic semiconductors[24–27] and nano-wire or nano-tube networks.[28–30] Among all existing approaches, microscale structuring often lacks the high-density advantage in modern microelectronics, which has been exploited to the extreme level under what's commonly known as Moore's law. On the other hand, intrinsically stretchable semiconductors currently are still quite limited in their mobility and/or reliability, with typical electron mobility still less than 10 $cm^2/V{\cdot}s$,[31–33] while bottom up assembled networks such as carbon nanotube webs are limited by their uniformity.[34,35] Existing approaches are still incompetent when high-density, high-performance stretchable electronics are needed.

Here, using Si as a model system we conceptualize and demonstrate a new stretchable semiconductor platform, namely nanomeshed Si nanomembranes. The nanomeshed nanomembrane is a dense network of fully connected, single-crystalline Si traces of nanoscale line-width and thickness. Due to their spring-like traces, the semiconductor nanomeshes possess promising stretchability while with high electrical performance and high scalability to microscale footprints. This latter property renders semiconductor nanomeshes almost as intrinsically stretchable for microelectronic layouts. As a proof of concept, we achieved nanomeshes of Si with tunable trace widths from a lift-off and transfer process using a Si-on-insulator (SOI) wafer, with nanomesh pattern defined by two different soft lithography methods. To facilitate the nanomesh transfer and provide additional mechanical support, we further introduced a bilayer structure of Polyimide (PI)/Si nanomeshes on elastomer substrates to improve the stretchability. The Si nanomesh film with a peak effective mobility of 50 $cm^2/V{\cdot}s$ has demonstrated a one-time stretchability of up to 25% strain, and robust cyclic stretchability with less than 10% fatigue after 1000 stretching cycles with a constant strain of 14%. An analytical model coupling factors from both the fractional material and trace sidewall surfaces predicted the mobility trend of the Si-nanomesh transistors as a function of fractional Si, indicating that the mobility can be enhanced with future surface passivation. Together these results demonstrate nanomeshing semiconductors as a unique and promising pathway towards high-density, high-performance stretchable microelectronics.

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RESULTS

Materials characterization and fabrication of stretchable single-crystalline nanomeshed Si nanomembranes

The nanomeshes consist thin, curvilinear nano-traces of single-crystalline Si densely connected with each other, and they can be bonded onto Polydimethylsiloxane (PDMS) or other elastomer substrates with Si–O chemical bonding for mechanical support. The mechanical, electrical and other properties of the Si nanomeshes are expected to be determined by the properties of the original Si and the structure of the nanomeshes. As shown in the photograph and images from atomic force microscopy (AFM) and scanning electron microscopy (SEM) (Fig. 1a), the Si nanomeshes can be achieved at cm scale with high uniformity and without any missing traces. Figure 1b illustrates the schematic of a stretchable Si-nanomesh film. These spring-like traces can be deformed to accommodate the applied strain which makes the nanomesh network stretchable. Here, an additional PI layer also exists underneath the Si, forming bilayer nanomeshes, further providing mechanical support. Figure 1c presents the Raman spectra of the Si nanomeshes and a single-crystalline Si (sc-Si) wafer. The transverse optical (TO) Raman peak is observed at 520 cm^{-1}, which is in good agreement with sc-Si. X-ray diffraction (XRD) characterization (Fig. 1d) shows that Si nanomeshes also have the same strong and sharp diffraction peak from the (400) plane of Si as sc-Si with comparable values of full width at half maximum (FWHM) of 0.16° for Si nanomeshes and 0.12° for Si wafer. The XRD and Raman results confirm the single-crystalline nature of the Si nanomesh traces, which is critical to achieving superior carrier transport properties.

To fabricate stretchable Si nanomeshes, we first patterned the Si film into nanomeshes in the SOI source wafer, then transferred them onto a PDMS substrate (Fig. 1e). Here, we modified the

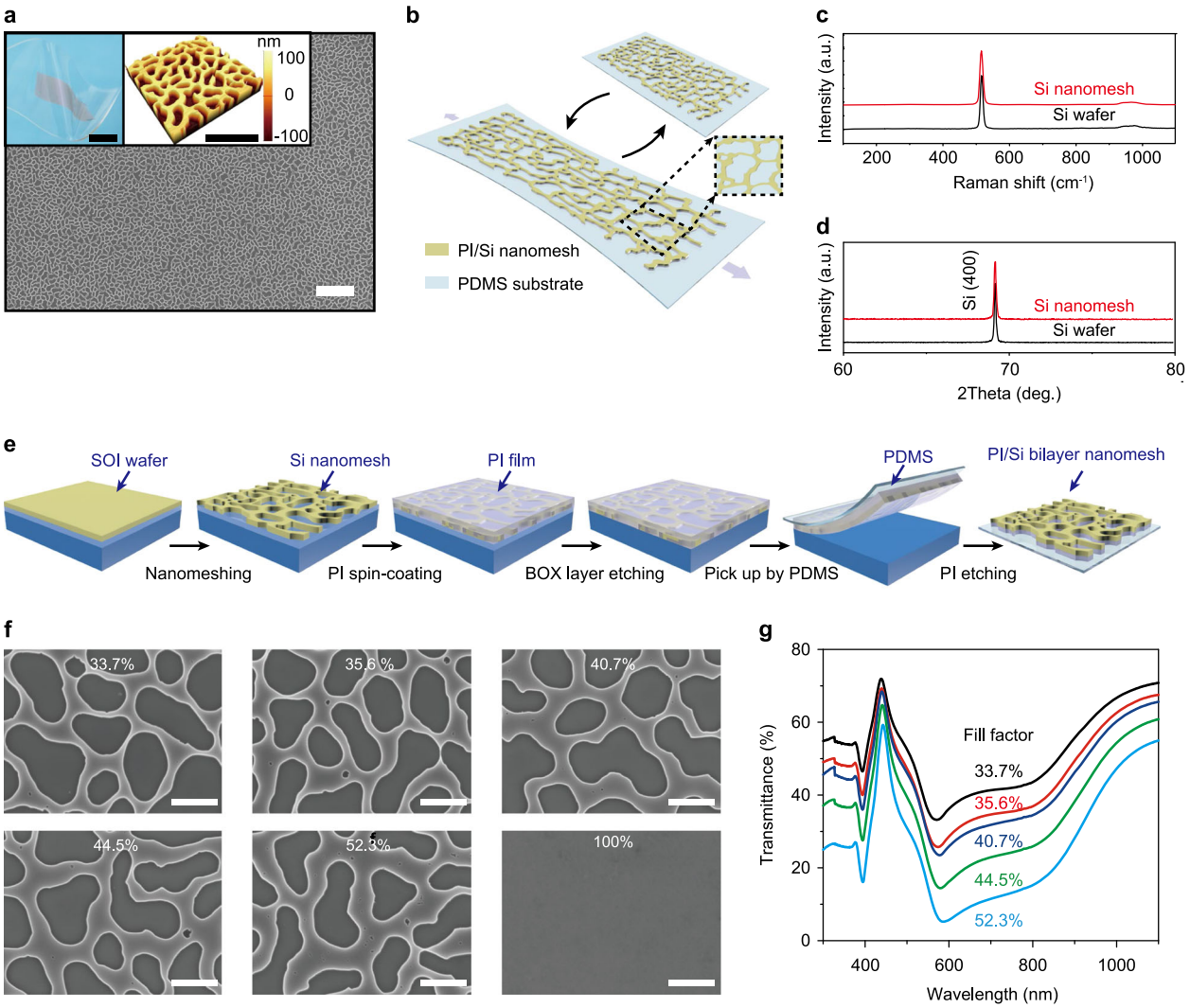

Fig. 1 Materials characterization, fabrication and optical properties of nanomeshed Si nanomembranes. **a** A scanning electron microscope (SEM) image of a Si-nanomesh film. The left inset is a photograph of the Si-nanomesh film on a twisted PDMS substrate. The right inset is an atomic force microscope (AFM) image of an area in the Si nanomeshes. The scale bar in **a**, left inset and right inset are 10 μm, 5 mm and 5 μm, respectively. **b** Schematic illustration of the stretchable PI/Si bilayer nanomeshes on the PDMS substrate. Raman spectra (**c**) and X-ray diffraction pattern (**d**) of Si nanomeshes (red) and a single-crystalline Si wafer (black), showing the single-crystalline nature of Si traces. **e** Schematic illustration of the transfer process to achieve stretchable PI/Si bilayer nanomeshes. This process starts by forming the Si layer in an SOI wafer into nanomeshes from a modified In grain boundary lithography and dry etching. An ultrathin PI film secures the nanomeshes during the wet etching of the buried oxide (BOX) layer. After being picked up by PDMS, patterning the PI film using Si nanomeshes as a self-aligned mask completes the formation of PI/Si nanomeshes. **f** SEM images of the Si nanomeshes with different fill factors controlled by the HNO_3 etching in the In grain boundary widening. The scale bar is 1 μm. **g** Transmittance spectra of Si nanomeshes with different fill factors in the wavelength range of 300–1100 nm

Indium (In) grain boundary lithography method[36,37] as an exemplar, large-scale, soft lithography approach to form the Si nanomesh pattern. This process utilizes self-formed In grain boundaries to achieve Cr nanomeshes on the source SOI wafer (Si thickness, $t_{Si} = 145$ nm), followed by Si dry etching with Cr nanomeshes as the mask (Supplementary Fig. 1). Removal of Cr completes the fabrication of Si nanomeshes in the SOI wafer. After the Si nanomesh formation, a simple transfer process achieves freely stretching Si nanomeshes onto PDMS substrates (Fig. 1e). An ultrathin PI layer secures the Si nanomeshes during the transfer process. After being picked by PDMS substrate, the PI layer was patterned by using Si nanomeshes as a self-aligned mask. The PI layer finally forms a bilayer nanomesh structure with Si, providing additional support for the Si nanomeshes during mechanical deformation. Detailed fabrication parameters can be found in the Methods section. We envision that similar fabrication processes can be applicable to a variety of other semiconductors and inorganic materials.

The trace width of Si nanomeshes can be tailored from this fabrication process (Supplementary Fig. 2). The SEM images of the Si nanomeshes with different trace widths and fill factors (defined by the occupation percentage of Si in the nanomeshes over a given microscale area, e.g., $10 \times 10\ \mu m^2$) are shown in Fig. 1f, along with the image of a Si full film. As another proof of concept, we also demonstrated free-standing, non-stretchable Si nanomeshes from nanosphere lithography with circular nanomesh openings (Supplementary Fig. 3). We note that previously non-free-standing Si nano-networks have been achieved for thermoelectric applications by either a superlattice nanowire lithography technique or electron-beam lithography,[38,39] however, there has not been any work in utilizing substrate-detached semiconductor nanomeshes for stretchable electronics nor studying relevant properties.

Optical properties of Si nanomeshes

The optical transmittance measurement reveals the optical properties of Si nanomeshes, which are transferred onto glass substrates for easy handling. Figure 1g illustrates transmittance spectra of Si nanomeshes with different fill factors in the wavelength ranging from 300 to 1100 nm. There are two prominent trends as the fill factor changes. First, as expected, the transmittance increases as the fill factor decreases, since there are less Si to absorb light. As a result, the transmittance of Si nanomeshes with the fill factor of 33.7% is larger than 35% over the entire measurement window. Compared with the transmittance spectra of a Si full film transferred from the same SOI wafer (Supplementary Fig. 4), transmittance through Si nanomeshes in certain wavelength regimes is lower, largely owing to the larger reflection from the textured surface of the nanomeshes. Second, both the absorption peak at 400 nm and 600 nm show blue shifts with decreasing fill factor. These shifts are intriguing, given that trace widths are on the order of a couple of hundred nm, and well above the exciton Bohr radius of Si (~only a few nm), therefore the quantum confinement effects should not be dominating. We attribute this phenomenon to the change of the volume modes of the Si trace dielectric waveguides. Indeed, previous theoretical and experimental studies on Si nanowires reveal that the wavelength λ of the photonic modes in the nanowires scale proportionally with their diameter d, with the position of the absorption peaks all moving to high energies when decreasing the nanowire diameter.[40] To a certain extent, the Si nanomeshes can be regarded as a network of nanoscale traces which are similar to nanowires. The exact relationship between λ and the trace width is yet to be determined in the nanomesh case here by considering the large variation in the trace width (as shown in Supplementary Fig. 2a), as well as the curvilinear nature of the nanoscale traces. However, the shift directions are the same between nanomeshes and nanowire arrays. Transmittance result of the circular nanomesh (Supplementary Fig. 5) also reveals similar trends.

Transport properties of nanomeshed Si nanomembranes

To study the carrier transport properties of Si nanomeshes, we fabricated and investigated N-channel metal-oxide-semiconductor (NMOS) transistors based on Si nanomeshes (Fig. 2a). Devices are made and studied on the SOI source wafer for easy gating while still revealing nanomesh properties. The source and drain nickel (Ni) contacted Si parts are heavily n-type doped and the channel is lightly p-type doped. Gate voltage is applied from the Si handle wafer with the 120-nm-thick BOX layer as the gate dielectric. The sheet resistance and contact resistance of the Si nanomesh transistor are 29.05 kΩ/sq and 2.16 kΩ, respectively, which are calculated through the transmission line measurement (Supplementary Fig. 6). The results are similar to those of previous poly-Si nanosheet transistors with nickel silicide contact after channel width normalization.[41] The transfer characteristics of a Si-nanomesh (52.3% fill factor) transistor (channel length $L = 40\ \mu m$, width $W = 35\ \mu m$) exhibit a clear NMOS switching behavior, with a high ON/OFF current ratio (I_{ON}/I_{OFF}) of over 10^5 (Fig. 2b). Above the threshold voltage (V_{th}) of -1.5 V, the drain current (I_d) increases nearly linearly as gate voltage (V_g) increases, indicating that neither the mobility (μ) is degrading at high electrical field nor the contact resistance is limiting the current conduction. The device exhibits clearly linear *I-V* characteristics at low drain voltage (V_d) region, also indicating Ohmic S/D contacts (Fig. 2c). The current saturation at high V_d region also matches with typical long-channel transistor behaviors. The OFF-state currents will not be influenced by the nanomesh fill factor, while the ON-state current increases with the fill factor, resulting in a small increase of the I_{ON}/I_{OFF} ratio (Supplementary Figs 7 and 8). Figure 2d presents extracted effective mobilities as a function of the gate voltage for nanomeshes with different fill factors. The transistor extracted parameter for the mobility calculation are summarized in the Supplementary Table 1. The mobility of all Si nanomeshes first increase at low values of V_g, then reach a peak, and finally decrease, consistent with a typical screening-scattering transition. Notably, we achieved peak effective mobilities from 50 $cm^2/V{\cdot}s$ to 95 $cm^2/V{\cdot}s$ at fill factor from 33.7% to 52.3%. The mobilities of Si nanomeshes are smaller than values expected from a 'dilution' perspective from the full-film Si transistor (with $\mu \sim 615\ cm^2/V{\cdot}s$, see Supplementary Fig. 9), where we can simply calculate the mobility of Si nanomeshes from multiplying the mobility of Si full film by the Si fill factor in the nanomesh. However, they are significantly higher compared to other stretchable semiconductors, where the mobilities are typically much less than 10 $cm^2/V{\cdot}s$. Understanding the fundamental transport properties therefore is encouraging to exploit the full potential of semiconductor nanomeshes.

Modeling of the carrier transport in nanomeshed Si nanomembranes

The mobility deviation of Si nanomeshes from the simple dilution perspective is intriguing. To shed light on the structure-property relationship of Si nanomeshes regarding their carrier transport properties, we constructed a simple analytical model, where the key point is to consider the Si-nanomesh film as a new material (Fig. 3a). The structure of a Si-nanomesh film will be determined by its nanomesh pattern, trace width, in addition to the Si film thickness. We hypothesize that there are two factors that mainly contribute to the nanomesh mobility: one is the fractional Si material, the other is the surface scattering from the sidewalls of the nanoscale traces. To simplify the analysis, we consider a Si-nanomesh film with a fixed nanomesh pattern and film thickness, while with shrinking trace width. As the trace width decreases, the fractional Si material reduces, which is represented by the

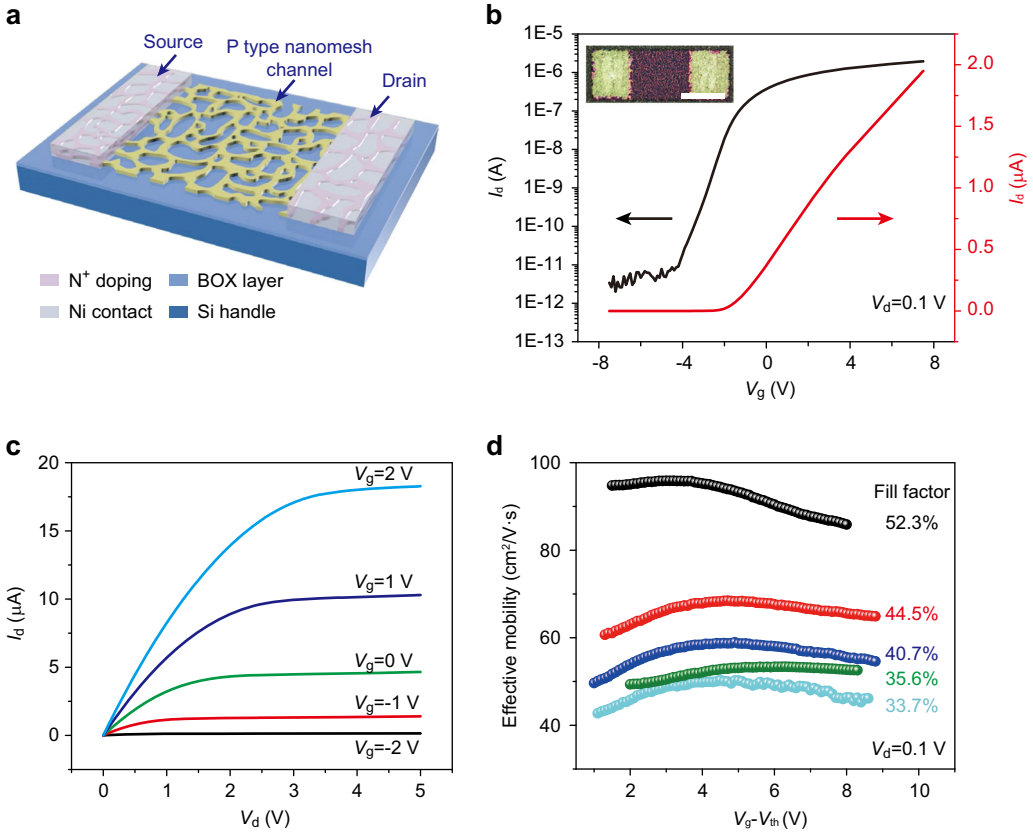

Fig. 2 Carrier transport properties of Si nanomeshes. **a** Schematic of a Si nanomesh transistor. The device is fabricated on an SOI wafer with 100-nm-thick Ni as the source-drain contact, a 120-nm-thick buried SiO_2 layer as the dielectric, and Si handle wafer as the global back gate. **b** Transfer characteristics of the Si-nanomesh transistor with 52.3% fill factor on a log scale (left y-axis) and a linear scale (right *y*-axis) at a drain voltage of 0.1 V. The channel width and length are 35μm and 40μm, respectively. The inset is the optical image of the as-fabricated device. The scale bar is 20 μm. **c** Output characteristics of the same device shown in **b** at gate voltage steps from −2 V (bottom) to 2 V (top). **d** Extracted effective mobility from transistors of nanomeshes with different Si fill factors as a function of gate voltage

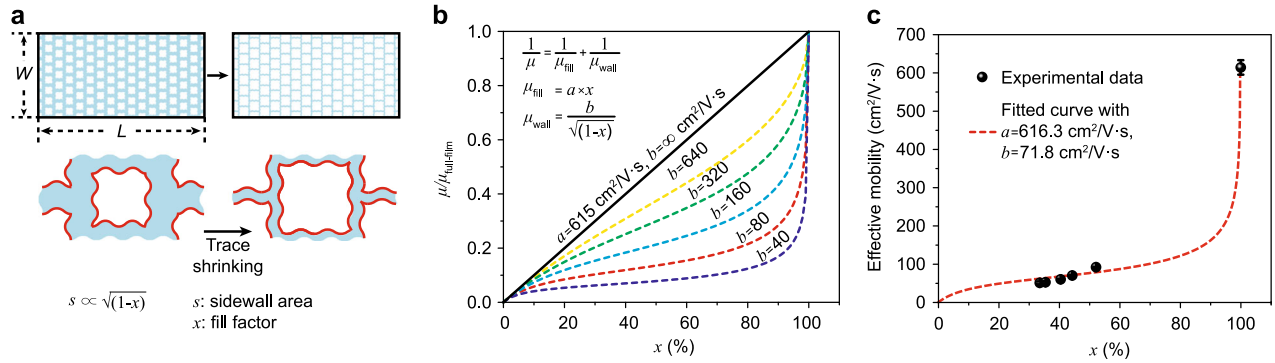

Fig. 3 Carrier transport modeling in Si nanomeshes. **a** Schematic concept of the analytical modeling which regards the nanomesh film as a new material. Assuming the same nanomesh openings (indicated by the white areas among the light blue material parts) for the entire $W \times L$ area, the sidewall circumference (indicated by the red curves) will then always be proportional to the square root of the mesh-opening area, which is a natural consequence of the theorems about similar figures. The sidewall area (*s*), equal to the sidewall circumference times the film thickness, will therefore also be proportional to the square root of $(1 - x)$. **b** Dependence of nanomesh mobility on fill factor which is affected by fractional material (μ_{fill}) and scattering of trace sidewall (μ_{wall}) using "Matthiessen's Rule". Here μ_{fill} and μ_{wall} are approximated as $a \times x$ and $b/\sqrt{1-x}$ respectively, where *a* and *b* are materials and surface dependent prefactors. **c** Fitting of experimental effective mobility of semiconductor nanomeshes as a function of fill factor using the analytical model here. A fitting curve with $a = 616.3$ cm^2/V·s and $b = 71.8$ cm^2/V·s matches closely with experimental data

shrinking of the blue area in Fig. 3a. If we denote *x* as the fill factor of Si in the $W \times L$ channel area, neglecting the scattering from the trace sidewalls, the fractional-material induced mobility (μ_{fill}) can be calculated as $a \times x$ to the first order as we have discussed in the dilution perspective, where *a* is a constant with a value equal to full film mobility, $\mu_{full\text{-}film}$.

On the other hand, there are increasing sidewall areas if the nanomesh trace narrows. Assuming all nanomesh openings have

the same shape for in the entire $W \times L$ area, the sidewall area (s), equal to the sidewall circumference times the film thickness, will therefore be proportional to the square root of $(1 - x)$. If assuming proportional scattering from the sidewall, the sidewall-area induced mobility (μ_{wall}) will then be $b/\sqrt{1-x}$, where b is a prefactor related with sidewall surface quality. To include effects from both the fractional material and trace sidewall scattering, we approximate the combination of their influences by using "Matthiessen's Rule":

$$\frac{1}{\mu} = \frac{1}{\mu_{fill}} + \frac{1}{\mu_{wall}} \quad (1)$$

where μ is the mobility of the Si nanomesh film. Thus, the dependence of mobility of Si nanomeshes on the Si fill factor can be expressed as:

$$\mu = \frac{abx}{ax\sqrt{1-x} + b} \quad (2)$$

Figure 3b plots the relative mobility curves ($\mu/\mu_{full\text{-}film}$) as a function of fill factor (x) with different a, b values. When the mobility is only dominated by the fractional material (i.e., $b = \infty$), there is a linear relationship between mobility and fill factor as expected. When considering the sidewall surface scattering (finite b values), the mobility shows a sharp decrease as the fill factor reduces. The more the sidewall surface scattering is (decreasing b value), the faster the drop of the nanomesh mobility will be, especially in the initial decrease in the fill factor.

To validate our analytical model, we fit the model to the experimental dependence of peak effective mobility on fill factor x. The curve extracted from Eq. (2) with $a = 616.3\ cm^2/V{\cdot}s$ and $b = 71.8\ cm^2/V{\cdot}s$ is in good agreement with the experimental data (Fig. 3c). This agreement strongly encourages the idea of incurring trace sidewall scattering for carrier transport studies in nanomesh films. This modeling result also suggests that the mobility can be further improved by future surface passivation, which can reduce the trace sidewall surface scattering. The mobility of circular nanomesh transistors shows a similar trend with the ones made by the In grain boundary lithography, and an analytical model with $a = 615.9\ cm^2/V{\cdot}s$ and $b = 94.6\ cm^2/V{\cdot}s$ well fits with the experimental results, validating our approach (Supplementary Fig. 10).

Mechanical stretchability of transferred Si nanomeshes on PDMS

Finally, the bilayer PI/Si nanomeshes also demonstrate promising stretchability. Here a customized automatic stretcher (Supplementary Fig. 11) characterizes the stretchability of the Si nanomeshes. The test was performed at a low speed of 0.05 mm/s to avoid any abrupt strain caused by the high stretching speed. Figure 4a plots the dependence of sheet resistance on tensile strain for PI/Si nanomeshes of 33.7% fill factor on a 1-mm-thick PDMS substrate. The sheet resistance increases nonlinearly as tensile strain with two obvious tendencies. When the strain is smaller than ~20%, the sheet resistance remains nearly unchanged, while at higher strain state a fast increase in resistance occurs. At a small global strain, the nanomesh traces can deform within the plane without exceeding the Si fracture strain limit. Indeed, as shown in the inset SEM image of 14% strain state in Fig. 4a, nearly no cracks or broken traces are observed. The resistance slightly increases in the strain range of 10 to 20%, which may arise from the piezoresistive effect of Si. When the global strain is large, nonreversible breaking of Si traces occurred, as observed from the SEM image of the nanomeshes at a 28% strain state in Fig. 4a. On the other hand, the low-strain stretching is reversible and repeatable. Figure 4b shows the fatigue test with up to 1000 stretching cycles at a 14% strain. No obvious fatigue from the sheet resistance change is observed after the cyclic stretching up to 1000 cycles. Since Si usually fractures at ~1% strain, this 14% stretchability has already achieved an order of magnitude increase of the performance.

Both theoretical and finite element analysis (FEA) models are developed to reveal the advantageous mechanical stretchability of the bilayer PI/Si structure. The models consist of a Si layer of thickness t_{Si}, a PI layer of the thickness t_{PI} and a PDMS substrate that is assumed to be very soft and infinitely thick as compared to the PI or the Si layers as shown in Fig. 4c. The loading is considered to be at the bottom of the PI layer where an applied strain $\varepsilon_{applied}$ extends the original length l_0 to the deformed length of $l_0\varepsilon_{applied}$. As l_0 approaches zero, this model gives the effects of a localized strain. For the theoretical model, the interaction between the PDMS and the bilayer structure is neglected, and the bilayer structure is modeled as a composite beam (equivalent tensile stiffness K_{eff}, bending stiffness B_{eff}, and the neutral axis position h_N can be obtained analytically.[42] The strain in the structure consists of the membrane and bending stress, and the total maximum strain is found to be at the interface between the Si and the PI layers, with the normalized magnitude of

$$\frac{\varepsilon_{max}}{\varepsilon_{max\,0}} = 1 - \frac{t_{PI}}{t_{Si}}\left(\frac{h_N}{t_{Si}} + \frac{12B_{eff}}{K_{eff}h_N t_{Si}}\right)^{-1} \quad (3)$$

where ε_{max0} is the maximum strain in Si when $t_{PI} = 0$. Figure 4d shows the comparison between the results given by Eq. (3) (solid line) and the results given by a 2D finite element model that considers the PDMS substrate, adopting the experimental data of $E_{Si} = 160$ GPa, $\nu_{Si} = 0.22$, $E_{PI} = 2.5$ GPa, $\nu_{PI} = 0.3$ (E, Young's modulus; ν, Poisson's ratio).[43,44] The analytical model predicts the maximum strain in the Si layer very well. Figure 4d also shows that a thicker PI layer significantly reduces the strain in the Si layer, thereby promoting stretchability. For example, when $t_{PI} = 10{\cdot}t_{Si}$, the maximum strain in the silicon is reduced by ~50 times as compared with a structure without the PI layer. This stretchability enhancement in the bilayer nanomesh structure is because the PI nanomesh can prevent the strain localization and redistribute the deformation in the Si traces to make stress uniform.

The FEA model with $t_{Si} = 145$ nm and $t_{PI} = 300$ nm is shown in Fig. 4e to further reveal the strain-stress behavior of the Si nanomeshes. When the nanomeshes are stretched, the stress is distributed in the entire bilayer nanomeshes. Due to the spring-like nano traces, the average stress in the nanomesh film is modest (less than 1 GPa) even at a 20% strain, consistent with our experimental results. With the global strain increasing (to 40% strain, Fig. 4e), the local stress of some traces in the parallel direction becomes greater than its fracture stress of ~2 GPa,[45] leading to possible fractures and a sharp, non-reversible increasing of resistance. This FEA analysis evidently reveals that nanoscale spring-like traces can effectively endure large global strain in semiconductor nanomeshes. Clearly, this stretching behavior will be heavily geometry dependent and we expect the stretchability of Si nanomeshes can be improved by forming more-stretchable patterns in future nanomesh traces.

DISCUSSION

The results presented here demonstrated a new material platform —nanomeshed Si nanomembranes—which are stretchable while with superior carrier transport properties. Devices such as stretchable diodes with large area coverages and/or high densities can be readily achieved, in a way that leverages both metal and semiconductor nanomeshes and conventional microelectronic layout. Future efforts have the potential to engineer the nanomesh pattern and materials surfaces to maximize the performance from Si nanomesh devices. For example, we envision that many previous design concepts such as the horseshoe and serpentine structures[46,47] in microscale wavy structures, and the fractal design[48,49] can also apply to semiconductor nanomeshes

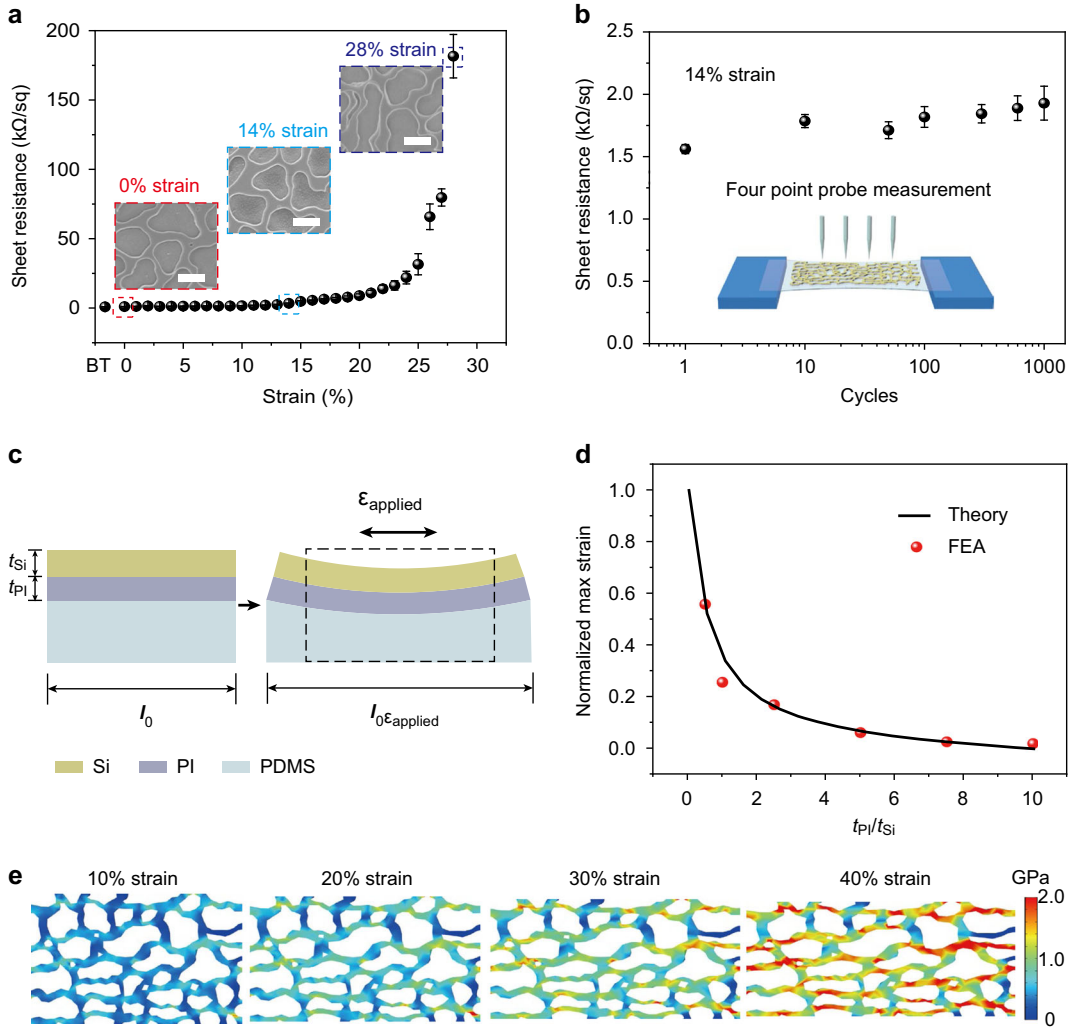

Fig. 4 Stretchability modeling of Si nanomeshes. **a** Sheet resistance of a bilayer nanomesh film with 33.7% fill factor as a function of tensile strain. BT means before transfer. SEM images (inset) of zero, 14 and 28% strain states, showing the microscale stretching behavior of the nanomeshes. The scale bar is 1 μm. **b** Change in sheet resistance versus stretching cycles (up to 1000 cycles) of a bilayer nanomesh film (33.7% fill factor). **c** Schematic mechanics model of the PI/Si bilayer structure on an infinitely thick and soft PDMS substrate. An applied strain extends the bottom of the PI layer from the original length of l_0 to the deformed length of $l_0\varepsilon_{applied}$. **d** The normalized maximum strain $\varepsilon_{max}/\varepsilon_{max0}$ in the Si layer vs the normalized PI layer thickness, as predicted by FEA (dots) and Eq. (3) (solid line). **e** FEA simulation of stress distribution in a PI/Si nanomesh film at 10%, 20%, 30%, and 40% strain state, respectively

for the enhancement of their stretchability. Key challenges to be addressed may lie in developing the fabrication methods to achieve the large-scale semiconductor nanomeshes with user-defined patterns of feature size down to the nanometer regime and at low cost. While using SOI can be uneconomic for many applications, there are certain areas such as in biomedical and clinical applications where the devices from this process could still be affordable. Future process development to replace the SOI process include utilizing deposited amorphous-Si layers as the active material (Supplementary Fig. 12), or transferring Si ribbons from bulk wafers[50] then converting to nanomeshes (Supplementary Fig. 13). Stretchable dielectrics are currently limited by their large leak current, small capacitance and poor environmental robustness. Parallel efforts should also focus on developing nanomesh compatible stretchable thin dielectrics and device miniaturization to fully enable nanomesh-based active electronics. This nanomesh approach is readily applicable to other inorganic materials such as optoelectronic semiconductors (e.g., gallium nitride) and piezoelectric materials (e.g., lead zirconate titanate) to enable stretchability. This work is expected to spur a stream of both fundamental and applied research on nanomeshed forms of existing and new electronic materials.

METHODS

Patterning of Si nanomeshes in a SOI source wafer

As shown in Supplementary Fig. 1, the nanomesh patterning started with a silicon-on-insulator (SOI) wafer which was commercially available (SIMOX SOI, distributed by University Wafer). The SOI wafer consisted of a top Si layer that was a single-crystalline Si with (100) crystal orientation, lightly p-type doped with a doping concentration of 1×10^{14} cm^{-3} and a thickness of 145 nm. The buried oxide layer was 120 nm thick, and the handle wafer was 750 μm thick. In principle, the Si nanomeshes can be achieved through various lithography processes, including electron-beam (e-beam) lithography, stepper lithography, In grain boundary lithography, and anodized-aluminum-oxide template lithography. Here in the patterning process, a Poly(methyl methacrylate) (PMMA) thin film with 500 nm thickness first coated the pre-cleaned SOI wafer. Electron beam (e-beam) evaporation then yielded a 2-nm-thick titanium (Ti) adhesion layer and 20-nm-thick SiO_2 thin film on the PMMA layer. This PMMA layer was to serve as a lift-off resist under the to-be-deposited In grains and the Ti/SiO_2 layer is for a better wetting of In to form irregular grains instead of circular ones.

E-beam evaporation then yielded an In film with a thickness of 250 nm, followed by a 20% HNO_3 wet etching to control the gap between grains. The In grain etching process was an isotropic process, including surface oxidation and acidic etching. The acidic etching was a fast process while the surface oxide layer prevented In from etching away, making the etching rate always under control. Here, the In grains defined the pattern of the final Si nanomeshes, while the gaps between In grains after the HNO_3 etching process determined the Si trace width. After forming clear In grain boundaries, inductive coupled plasma (ICP) (Plasma-Therm, 790) dry etching processes selectively etched the SiO_2 and PMMA layer to expose the SOI wafer under the grain boundary. E-beam evaporation then formed a 30-nm-thick Cr film on the exposed Si. Immersing the wafer in acetone dissolved the PMMA and lift off the In grains and Ti/SiO_2 wetting layer, with the help of a gentle sonication. The steps mentioned above formed a Cr nanomesh mask on top of the SOI wafer, which served as the master pattern to achieve the final Si nanomeshes. ICP Si dry etching process then etched the Si in the SOI wafer with Cr nanomesh mask. Finally a Cr etchant (Transene, 1020AC) removed the Cr nanomesh mask, leaving only Si nanomeshes on the SOI wafer. The Cr mask should be removed immediately to avoid the oxidation of Cr. The thickness of top Si layer therefore defined the Si nanomesh thickness.

Fabrication of silicon-nanomesh transistors

First, plasma-enhanced chemical vapor deposition (PECVD) (SPTS, LpX) deposited a 300 nm-thick SiO_2 film on the SOI wafer as the doping mask. Conventional photolithography then defined the source and drain patterns, followed by the SiO_2 film etching by a trifluoromethane (CHF_3) plasma in ICP system. The diffusion of phosphorus (Filmtronics, P451) then occurred at 950 °C for 5 min in a tube furnace (Thermco, MB-71 Mini Brute Tube). The doping concentration here was quantified from 4-point-probe measurements to be $\sim 6 \times 10^{19}\,cm^{-3}$. After the doping, immersing the wafer in 20% HF for 10 s etched SiO_2 mask film. The process of patterning Si nanomeshes mentioned above was then conducted on the post-doping SOI wafer. After the nanomesh formation, photolithography then defined the transistor area, and an ICP etching with sulfur hexafluoride (SF_6) gas isolated the transistor. E-beam evaporation then yielded Ni layer with a thickness of 100 nm to form contacts with heavily doped Si parts, with photolithography defining the source and drain regions. Immersing the wafer in 30 wt.% iron (III) chloride ($FeCl_3$) solution for 20 s finally isolated Ni contact and completed the back-gated transistor fabrication.

Effective mobility of silicon-nanomesh transistors

The effective mobility of Si-nanomesh transistors was extracted from their transfer characteristics curves by using the equation,

$$\mu = \frac{L}{WC_{ox}(V_g - V_{th} - 0.5V_d)}\frac{\partial I_d}{\partial V_g} \quad (4)$$

where C_{ox} represents the gate capacitance which is calculated from a parallel plate model. Note that the W here is defined as the overall device width, instead of the sum of the Si nanomesh trace widths, since we regard the Si-nanomesh film effectively as a new material.

Transfer of stretchable PI/Si bilayer nanomeshes on a PDMS substrate

Before the transfer process, a high temperature doping step doped the top Si layer in the SOI wafer to a doping concentration of $\sim 5 \times 10^{18}\,cm^{-3}$. The aforementioned soft lithography process then patterned the doped Si into nanomeshes on the SOI wafer. To facilitate the transfer, a 300-nm-thick PI film coated on the post-nanomeshing SOI wafer, followed by curing at 250 °C for 90 min. Immersing the wafer in 20% HF for 1 min then undercut the buried oxide layer through the ultrathin PI layer. Before the lift-off of the PI layer embedding the Si nanomeshes, e-beam evaporation yielded a thin layer of Ti/SiO_2 on the PI film. In parallel, a PDMS elastomer base was mixed at a 10:1 ratio with the curing agent, followed by curing at 80 °C for 1 h to prepare the PDMS receiving substrate. A 1-mm-thick PDMS substrate with a pre-treatment by UV-O_3 plasma for 15 min then picked up the PI layer with Si nanomeshes embedded. After this step, the Si nanomeshes and PI layer were flipped over, resulting that the Si nanomeshes were on top of the PI layer. Finally, an ICP RIE step with O_2 plasma patterning the PI layer with Si nanomeshes as the self-aligned etching mask completed the formation of the stretchable PI/Si nanomeshes on PDMS.

Stretching experiments

The engineering strain was utilized to characterize the stretchability. The strain (e) can be calculated as $e = \frac{\Delta L}{L} = \frac{l-L}{L}$, where L and l are the length of stretchable area in the original and stretching status, respectively. Each stretching cycle consists of one stretching immediately followed by one releasing movement. The test was performed at a low speed of 0.05 mm/s to avoid the external effects caused by the high stretching speed. After the transfer process, the UV-O_3 plasma treated the back side of the PDMS substrate. Two glass pieces fixed the two ends of the PDMS substrate with the nanomesh film by the Si–O bonding, and a 1-cm-wide gap in between the glasses allowed for stretching tests. The sheet resistance during stretching was measured by using the four point probe method.

Materials characterization of Si nanomeshes

We took the morphology and topographic images of the nanomeshes utilizing the scanning electron microscope (Zeiss, Supra 25) and atomic force microscope (Park systems, XE7), respectively. A Raman system (Renishaw) with the 488 nm laser measured Raman spectrum of the nanomeshes. A UV-visible spectrometer (PerkinElmer, Lambda 35) recorded optical spectra in the wavelength range from 300 to 1100 nm. A probe station (EverBeing Int'l corp) connected with a semiconductor analyzer (Keysight, B1500A) measured transport properties of nanomesh transistors.

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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AUTHOR CONTRIBUTIONS

X.H., K.J.S. and H.F. designed the research. X.H. and K.J.S. did device fabrication, tests and performed data analyses and transport modeling. Y.Q., S.V. and S.W. assisted strain simulation. Z.L., Y.Z., X.Z. and P.H. assisted in nanosphere lithography and device fabrication. X.H., S.W. and H.F. co-wrote the manuscript. X.H. and K.J.S. are contributed equally to this work.

ADDITIONAL INFORMATION

Supplementary information accompanies the paper on the *npj Flexible Electronics* website (https://doi.org/10.1038/s41528-019-0053-5).

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