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Direct writing of anodic oxides for plastic electronics

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Metal oxide thin films for soft and flexible electronics require low cost, room temperature fabrication, and structuring processes. We here introduce an anodic printing process to realize the essential building blocks of electronic circuitry, including resistors, capacitors, field-effect transistors, diodes, rectifiers, and memristors directly on imperceptible plastic substrates. Largely independent on surface properties, we achieve high-quality, few nanometer thin dielectric and semiconducting films even on rough substrates via localized anodisation of valve metals using a scanning droplet cell microscope. We demonstrate printing-like fabrication of 3D multilayer solid-state capacitors with a record-high areal capacity of 4 μF cm^{-2}. Applicable to the whole class of valve metals and their alloys, our method provides a versatile fabrication technique for the circuits that empower the flexible and stretchable electronics of tomorrow.

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INTRODUCTION

The accelerating metamorphosis of bulky-in-origin electronics to a flexible, lightweight, and even soft, biomimetic embodiment is changing our perception of technology.[1–7] Applications of soft electronics are expanding rapidly, ranging from consumer devices[8,9] to soft robotics[10–12] and bioelectronic interfaces.[13–15] This change in paradigm demands forming and patterning of dielectrics and semiconductors in thin-film devices in ways that are compatible with low-cost, room temperature fabrication.[16] Metal oxides are a promising materials class as they offer high carrier mobility as semiconductors and high permittivity as dielectrics in thin, flexible form factors.[17–20] Challenges remain in low-temperature processing, pinhole-free layer formation, and facile patterning, especially when applied on unconventional substrates.[21,22] Electrochemical oxide growth in a printing-like manner may help alleviating these issues. The underlying process, anodisation, was first discovered during the search for rectifier elements in the early days of electrical engineering, still reflected in the name of those materials: valve metals.[23] This initial application has since faded but the electrochemical growth of oxides on metals has become a powerful method for passivation instead,[24] and further advanced to a wide range of application fields including electronics,[21] catalysis,[25] dental implants,[26] nano-structuring,[27,28] and even arts or jewelry. A next step is the application in flexible and plastic electronics,[29] owing to the broad variety of oxide properties, achievable through material selection and anodisation conditions. Commonly, fabrication of plastic oxide electronics relies on vacuum deposition of oxides through atomic layer deposition (ALD), molecular beam epitaxy, and sputtering, where remarkable achievements have been made, from single components to working demonstrators.[30–34] The oxides of valve metals like titanium, hafnium, tungsten, and tantalum are used for resistive memories,[35,36] electrochromic devices,[37–39] and electronic components.[40,41] The anodisation of valve metals promises fast, cost-effective, and precise fabrication on large areas at room temperature, vacuum-free, and without involvement of environmentally problematic chemicals.[21,42,43] Even on rough substrates, it generates defect-free layers on nm-scale.[29]

We here present localized anodisation of valve metals as a versatile platform for fabrication of plastic oxide electronic components, circuits, and devices including resistors, capacitors, diodes, transistors, and memristors. A scanning droplet cell microscope (SDCM)[44] acts as an anodic printing head to pattern metal oxide structures in an adaptable, rapid-prototyping-like anodic printing process. With our method, no lithography or mask is needed for structuring oxide layers. We expand the concept of anodic printing further into the third dimension and demonstrate multilayer capacitors with a record-high capacitance per area of 4.2 μF cm^{-2} while retaining a leakage current below 6 nA cm^{-2}. Accurate control over oxide purity and thickness allows fabrication of diodes and memory elements with on–off ratio $> 10^4$ and excellent retention times even on rough plastic substrates. Because anodisation is a low-cost process, its application for anodized oxide electronics may be as common in the future, as it is for passivation today.

RESULTS

Direct writing of anodic aluminum oxide

Printing processes that utilize printing heads allow fast and adaptable fabrication and patterning. We exploit a custom made SDCM as anodic printing head for direct fabrication of metal oxide structures from valve metals (Fig. 1a and S1, details in Materials

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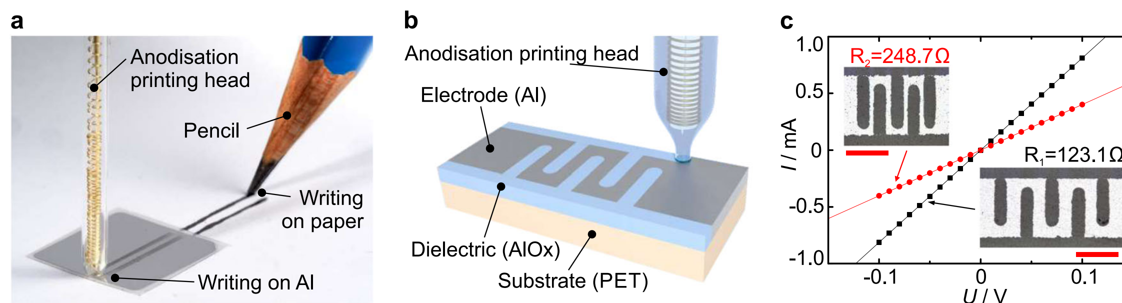

Fig. 1 Direct writing of flexible thin-film resistors. **a** Photograph of the Scanning Droplet Cell Microscope (SDCM) as printing head applied in direct writing of oxides on valve-metal coated substrates. The method is comparable to other writing-like printing processes such as drawing with a pencil. **b** Schematic of resistor meanders fabricated with the anodic printing head. **c** Current–voltage characteristics of two meander structures and their corresponding resistance values together with optical microscopy images of the structures. Larger meanders yield lower resistance values. Scale bars: 500 µm

and methods) to realize printed electronics. Resistors are virtually present in every electric circuit, acting as current limiters, voltage dividers, and in low or high pass filter elements. Meander structures are a way to realize them. We print such resistive structures to form resistors with different geometries (Fig. 1b and SI video 1) on metalized plastic substrates. The anodic printing head is mounted on a three-axis gantry robot, enabling a rapid fabrication with a wide flexibility in designs, similar to rapid-prototyping processes.[44,45] Our setup allows using printing head capillaries with an inner diameter as small as 100 µm, whereas keeping mechanical stability of the capillary and effects of electro-capillarity in a controlled range. With this, oxide structures with 60 µm line width are achieved. This is, however, not a fundamental limit, smaller capillary diameters seem feasible with advanced fabrication protocols. Future work is directed toward increasing the resolution of our direct writing technique to the 10 µm range. The resistance of the printed meander-resistor declines by widening of the conductive path, and vice versa. We fabricate two geometries with a factor of 2 in resistance change, whereas still maintaining a perfectly linear current–voltage characteristic (Fig. 1c). Inspired by the results, we decided to expand the printing process to more complex structures, such as capacitors, field-effect transistors, and bridge diode rectifiers (Fig. 2).

Solid-state thin-film capacitors are omnipresent in electric circuits; they are essential components in filter elements, as coupling capacitors in amplifiers and as energy buffers. Capacitor fabrication with the anodic printing head on an aluminum metalized plastic substrate starts with a two-step printing process. Initially aluminum stripes are patterned, serving as the bottom electrode for the capacitors. Here, the printing head moves at a high speed while applying a sufficiently high anodisation voltage to ensure complete conversion of aluminum into a dense, amorphous, highly insulating oxide, with an faradaic efficiency close to 100%, even on rough plastic substrates.[24,29] In the second step, the dielectric oxide is printed atop the bottom electrodes. Here, we use a lower speed to allow sufficient time for defect-free oxide formation, resulting in a high quality, barrier layer oxide-dielectric with reduced dielectric relaxation.[44] Evaporated gold electrodes complete the device (Fig. 2a).

A second process, including an etching step, was also investigated (Fig. S2). Regardless of the substrate material, the dielectric layers of thin-film capacitors must be dense and pinhole-free with low-leakage current. Tunnel current and impedance measurements reveal that the leakage current density of our capacitors remains below 1 µA cm^{-2} at 4 V bias (Fig. 2b), which is attributed partly to the large 8 eV band-gap of Al_2O_3 and the defect-free oxide fabrication via the anodic printing process. The low leakage is achieved even at a high applied electric field of 360 MV m^{-1} across the dielectric (about half the breakdown field of ~ 700 MV m^{-1} for amorphous Al_2O_3).[23,31] Here, the reduction of defects in the oxide through a sufficiently long polarization of the growing oxide decreases sites that enable resonance tunneling and thus leads to a low-leakage current density. The dielectric response of our capacitors stays nearly constant over several orders of magnitude of frequency and the loss tangent does not exceed 10^{-1} (Fig. 2c). The pinhole-free formation of the dielectric with the SDCM allows reliable fabrication of 11 nm thin oxide layers, ultimately resulting in a capacitance per area of 740 nF cm^{-2}. This corresponds to a relative permittivity of 9.2 for the fabricated Al_2O_3, in agreement with previously reported values.[31,46–48] Capacitors fabricated with an additional etching process show similar results, with a capacitance per area of 700 nF cm^{-2} and a leakage current density of 1 µA cm^{-2} at 4 V bias (Fig. S2b and c). Devices fabricated on polymer substrate are essentially identical to reference capacitors on borosilicate glass substrates (Fig. S3a and b).

Although resistors and capacitors are integral passive building blocks, active circuit components are required for state-of-the-art flexible electronic foils. Transistors are, for example, key elements of amplifiers and logic circuits. Commonly, thin-film transistors employ a bottom gate electrode, covered with a dielectric. A semiconductor with source and drain contacts on top of the dielectric serves as the active switching part of the device. Here, the gate electrode and high-k gate dielectric layer is fabricated on ultrathin 1.4 µm polyethylene terephthalate (PET) foils using the same process flow as for our thin-film capacitors. Then, the organic semiconductor and gold source and drain electrodes are evaporated via two subsequent physical vapor deposition processes, completing the device (Fig. 2d and S2). The gate oxide is plasma treated and functionalized with a *n*-tetradecyl phosphonic acid self-assembled monolayer (SAM)[46] to achieve better interfacing with the organic semiconductor dinaphto-thieno-thiophene (DNTT). The well-matched fabrication steps manifest in optimized electrical behavior, visible in the transfer (Fig. 2e) and output characteristics (Fig. 2f). Our transistors feature a high on–off ratio of 1×10^7, critical for applications as electronic switch. In addition, owing to the high-quality dielectric, the gate leakage current stays below 10 pA, whereas the Al_2O_3-SAM-hybrid capacitance retains a value of 450 nF cm^{-2}. Fitting the saturation regime yields a low threshold voltage of − 0.56 V and a carrier mobility of 2.7 cm^2 V^{-1} s^{-1}.[49] This enables use of the device for low-voltage applications, like mobile and wearable appliances. The optimized performance is attributed to the very good properties of the insulating hybrid-dielectric, which further manifests itself in a small subthreshold swing of 111 mV dec^{-1}. Similar results are also achieved for transistors fabricated from etched gate dielectric structures (Fig. S2d and e). In this case the hybrid capacitance is 480 nF cm^{-2} and exhibits a slightly larger threshold voltage of − 0.72 V. The saturation mobility of 2.3 cm^2 V^{-1} s^{-1} remains essentially the same. The on–off ratio as well as the subthreshold swing

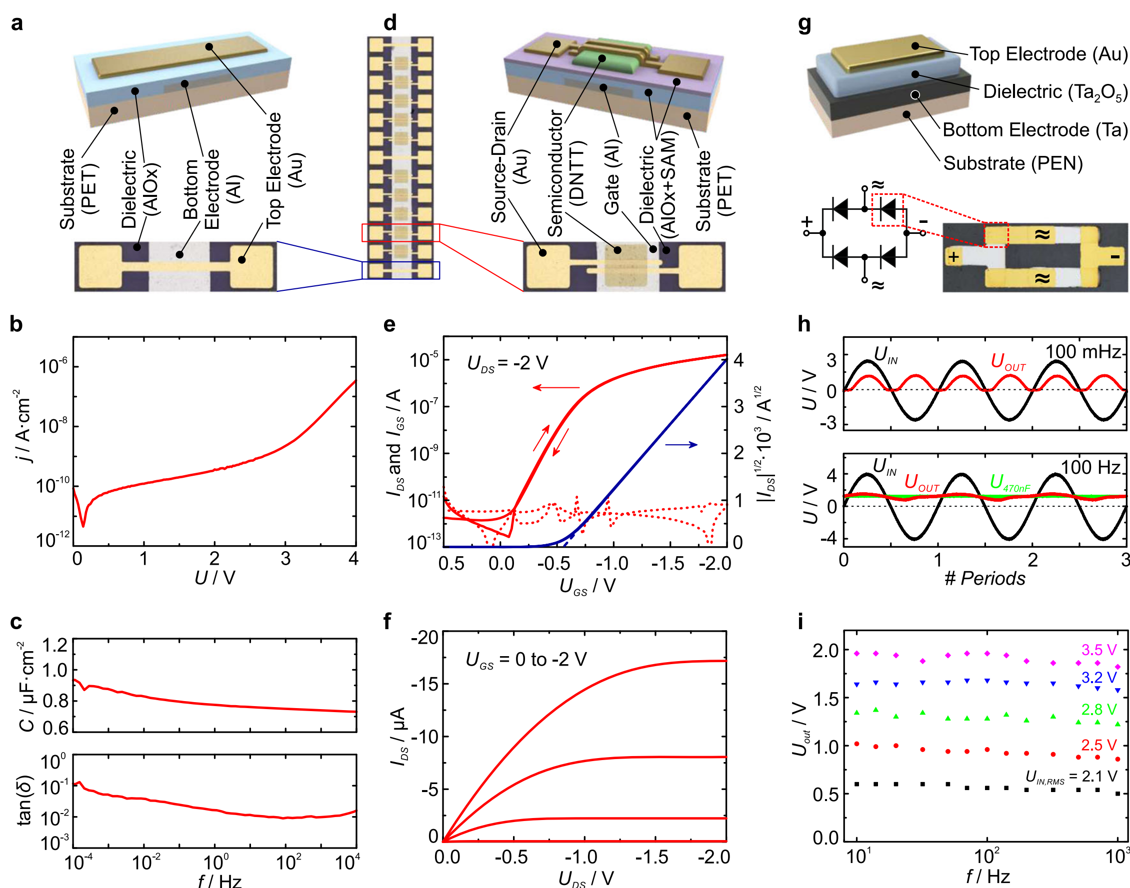

Fig. 2 Thin-film capacitors, organic transistors, and diodes with printed oxide dielectrics and semiconductors. **a** Schematic and optical microscope image of capacitors fabricated by utilization of the anodic printing head. Gold contact pads are 500 µm × 500 µm. **b** Low-leakage current per area is achieved for capacitors with a dielectric thickness of 11 nm even at high electric fields of 360 $\mathrm{MVm^{-1}}$. **c** High capacitance per area of 740 $\mathrm{nFcm^{-2}}$ and low dielectric loss for aluminum oxide capacitors. The dielectric constant of the written aluminum oxide is $\varepsilon_r = 9.2$. **d** Schematic and optical microscope image of organic transistors with gate electrodes and dielectric layers structured by direct writing. **e** Transfer characteristic of a p-type low-voltage organic transistor on 1.4 µm PET foils. We reach on–off ratios of 1×10^7 (red solid trace), threshold voltages of −0.72 V and mobilities of 2.3 $\mathrm{cm^2\,V^{-1}\,s^{-1}}$ (extracted from the saturation regime, blue solid trace). The leakage currents remain below 10 pA (red dotted line). **f** Output characteristics of the same transistor. **g** Schematic of a tantalum oxide diode with circuit diagram and photograph of a full bridge rectifier. Gold contact pads are 500 µm × 500 µm. **h** Output transients (red solid traces) of the rectifiers measured at 100 mHz and 100 Hz are compared with the sinusoidal input signal (black solid traces). The AC ripple voltage is very small for input frequencies of 100 Hz (see also Fig. S6) owing to parasitic parallel capacitances of the diodes and is fully suppressed when using a 470 µF external smoothing capacitor (solid green transient). **i** Smoothed output signal as measured at various root-mean-square input voltages and frequencies from 10 Hz to 1 kHz

is smaller at values of 2.4×10^6 and 87 $\mathrm{mV\,dec^{-1}}$, respectively. We extract carrier mobilities both in the linear and saturation regime (Fig. S4a and b) and find them to be in good agreement. Our devices have an average mobility of (2.33 ± 0.15) $\mathrm{cm^2\,V^{-1}\,s^{-1}}$, which is well within the range of previously reported values for this material.[21,50] With successfully fabricated transistors for low power and large area-sensing applications we show the versatility of the anodic printing process for fabrication and structuring of 2D devices. The process is not limited to aluminum and can be readily extended to other valve metals such as tantalum and titanium.

Anodic tantalum oxide diodes and rectifiers

The dielectric constant and band-gap of insulating materials are coupled. Ta_2O_5, for example, has a relative permittivity of 20–26 and a band-gap of 3.9 eV, causing an increase in the leakage and additionally introducing the possibility of creating strongly non-symmetric "leakage currents".[51,52] This asymmetry can be exploited for the fabrication of diodes through direct writing. The energy diagram of Ta_2O_5 and Fermi level alignment suggests placing the Ta_2O_5 between a gold and a tantalum electrode, forming a blocking and an ohmic contact. In addition, Ta_2O_5 layers thinner than 10 nm are n-type semiconductors.[53]

Our diodes are a Ta (100 nm)/Ta_2O_5/Au (50 nm) metal-insulator-metal (MIM) stack (Fig. 2g). We investigate oxide thicknesses ranging from 7 nm up to 20 nm as the semiconducting layer. The current–voltage characteristics of diodes with these different oxide thicknesses exhibit a clear non-symmetrical behavior (Fig. S5a). We use Fowler–Nordheim plots for the observed tunneling currents across the thin layers to gain deeper insight into the origin of the non-symmetric behavior and the prevailing conduction mechanism. The linear dependency at high voltages observed for our Ta_2O_5 diodes indicates that Fowler–Nordheim tunneling is dominating for those diodes with an oxide thickness larger than 11 nm (Fig. S5b). At thickness values below 10 nm deviations from a linear dependency occur and are attributed to the more n-semiconducting like behavior of the oxide. At 11 nm thickness the shape of the current–voltage characteristics suggests a transition behavior between these conduction mechanisms, ultimately yielding the best diode characteristic with an on–off or rectification ratio of roughly 3×10^4 (Fig. S5a). We find that the on–off ratio of reference diodes fabricated on borosilicate glass substrates is

significantly lower, with a larger current density at negative potentials and reduced rectification (Fig. S5c and d). This is attributed to the different surface energies of the substrate materials, directly affecting the metallic film adhesion during deposition. This leads to different levels of mechanical stress build-up during oxide growth. Moreover, a rigid substrate may enhance the stress levels up to the point where interfacial mechanical fractures form, which act as charge trapping defects creating higher conductivity paths for leaking electrons. Similar paths may also be obtained through the process of field-induced anodic oxide crystallization, which results in compressive stress build-up within the oxide.[54] Plastic substrates appear to be ideally suited for fabrication of Ta_2O_5 diodes with high rectification, likely owing to their ability of accommodating stress by mechanical deformation.

Direct writing of anodic oxide diodes is readily extended towards more complex flexible circuits such as full bridge rectifiers, required in inductively powered wireless energy transmission for mobile appliances.[34] Our rectifier uses 11 nm thin Ta_2O_5 layers, connected via gold and tantalum electrodes to create the four diodes and interconnects required for a full bridge rectifier (Fig. 2g). We characterize the rectifier for sinusoidal input between 100 mHz and 100 Hz (Fig. 2h). The low-frequency response exhibits the characteristic rectifier output signal, reaching a peak value of 1.1 V in each half period. However, at input frequencies higher than 100 Hz we no longer observe classical rectifier output. Even without an external smoothing capacitor, the virgin output (Fig. 2h) closely resembles the expected output when using an additional 470 nF smoothing capacitor (Fig. 2h). In both cases, no significant ripple voltage occurs. This unusual behavior stems from the dielectric properties of Ta_2O_5. Owing to the high relative permittivity ε_r of anodic Ta_2O_5, each diode has a parasitic parallel capacitance of 6 nF (Fig. S6a), whereas still exhibiting an on–off ratio larger than 10^4 (Fig. S6c). Modeling the output transient of the non-ideal rectifier at 100 mHz and 100 Hz shows, that the parasitic capacitance exerts a smoothing effect on the output signal at higher frequencies. The effect is equal to that of an external smoothing capacitor (Fig. S6b). This parasitic capacitance is beneficial for smoothing the output ripple voltage, however it reduces the power efficiency of the rectifier. We in addition test the dependence on input voltage by applying different root-mean-square input voltages, ranging from 2.1 V up to 3.5 V. We observe an almost frequency independent output DC voltage between 10 Hz up to 1 kHz (Fig. 2i). Taking the values of the output and input signals into account, we find a forward voltage of 1.5 V for the Ta_2O_5-diodes. Reducing the forward voltage could be achieved by tuning the work functions of both

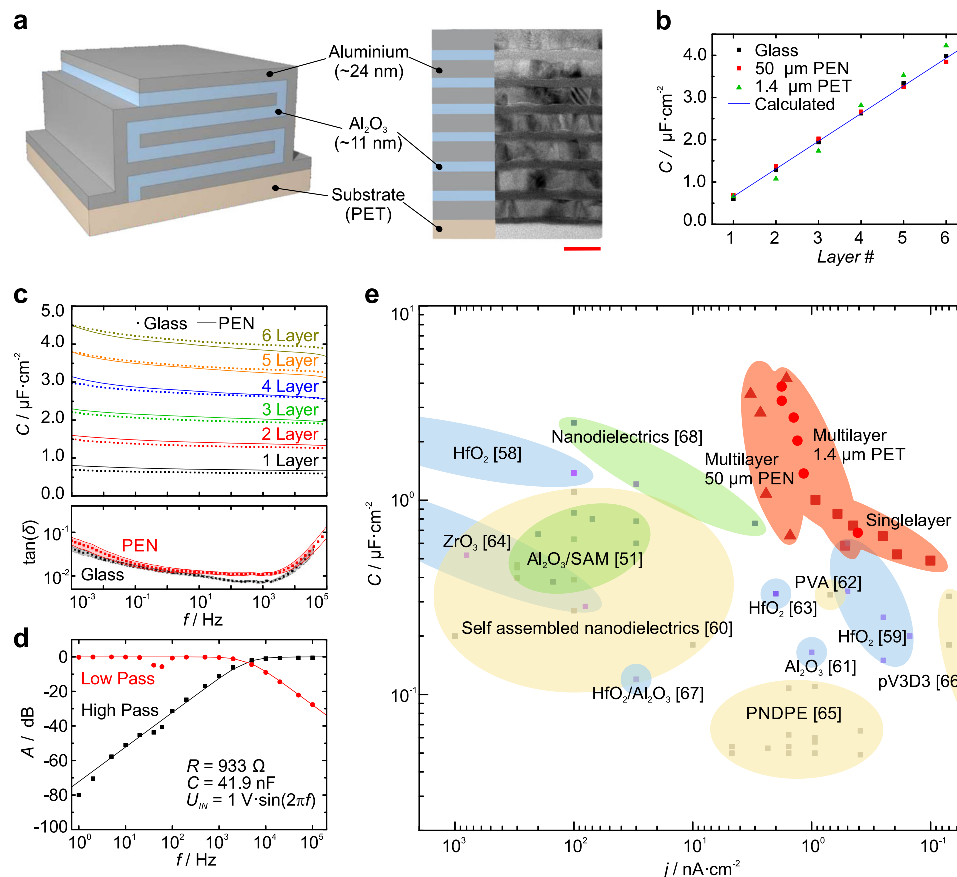

Fig. 3 Multilayer capacitors fabricated by local anodisation. **a** Schematic of multilayer structure and corresponding STEM image, highlighting the high precision and reproducibility of the anodisation process down to nm-size. Scale bar: 50 nm **b** Each layer increases the capacitance linearly until a value of 4.2 µF cm^{-2} is achieved for six layers. No significant influence of the substrate (50 µm PEN, 1.4 µm PET, and borosilicate glass) is observed. The increase matches well with theoretical predictions (solid blue line) were an oxide thickness of 12 nm and a dielectric constant of $\varepsilon_r = 9$ is assumed (see SI for details). This leads to an increase of 650 nF cm^{-2} per layer. **c** Impedance data show a linear increase in capacitance and the same shape for all number of layers. The dielectric loss tangent is independent on the number of layers. Dotted lines are for samples prepared on glass, solid lines represent flexible devices on PEN. **d** High and low pass filters from anodically printed resistors and multilayer capacitor structures. Here, a resistor of 933 Ω and a capacitance of 41.9 nF is used. Measurements (black and red points) agree excellently with simulation (solid lines, see SI for details). **e** Comparison of capacitance per area and leakage current density with literature.[51,58-68] Our multilayer capacitors (red symbols) reach record-high capacitance of 4.2 µF cm^{-2} at sub-10 nA cm^{-2} leakage current levels

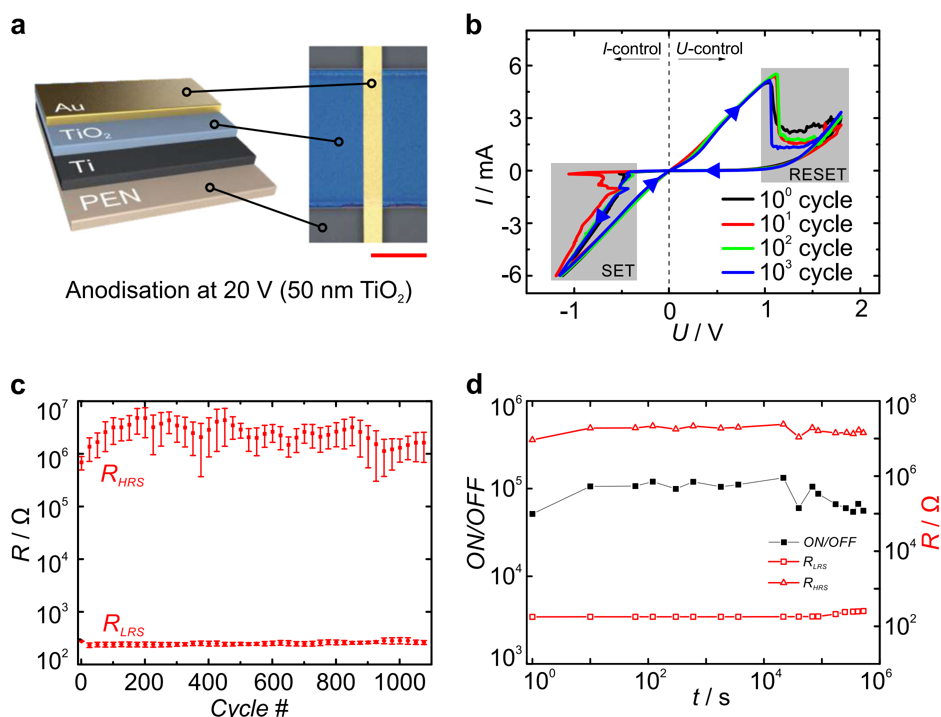

Fig. 4 Titanium oxide memristors. **a** Schematic illustration of the memristor devices with 50 nm titanium oxide layer together with an optical microscope picture. Scale bar: 300 µm. **b** Current–voltage characteristic of a typical memristor for one (black trace), 10 (red trace), 100 (green trace), and 1000 (blue trace) switching cycles. No significant changes in switching hysteresis are observed. The SET and RESET half-cycles are performed under current control and voltage control, respectively, to reduce power dissipation and improve lifetime. **c** HRS (high resistive state, R_{OFF}) and LRS (low resistive state, R_{ON}) for over 1100 switching cycles, showing no visible degradation. **d** Long time retention measurements for 6 days (533,060 s). Readout of both LRS and HRS is reliable without visible degradation, ultimately implying that stable memory performance is achievable

oxide and gold electrodes by doping of the oxide, or by fabricating PN-junctions. The semiconducting properties of oxides can be changed with the anodisation process itself, as previously shown for Indium-Tin-oxide.[55] Having demonstrated passive and active building blocks of flexible electronic circuits by direct writing, we now show that it is even possible to extend the patterning into the third dimension to further increase integration density.

3D-anodic oxide structures

Miniaturization is vital for integrating soft electronic circuits more intimately into our daily lives. Shrinking the size, for example, of organic amplifiers, critically depends on reduction of capacitor space.[56] Commonly, there are two pathways to address this need. One is by material selection, namely boosting capacitance per area, by choosing a dielectric material with a high ε_r. The second possibility is to decrease the thickness of the dielectric. Often both approaches are taken in combination to increase the capacitance as much as possible. However, high-ε_r materials and smaller insulating layer thickness usually come at the cost of increased leakage currents.[31] To overcome these issues, we here introduce a different approach. We employ our direct writing method to expand the layered structure of capacitors into the third dimension, generating a 3D stack that increases the capacitance per unit area. We choose anodic Al_2O_3 as a dielectric material since it offers a comparably large dielectric constant of ~9, paired with a large ~8 eV band-gap. It enables fabrication of capacitors with a capacitance per area of 650 nF cm^{-2} and a low-leakage current density of only 1.5 nA cm^{-2} at an electric field of 100 MV m^{-1} across the dielectric. Such single capacitors are processed on top of each other, forming an interconnected three-dimensional multilayer capacitor stack (Fig. 3a). Every individual dielectric layer has a thickness of 11 nm and shows a high degree of reproducibility and precision achieved through the anodisation process. We confirm the successful layer formation by Scanning Transmission Electron Microscopy (STEM, Fig. 3a). Each fabricated layer adds further 650 nF cm^{-2} to the total capacitance per area, yielding a linear increase of the capacitance per area with the number of layers (Fig. 3b). We fabricate up to six layers to demonstrate scalability of our process, achieving a record-high 4.2 µF cm^{-2}. Yet, an ultimate limit in the amount of stacked layers has not been encountered and is subject for further work. The leakage current density follows the same linear behavior and thus further emphasizes on the high degree of purity and reproducibility of the anodic oxide layers (Fig. S7a), even at electric fields as high as 100 MV m^{-1}. The logarithmically placed frequency spectrum obtained by AC impedance spectroscopy for each layer (Fig. 3c) evidences applicability of our multilayer capacitors over a wide range of frequencies, from 1 mHz up to 100 kHz. The loss tangent stays at low values and shows no dependency on frequency, highlighting the capacitive behavior. We observe no significant differences for capacitors fabricated on 50 µm PEN substrates and their borosilicate glass substrates references. Even six layer capacitors fabricated on ultrathin 1.4 µm PET substrates show the same behavior as their glass and thicker plastic substrate counterparts (Fig. S7b). We thus demonstrate that the proposed multilayer capacitor approach works independent of substrate surface morphology. Benefiting from the ultrathin form factor, multilayer capacitors on imperceptible foils are largely insensitive to bending deformation. We perform repeated folding tests (Fig. S8) and find no influence on the capacitance due to the negligible induced strains (see also discussion on the mechanical performance of imperceptible thin-film electronics in the methods section).

AC-signal manipulation in measurements and electronic circuits critically depends on analogue filter technology such as high and

low pass filters. Connecting our printed resistors (Fig. 1c) to six layer capacitors with a total capacitance of ~42 nF results in low and high pass filters, with a cutoff frequency of 4080 Hz and excellent transmission functions over a wide range of frequencies (Fig. 3d). The measured transfer functions of our high and low pass filters match closely with the model of an ideal high and low pass filter. We attribute this close-to-ideal behavior over a wide frequency range to the excellent frequency behavior of the multilayer capacitor stacks.

Our capacitor stacks perform favorably when compared with other available capacitor technology platforms. Here, the two most important parameters for technical applications are the capacitance per area and the leakage current density. Applying a reasonable bias stress of 100 MV m^{-1} across the dielectric of the capacitor is chosen as the standard for leakage current measurement. We compare the leakage current density as a function of capacitance per area (Fig. 3e) for recent reports of dielectric materials and capacitors.[51,58–68] Here, high-performing capacitors require both a high capacitance per area and a low-leakage current density. Although some materials (like pV3D) show superior leakage behavior compared to anodic Al_2O_3, this is typically only achievable by sacrificing the high capacitance per area. Our 3D stacking approach overcomes these limitations and reaches record-high capacitance per area of 4 μF cm^{-2} in thin-film solid-state capacitors, whereas the leakage currents remain below 4 nA cm^{-2}. This highlights the high degree of miniaturization achievable through anodic printing, making our multilayer capacitors a sensible approach for fabrication of highly integrated electrical circuits.

Anodic titanium oxide memristors

Titanium and its oxide, TiO_2, finds applications as body implants, in photovoltaics, catalysis, and as dielectric.[25,27,41,68] More recently, advancements in data storage technologies drive the development of resistive memory elements such as memristors, where data storage is achieved in the form of two different resistive states. First reports describing unprecedented resistive switching processes[69] in TiO2 appeared in the 1960s, later acknowledged as memristive switching behavior.[70,71] Nowadays, TiO_2 is the most widely studied and prominent memristive material,[35,36,72] where first comprehensive views on the switching mechanism were recently presented.[73] The bulk of research on memristive materials is carried out on ALD or sputter deposited oxides, with lesser focus on anodic oxides.[74,75] We here present a fabrication and electrical measurement protocol for memristors based on anodic TiO_2 on flexible substrates with improved switching performance and prolonged device lifetime. We implement a Ti/TiO_2/Au MIM on plastic substrates (Fig. 4a, schematic and an optical microscope picture), where electroforming turns the MIM structure in a memristor (Fig. S9a). We chose to carry out the electroforming process with a current slope, instead of commonly employed voltage slopes,[76] as this process allows for better control and reliability. During the electroforming process, the resistance initially starts at a high level and continuously decreases with increasing current. A sudden drop in voltage marks the initial transition from a high resistive state (HRS) into a low resistive state (LRS) of 150–300 Ω, after which the memristor is formed. Typical switching cycles of electroformed devices show bipolar switching characteristics (Fig. S9b). Starting from an LRS, a positive increase of the voltage leads to a linear increase in current until a switching threshold current I_{RESET}. There, the current rapidly drops to a lower level, passing through the RESET-transition into the HRS. We use current sweeps when applying negative voltages, where originating from the HRS the voltage rapidly increases until a SET-transition occurs that switches the memristor back into the LRS. After the SET-transition we increase the current further until a final desired set-current I_{SET}, where the sweep direction is reversed. Employing both current and voltage sweeps is beneficial when considering power dissipation. If the current is controlled for positive voltages, the rapid increase in resistance at the reset-transition leads to an equally rapid increase in power dissipation in the memristor according to $I^2 R$. Voltage controlled switching on the contrary is self-protecting, as the power dissipation declines with U^2/R during the transition. The same reasoning preferences a current sweep for negative potentials, where the SET-transition occurs. We record switching cycles for three different set-currents (−4 mA, −6 mA, and −8 mA, Fig. S9b). A larger I_{RESET} threshold must be reached for a higher I_{SET} to trigger the RESET-transition. This behavior becomes more apparent when looking only at the positive voltage regime of the data presented in S9b (Fig. S9c). We in addition observe a relation between the slope of the linear regime, which represents the resistance R_{LRS} of the LRS, and the I_{SET}. Here, a higher I_{SET} leads to a decrease in R_{LRS}, and we find a linear relationship with an R-square value of 0.98 for I_{SET} and the corresponding I_{RESET} (Fig. S9d). These findings agree well with previous reports.[77]

Switching cycle performance and memory retention is crucial for applications in data storage. We evaluate the long time performance of the memristor elements with a pulse measurement and in addition record current–voltage characteristics following one, 10, 100, and 1000 switching cycles (Fig. 4b). The switching is carried out with a current pulse and a voltage pulse for the SET and RESET-transition, respectively. No significant changes in switching current I_{RESET} and resistance of the LRS and HRS (Fig. 4b and c) are observed for our memristors, demonstrating a good cyclic stability. An on–off ratio of ~10^4 separates the resistances of the two states, enabling clear distinction. We find a switching accuracy of >99.5%, with only four out of 1100 performed cycles not switching. Limitations of our measurement setup necessitate, comparably long switching times that result in an energy consumption of $W_{SET} = (0.27 \pm 0.02)$ mWh and $W_{RESET} = (8.28 \pm 1.13)$ mWh.[35] We anticipate drastically lower values through reducing the size of the memristor elements. Long time retention tests of our memristive devices are carried out in the LRS and HRS state using the before mentioned pulse method (Fig. 4d). Consecutive readout with a voltage pulse of 50 mV for 30 ms is performed for 6 days (533,060 s). Our memristors maintain a high on–off ratio between 10^4 and 10^5 during the entire time, whereas the respective resistances of the LRS and HRS show little variation. A simple linear extrapolation of this data suggests excellent retention times for either the programmed LRS or HRS states. Here, a decay of the on–off ratio to 10 or less would require on the order of 10^{11} years, by far exceeding the operational lifespan of the devices.

Switching between current- and voltage-control allows long and reliable operation of our memristors. By minimizing the power dissipation in the device, less degradation occurs. This readily allows applications in digital and analogous data storage with good retention times in flexible and soft electronics. Here, electrically adjusting the reset-point and resistance of the LRS is possible by applying appropriate values for the set-current, opening additional opportunities in synapse-like neuromorphic computing.[78]

DISCUSSION

We introduce direct writing of anodic oxides as versatile tool for plastic oxide electronics including circuit elements and devices at low cost under ambient conditions. The anodic printing process enables adaptable 2D structuring for the fabrication of resistors, capacitors, and transistors. Drawing inspiration from 3D printing, we expand the process into the third dimension for the fabrication of multilayer devices with unmatched capacitance densities in thin-film devices. The precise control over oxide thickness and purity readily allows the fabrication of diodes, rectifiers, and

memristors. The future of anodisation may thus rapidly expand from applications in passivation to the manufacturing of complex plastic oxide electronic devices for healthcare, biomedical systems, mobile appliances, and sensors.

MATERIALS AND METHODS

Fabrication and electrical characterization of devices

Ultrathin film substrates. Ultrathin 1.4 µm thick PET foil (Teonex Q51, obtained from Pütz GmbH + Co. Folien KG, Germany) was adhered to polydimethylsiloxane (PDMS)-coated 150 µm PET foils as supporting substrate to ease handling in laboratory-scale device fabrication. Adhesion of the ultrathin PET foil to the supporting substrate is due to Van-der-Waals forces, enabling all used process steps (vacuum metal deposition and anodisation) and non-destructive release through peeling of the finished devices.

Resistors. Resistors were fabricated by thermal evaporation of 30 nm aluminum on 1.4 µm PET substrates and subsequent anodisation with a scanning droplet cell microscope (SDCM) used as anodic printing head (Fig. S1) to form the resistor meander geometry (Fig. 1). The aluminum was evaporated without a shadow mask, covering the whole substrate, with a rate of 1 nm s^{-1} at a base pressure of 10^{-6} mbar. Thereafter, the anodic printing head with a tip diameter of 130 µm was employed to electrochemically pattern resistor meander structures of various geometrical dimensions.[45,79] To ensure complete anodisation of the 30 nm-thick aluminum layer, an anodisation voltage of 20 V and a writing speed of 34 mm min^{-1} were used, whereas a distance of ~ 50 µm between printing head and aluminum surface was maintained.[44] A three-axis stage, controlled by a custom made LabView program, allowed precise speed and position control during the patterning process. All anodisation with the anodic printing head was carried out under ambient conditions with a pH 6.0 citric acid buffer electrolyte (0.265 g citric acid (MERCK, per analysis), 2.57 g tri-sodium citrate dehydrate (MERCK, per analysis) in 100 ml ultrapure 18 MΩ cm water). Electrical characterization was done with an Agilent B1500A Semiconductor Device Parameter Analyzer under ambient laboratory conditions.

Capacitors. We used an Al (30 nm)/Al_2O_3 (11 nm)/Au (50 nm) MIM structure for the capacitors. Processing started with thermal evaporation (rate of 1 nm s^{-1} at a base pressure of 10^{-6} mbar) of a 30 nm-thick aluminum bottom layer, covering the whole 1.4 µm PET film substrates (Fig. S10a). Patterning of the bottom electrode was done by anodisation with the anodic printing head, analogous to the resistor meanders. A 600 µm diameter capillary at a writing speed of 34 mm min^{-1} was utilized for structuring a 500 µm wide capacitor bottom electrode. Application of 20 V anodisation voltage with a Keithley 2611 A SourceMeter ensured complete anodisation of the 30 nm-thick aluminum layer. After patterning of the electrode, the dielectric oxide layer was written at 5 V vs. Standard hydrogen electrode (SHE) (11 nm) with a slow writing speed of 0.34 mm min^{-1}, leading to an anodisation time of at least 2 min for every spot on the electrode (Fig. S10b, c). During the process, a mercury/mercury acetate micro-reference electrode in combination with an EG&G Instruments Potentiostat/Galvanostat 283 ensured precise potential control in the electrolyte, leading to a uniform and homogeneous dielectric oxide layer on top of the aluminum bottom electrode.[80] The high-field model governs the growth of anodic oxides; therefore precise potential control readily allows determining the oxide layer thickness down to nm-accuracy.[81–83] The relationship between oxide thickness d_{ox} and applied potential U is given by $d_{ox} = k\,(U - U_{ox})$, where the growth factor k equals 1.6 nm V^{-1} and the thermodynamic equilibrium potential U_{ox}, accounting for the potential of oxide-free metal, takes the value of −1.6 V for aluminum.[24] Thus, an oxide thickness of 11 nm is achieved for an applied potential of 5 V vs. SHE. In a last step a gold top electrode is thermally evaporated (rate of 0.1 nm s^{-1} at a base pressure of 10^{-6} mbar) through a shadow mask, forming capacitors with an area of 0.77 mm^2. We in addition developed an alternative method for patterning the bottom electrode (Fig. S2) with increased fabrication speed. Here, only two fully anodized lines are printed to define the bottom electrode geometry, followed by the writing of the dielectric oxide layer. The remaining excess aluminum (not anodized) is then removed through an 1 min selective etching in an acid solution (19:1:1:2, ortho-phosphoric acid: acetic acid: nitric acid: ultrapure 18 MΩ cm water). All other process steps are equivalent to the previously described capacitor fabrication. Frequency-dependent impedance characterization of the devices was done with a Novocontrol Alpha-A Performance Frequency Analyzer from 0.1 mHz to 10 kHz, with a perturbation amplitude of 20 mV. Leakage currents of the capacitors were recorded with a Keithly 617 electrometer and an Agilent 33250A Waveform Generator, controlled by a custom made LabView program. For reference purposes the same fabrication and characterization was also carried out, using glass substrates instead of the 1.4 µm PET foil.

Transistors. Fabrication of the organic thin-film transistors starts with the same processing steps as capacitor fabrication, only without the last step of top electrode deposition. Thus, an Al (30 nm)/Al_2O_3 (11 nm) gate electrode−dielectric structure was fabricated, using only the anodic printing head. Subsequently, the oxide was functionalized with an *n*-tetradecyl phosphonic acid SAM for better interfacing with the organic semiconductor DNTT.[46] Functionalization consists of a short activation of the surface in oxygen plasma (1 min at 100 W), followed by dipping into a 5 mM solution of SAM molecules in propan-2-ol. This readily forms a 2 nm-thick SAM on top of the anodically grown Al_2O_3, resulting in a total hybrid-dielectric capacitance of about 450 nF cm^{-2} (fully printed gates) and 480 nF cm^{-2} (etched gates). On the SAM, a 20 nm-thick DNTT semiconducting layer was deposited trough a shadow mask at a rate of 0.01 nm s^{-1} and a base pressure of 10^{-6} mbar. The device was finalized by thermal evaporation of gold source and drain contacts through a shadow mask, at a rate of 0.1 nm s^{-1} and a base pressure of 10^{-6} mbar, forming a channel of width 500 µm and length 40 µm. Electrical characterization of OTFTs was performed with an Agilent B1500A Semiconductor Device Parameter Analyzer under ambient laboratory conditions. The carrier mobilities in the linear regime (μ_{lin}) were extracted from drain source current (I_{DS}) vs. gate source voltage (U_{GS}) curves according to:

$$\mu_{lin} = \frac{L}{WC_i U_{DS}} \frac{\partial I_{DS}}{\partial U_{GS}} \quad (1)$$

And in the saturation regime (μ_{sat}) from the plots of the square root of I_{DS} vs. U_{GS}:

$$\mu_{sat} = \frac{2L}{WC_i} \left(\frac{\partial \sqrt{|I_{DS}|}}{\partial U_{GS}} \right)^2 \quad (2)$$

Here, L and W are the length and width of the accumulation channel, C_i is the gate channel capacitance per unit area, and U_{DS} is the drain source voltage.[84]

Multilayer capacitors. The first layer was formed by thermal evaporation (rate of 0.5 nm s^{-1} at a base pressure of 10^{-6} mbar) of a 24 nm-thick aluminum stripe of 0.5 × 12 mm dimensions. The center of the stripe was locally oxidized at a constant potential with a 100 µm diameter anodic printing head at a voltage of 6 V vs. SHE (11 nm) for 5 min. Voltage was applied with EG&G Instruments Potentiostat/Galvanostat 283 and a mercury/mercury acetate micro-reference electrode in the anodic printing head ensured precise potential control. Perpendicular to the previous stripe a 24 nm-thick top aluminum electrode (0.5 × 12 mm) was deposited, forming an Al/Al_2O_3/Al cross-bar MIM structure with an area of 1 mm^2. Subsequently, it was locally anodized at the center in the same fashion as the first layer. Perpendicular to the second aluminum stripe a third one was evaporated, aligning with the bottom aluminum layer. Lateral connection of the first and third aluminum stripe was readily formed, as only the middle spot of each layer was anodized and natural oxide is not sufficient to prevent current flow. Next, the procedure of perpendicular stripe evaporation with consecutive local anodisation was repeated until the desired number of layers was achieved. Frequency-dependent impedance characterization of the devices was done with a Novocontrol Alpha-A Performance Frequency Analyser from 1 mHz to 100 kHz, with a perturbation amplitude of 20 mV. Leakage current measurements of the multilayer stacks were recorded analogous to the single layer systems. For reference purposes the same fabrication and characterization was also carried out, using 50 µm PEN film (Teonex Q51) and glass substrates instead of the 1.4 µm PET foil.

Diodes. Devices consist of a Ta (100 nm)/Ta_2O_5 (7–20 nm)/Au (50 nm) MIM structure. The 0.5 × 12 mm bottom electrode was formed by sputter deposition (10^{-7} Pa base pressure, deposition rate of 2.2 nm min^{-1} in 5 × 10^{-1} Pa Ar) of 100 nm metallic tantalum, through a shadow mask (Fig. S10d). A 125 µm PEN foil (Teonex Q65HA, supported by Teijin DuPont Europe) was used as substrate. Anodisation at different voltages was

carried out in a beaker, were Platinum served as counter electrode in the same electrolyte as described above. Tantalum anodisation started with an increase of the potential at 100 mV s^{-1} until the desired end potential was reached, which was then held constant for 6 min (Fig. S10e, f). Anodic oxide growth of tantalum follows again the high-field model, with a linear dependence of oxide thickness and applied anodisation potential. The growth factor k equals 1.8 nm V^{-1} and the thermodynamic equilibrium potential U_{ox} is – 0.3 V for tantalum.[24,81–83] Anodisation was carried out at the following end potentials: 3 V (7 nm), 4 V (9 nm), 5 V (11 nm), 6 V (13 nm), 7 V (14 nm), 8 V (16 nm), 9 V (18 nm), and 10 V (20 nm). A 50 nm-thick gold top electrode completed the devices, forming a Ta/Ta_2O_5/Au structure with an area of 0.37 mm^2. Current–voltage characteristics of diodes where recorded at a scan rate of 200 mV s^{-1}, with a Keithley 2611 A SourceMeter, controlled by a custom made LabView program. In all measurements, the gold top electrode was connected to the positive terminal and the tantalum electrode to the negative terminal of the SourceMeter. For reference purposes, the same fabrication and characterization was also carried out using glass substrates.

Rectifiers. Rectifiers were fabricated in a similar manner as diodes. In a first step 100 nm tantalum is sputter deposited through a shadow mask, designed to form four diodes in a bridge rectifier configuration, on 125 µm PEN foil substrate. Thereafter, local anodisation of the tantalum was performed with the anodic printing head, at the respective diode spots. The potential was increased at 100 mV s^{-1} until 5 V vs. SHE was reached, and held constant for further 6 min. A thermally evaporated 50 nm gold (rate of 0.5 nm s^{-1} at a base pressure of 10^{-6} mbar) layer formed the diode top electrode and circuit interconnects between the diodes. The rectifiers were powered with an Agilent 33250A Waveform Generator in the frequency range from 1 mHz up to 1 kHz, with 3–5 V amplitudes. Time responses and rectified output of the circuit was analyzed with a Tektronix TDS3012 Digital Oscilloscope.

Memristors. Fabrication of memristors starts with e-beam deposition of 100 nm Ti (rate of 1 nm s^{-1} at a base pressure of 10^{-6} mbar), and subsequent anodisation (Fig. S10g–i). Titanium anodisation was carried out in a beaker with a platinum counter electrode and a pH 6.0 citric acid buffer as electrolyte. First, the anodisation potential was increased at 300 mV s^{-1} until the desired end potential of 20 V was reached and held constant for further 10 min. The growth factor k is 2.5 nm V^{-1} and the thermodynamic equilibrium potential U_{ox} is – 0.86 V for titanium.[24] This results in an oxide thickness of roughly 50 nm for an anodisation potential of 20 V. Through a shadow mask a 50 µm top gold layer was evaporated (rate of 0.1 nm s^{-1} at a base pressure of 10^{-6} mbar), forming a MIM structure with an area of 0.046 and 0.078 mm^2. Initially, the MIM structure behaves like a diode, but is turned into a memristor through an electroforming process.[36,76] Nauenheim et al.[85] previously showed high reliability of current controlled electroforming, at low sweeping rates. Here, a current sweeping rate of 5 µA s^{-1} between the gold (positive) and titanium (negative) electrode was used, supplied with a Keithley 2611 A SourceMeter. When increasing the current, a rapid decrease in resistance to a LRS (low resistive state) of 150–300 Ω happened at 0.5–0.8 mA. After the initial electroforming the memristors were switched between the LRS and HRS with a SourceMeter controlled by a custom build LabView program.

Structural investigations (SEM, AFM, STEM)

SEM pictures were recorded using a Zeiss Gemini 1540 XB with a SE2 detector at 3 kV acceleration voltage, with a magnification of 25,000 for general and 100,000 for detailed images. AFM topologies were recorded using a Nanosurf easyScan 2 in contact mode. Data analysis was performed with Gwyddion software. Cross-sections of the multilayer capacitors were prepared by focused ion beam milling (1540 CrossBeam Scanning Electron Microscope, ZEISS). A thin gold layer was sputtered onto the specimen prior to milling. TEM lamellas were prepared by standard FIB cutting, lift out and transfer to a TEM grid, followed by a final thinning to ~ 100 nm with an ion energy of 5 keV to minimize preparation artefacts. Samples were investigated with a JEOL JEM-2200FS transmission electron microscope with STEM mode operated at 200 kV.

Mechanical performance of imperceptible thin-film electronics

By fabricating our electronic devices on ultrathin (1.4 µm-thick) PET foils, the strain in the active part of the circuits is greatly reduced when bending. This consequently follows from calculations on the mechanics of foldable film-on-foil electronics.[86] For a rigid metal film (Young's modulus E_f, thickness t_f) laminated on a softer substrate (Young's modulus E_s, thickness t_s) the strain ε_{top} scales inversely with the bending radius R via

$$\varepsilon_{top} = \frac{t_f + t_s}{2R} \frac{(1 + 2\eta + \chi\eta^2)}{(1 + \eta)(1 + \chi\eta)} \quad (3)$$

With $\eta = t_f/t_s$ and $\chi = E_f/E_s$. The PET foil used in this work as substrate has a Young's modulus of $E_s = 2.5$ GPa and a thickness of $t_s = 1400$ nm. For our capacitor that consists of six alternating layers of aluminum ($E_{Al} = 69$ GPa, $t_{Al} = 24$ nm) and aluminum oxide ($E_{AlOx} = 130$ GPa, $t_{AlOx} = 11$ nm) the total capacitor active layer is $t_f = 234$ nm with an average modulus of 86 GPa (seven layers aluminum, six layers aluminum oxide). Using these parameters together with the model[86] and applying a bending radius as small as 10 µm, we estimated the strain of the capacitor to be maximum 2.5%. This estimate is below the fracture strain even for amorphous AlOx.

Applications in wearables will profit from coating our ultrathin oxide electronics with a thin layer of a soft elastomer as strain-buffering interface to human skin or robotic bodies. As calculated below, a 14 µm thick PDMS sheet would shift the active parts of the electronics into the neutral mechanical plane b, vastly decreasing the bending-induced strain on the metal/oxide layers[87]

$$b = \frac{\sum_{i=1}^{n} \bar{E}_i t_i \left(\sum_{j=1}^{i} t_j - \frac{t_i}{2} \right)}{\sum_{i=1}^{n} \bar{E}_i t_i} \quad (4)$$

$$\bar{E}_i = \frac{E_i}{1 - \nu_i^2} \quad (5)$$

where E_i, t_i, and v_i are the Young's modulus, thickness, and Poisson's ratio of the ith layer in the stack of layers forming the capacitor, respectively. b is the distance between the neutral mechanical plane and the bottom of the multilayer system. The PET foil ($E_1 = 2.5$ GPa, $v_1 = 0.43$) builds the first layer and is followed by the capacitor layers where the aluminum layers have a Young's modulus $E_{2,4,6,8,10,12,14} = 69$ GPa and a Poisson's ratio $v_{2,4,6,8,10,12,14} = 0.33$ and the AlOx layers a Young's modulus $E_{3,5,7,9,11,13} = 130$ GPa and a Poisson's ratio $v_{3,5,7,9,11,13} = 0.22$. PDMS as the strain buffer has $E_{15} = 1.84$ MPa and $v_{15} = 0.5$. Using these parameters, the mechanical neutral plane b is located within the capacitor layers at ~ 1.52 µm from the bottom of the stack. The capacitor layers that are located with distance d from the neutral plane, experience a strain of $\varepsilon = d/r$, when bend by the curvature radius r. Alternatively, a 1.4 µm PET layer can be used instead of PDMS to improve the strain tolerance of the electronics. The now matching Young's moduli of both substrate and encapsulation will lay the capacitor again in the neutral mechanical plane, and thus prevent damaging of the electronics and allow extreme flexibility.

DATA AVAILABILITY

All data and methods for device fabrication and evaluation are presented in the paper and Supplementary Materials. Data, materials, and further information are available from the authors upon request.

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AUTHOR CONTRIBUTIONS

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ADDITIONAL INFORMATION

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