nature communications

Article

https://doi.org/10.1038/s41467-023-40938-y

Non-volatile optoelectronic memory based on a photosensitive dielectric

Received: 7 April 2023

Accepted: 15 August 2023

Published online: 05 September 2023

Check for updates

Rui Zhu[1,2] ✉, Huili Liang[1,2], Shangfeng Liu[1,3], Ye Yuan[1], Xinqiang Wang[1,3], Francis Chi-Chung Ling[4], Andrej Kuznetsov[5], Guangyu Zhang[1,2] & Zengxia Mei[1,2] ✉

Recently, the optoelectronic memory is capturing growing attention due to its integrated function of sense and memory as well as multilevel storage ability. Although tens of states have been reported in literature, there are still three obvious deficiencies in most of the optoelectronic memories: large programming voltage (>20 V), high optical power density (>1 mW cm^{-2}), and poor compatibility originating from the over-reliance on channel materials. Here, we firstly propose an optoelectronic memory based on a new photosensitive dielectric (PSD) architecture. Data writing and erasing are realized by using an optical pulse to switch on the PSD. The unique design enables the memory to work with a programming voltage and optical power density as low as 4 V and 160 μW cm^{-2}, respectively. Meanwhile, this device may be extended to different kinds of transistors for specific applications. Our discovery offers a brand-new direction for non-volatile optoelectronic memories with low energy consumption.

The emergence of smart home, autonomous driving, and bionic robots etc. marks the arrival of big data era, which puts forward increasingly higher requirements for nonvolatile memory, one of the carriers of information storage[1]. Flash memory has always been in an unshakable position in nonvolatile memory field[2–4], although some new structures or principles, such as magnetic random-access memory[5], ferroelectric random-access memory[6], phase-change memory[7] and resistive random-access memory[8], were constantly proposed. However, faced with the already-arrived big data era, the drawbacks of flash memory have gradually emerged. Firstly, general flash memory cell has a two-state storage capacity, and the integration density is being restricted by the scaling down limit[9], which creates a huge gap between the considerable data generated every day and the existing storage capability. Secondly, the programming voltage of flash memory has been maintained above 10 V, leading to a huge energy consumption[4]. The reason lies in its core structure and programming process, as shown in Fig. 1a, b. The difference between the flash memory and the common metal–oxide–semiconductor field-effect transistor (MOSFET) is the insertion of a 9–10 nm tunneling dielectric (TD) layer and a floating gate (FG) surrounded by the dielectric layers. Writing or erasing data depends on the electrons' transport through the TD layer back and forth via Fowler–Northeim tunneling[10] process and the resulting shift of the threshold voltage, which inevitably requires a large gate voltage (V_{GS}) pulse (Fig. 1b).

The property of electrical read-out orthogonal to the photo-programming operation promises high differentiation among different data levels and imparts the ability of multilevel storage to optoelectronic memory[9]. For instance, different electrical signals, namely multi-states, can be obtained by adjusting the wavelength, the pulse width, the pulse number, the optical power density and even the polarization of the optical pulse.

Currently, three storage mechanisms were mainly adopted in optoelectronic memories: photochromic effect[10], defects trapping of photogenerated carriers[11–17], and tunneling of photogenerated carriers[1,18,19]. For photochromic memories, high optical power density is essential to break or connect the bonds in the polymer

[1]Songshan Lake Materials Laboratory, 523808 Dongguan, Guangdong, P. R. China. [2]Institute of Physics, Chinese Academy of Sciences, 100190 Beijing, P. R. China. [3]State Key Laboratory for Mesoscopic Physics and Frontiers Science Center for Nano-optoelectronics, School of Physics, Peking University, 100871 Beijing, P. R. China. [4]Department of Physics, The University of Hong Kong, 999077 Hong Kong, P. R. China. [5]Department of Physics, University of Oslo, P.O. Box 1048 Oslo NO-0316, Norway. ✉e-mail: zhurui@iphy.ac.cn; zxmei@iphy.ac.cn

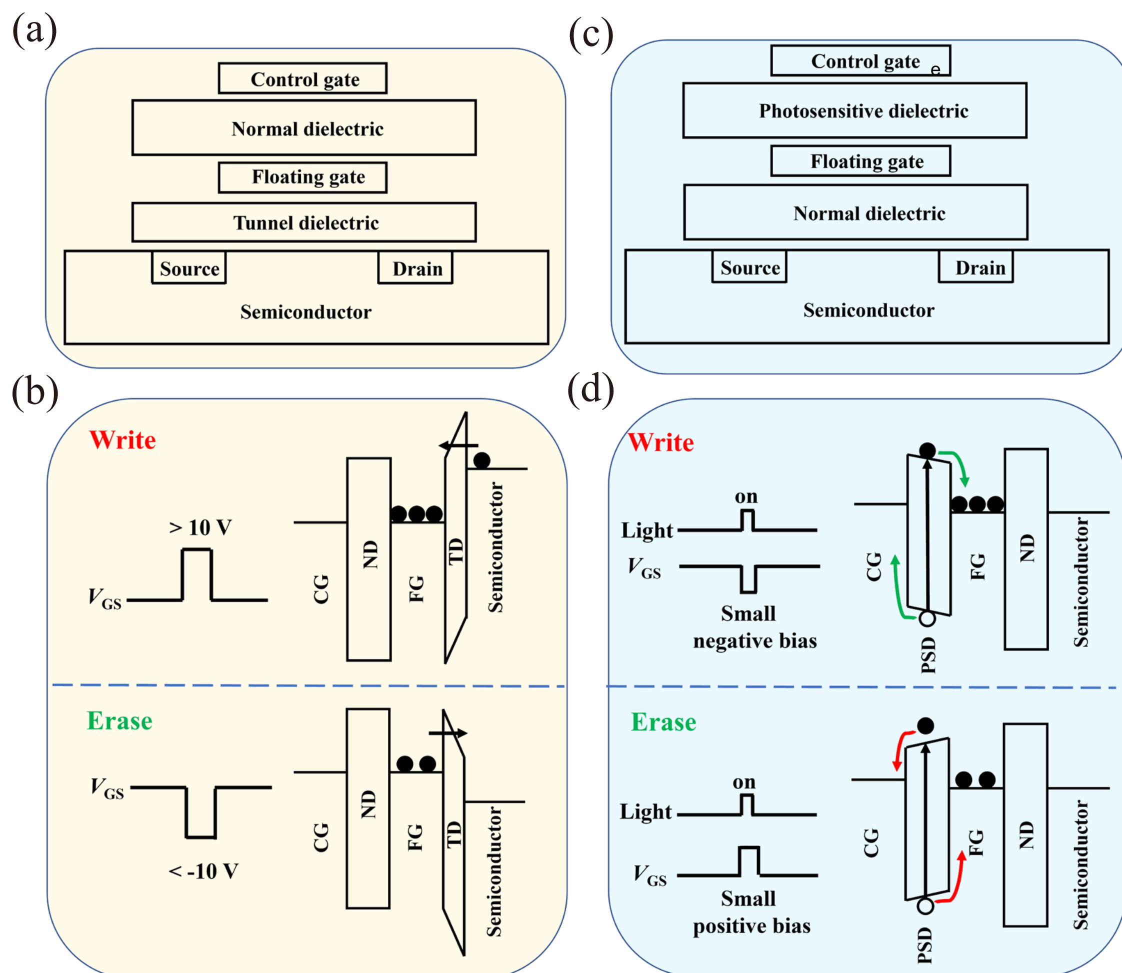

Fig. 1 | Difference between flash memory and PSD-based optoelectronic memory in terms of the device structure and write and erase processes. a Flash memory structure. **b** Write and erase processes in the flash memory. **c** Structure of the PSD-based optoelectronic memory. **d** Write and erase processes in the PSD-based optoelectronic memory. The solid balls represent the electrons, and the hollow balls represent the holes. The arrows represent flow directions of electrons or holes.

materials and modulate their resistance. A high-programming voltage is then a major requisite for the electrical regulation of the polymers. In the case of defects trapping in channel or interface, the photogenerated carriers will be captured in the defects and released slowly after turning off the optical pulse, known as persistent photoconductivity (PPC) effect. Because only a fraction of photogenerated carriers can be trapped by defects, the high optical intensity is needed to provide enough photogenerated carriers. Meanwhile, a large V_{GS} needs to be exerted to release the carriers trapped by the defects. The third-type memory device utilizes the tunneling of the photogenerated carriers in channel through the TD to FG under the large V_{GS}. Similarly, because the probability of tunneling is small, the high optical power density is needed to provide enough photogenerated carriers into the channel.

As discussed above, a situation of high energy consumption will be inevitably encountered, considering the fact that the programming voltage and optical power density used in the previously reported optoelectronic memories were in excess of 20 V and 1 mW m^{-2}, respectively. In addition, the strong dependence of these structures on the selection of channel materials and the control of defects makes it difficult to adapt to certain situations with different channel materials. It is urgently needed to develop new storage structure and working principle to realize the optoelectronic memory with low energy consumption and improved compatibility.

Results

Design of novel optoelectronic memory based on the PSD

A new optoelectronic memory structure with a photosensitive dielectric (PSD) is designed on the basis of the flash memory cell. As shown in Fig. 1c, the original normal dielectric (ND) layer in the flash memory (Fig. 1a) is replaced with a PSD layer, and the TD layer between the FG and the channel is replaced with an ND layer. Critically, the dielectric layer instead of the channel serves as the photosensitive component. The new PSD should own three significant features—(i) it works as a dielectric layer in dark, that is, it is insulating; (ii) it acts as a semiconductor and produce photogenerated carriers under illumination; (iii) it forms a distinct band offset with the FG layer and offers an energy barrier sufficient to block the carriers trapped in the FG.

It can be recognized that, with the assistance of an optical excitation with a suitable wavelength matching the bandgap of the PSD layer, the injection of electrons will be achieved by applying a small negative V_{GS} pulse, as indicated by the green arrows in Fig. 1d. Under the illumination, the photogenerated electrons in the PSD layer will drift to the FG layer driven by the negative V_{GS}. After turning off the optical pulse, the PSD immediately becomes insulating, and the electrons in the FG are bound in the potential well formed by the energy barriers between the PSD, FG, and ND separately. In this case, the threshold voltage (V_{th}) of the transistor will positively shift[2], therefore accomplishing the writing and storage process of “0” state.

Correspondingly, extraction of electrons will be achieved by applying a small positive V_{GS} pulse combined with a similar optical pulse, as indicated by the red arrows in Fig. 1d. The electrons bounded in the FG will easily transport across the original barrier between the FG and PSD due to illumination-induced conductivity change in the PSD layer. Once stopping the optical pulse, the PSD immediately becomes insulating again, no electrons stay in the FG, and the threshold voltage will shift to the negative direction, erasing the "0" state and storaging "1" state.

In contrast to the optoelectronic memory reported in literature, the PSD-based memory introduces an innovative approach of injecting and extracting carriers with low power consumption as well as avoiding tradeoffs with choosing specific channel materials. The first and foremost, since the programming voltage is only used to guide the transport direction of the photogenerated carriers originated from the PSD, its value does not need to be large. Another outstanding merit of the new architecture is the efficient use of the intrinsic excitation-generated carriers in PSD for charge storage. It will remarkably decrease the need for a high optical power density. Thirdly, photogenerated carriers are generated in the PSD layer rather than in the general channel layer. It indicates that this new idea may feasibly work in different types of transistors, with less selectivity for channel materials (e.g., Si, oxides, 2D materials).

The fabrication and performance of the novel PSD-based optoelectronic memory

The key for realizing the designed structure and mechanism is to find a suitable PSD material that exhibits the above-mentioned three features. Recently, Ga_2O_3 ultra-wide bandgap semiconductor (~5.0 eV[20]) has attracted considerable attention in the solar-blind UV detection research field[20–23]. Zheng et al.[24] and Kaya et al.[25] reported the use of Ga_2O_3 a the high-K dielectric layer for MOSFETs in 2007 and 2016, respectively. It should be noticed that the electron affinity of Ga_2O_3 is ~4 eV, which enables the formation of a sufficiently high band offset between Ga_2O_3 and metals with high work function, such as Au having the work function of 5.2 eV[26]. These data suggest that Ga_2O_3 may satisfy all tradeoffs as the PSD we are looking for.

To start with, we prepared a two-terminal vertical structure based on Ga_2O_3, which is the top and core part of the PSD-based optoelectronic memory. The schematic diagram and top view of the magnified micrograph of the fabricated device are shown in Fig. 2a and Supplementary Fig. S1, respectively. Note that no diffraction peaks were observed in the XRD curve of the Ga_2O_3 film (Supplementary Fig. S2), proving the amorphous nature of the Ga_2O_3 deposited by radio-frequency magnetron sputtering at room temperature. Figure 2b demonstrates the core level spectra of O 1*s* and Ga 3*d* measured by X-ray photoelectron spectroscopy (XPS), and Ga:O atomic ratio approaches 2:3 determined by the ratio of the integrated photoelectron peak area of O 1*s* to Ga 3*d*. It suggests fewer oxygen vacancy defects in the Ga_2O_3 film and thus lower dark current in the device[23]. As shown in Fig. 2c, the dark current of the vertical structure is maintained at the ~10^{-14} A level, which is basically the limit of the source meter. In addition, a C–V test is conducted on the vertical structure at 5 MHz (Fig. 2d) and a relative permittivity value is extracted as 13.01, which shows that Ga_2O_3 can work as an insulating dielectric layer. The transmission spectrum of the Ga_2O_3 film is illustrated in Fig. 2e, with a direct bandgap of ~5.1 eV by Tauc's law, as shown in Fig. 2f. It means that the Ga_2O_3 film has strong absorption for light whose wavelength locates at around 250 nm. Correspondingly, an apparent photoresponse is observed in Ga_2O_3 under 254 nm irradiation (Fig. 2c), satisfying the second requirement of the PSD as a semiconductor under suitable illumination. In addition, to decrease the absorption of control gate (CG) in the final device (Fig. 1c), 15 nm half-transparent Au was deposited on Ga_2O_3 as CG. The result manifests that about 50% of light is still absorbed and reflected by the top CG (Fig. 2e).

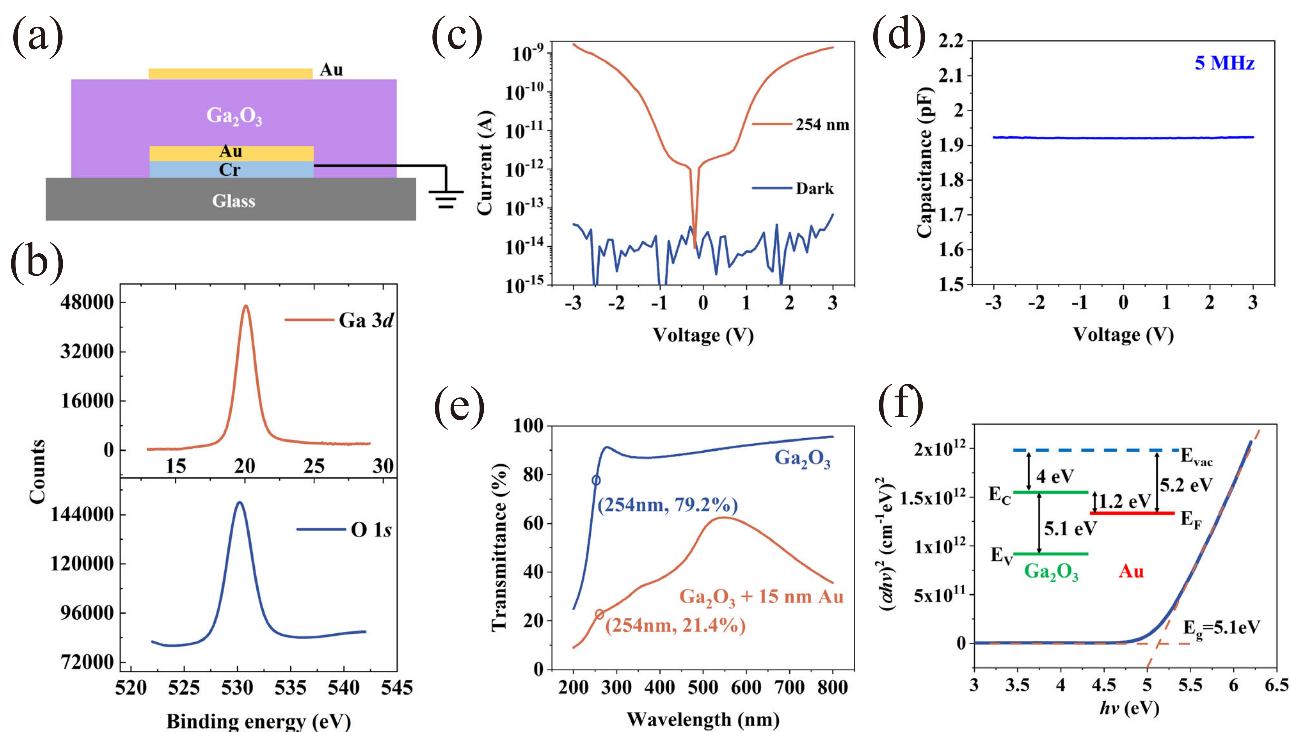

Fig. 2 | Characterization of the vertical structure based on Ga_2O_3 film. **a** Schematic diagram of the vertical structure. **b** XPS spectra of the Ga_2O_3 film. The upper and lower panels show the core level spectra of Ga 3*d* and O 1*s*. **c** I–V curves in dark (blue curve) and under 254 nm illumination (orange curve). **d** C–V sweep curve at 5 MHz. **e** Optical transmittance spectra of the Ga_2O_3 (45 nm) film (blue curve) and the Ga_2O_3 (45 nm) + Au (15 nm) film (orange curve). **f** The plot of $(\alpha h\nu)^2$ versus $h\nu$ for Ga_2O_3 film. The inset is the energy band structure of Ga_2O_3 and Au.

https://doi.org/10.1038/s41467-023-40938-y

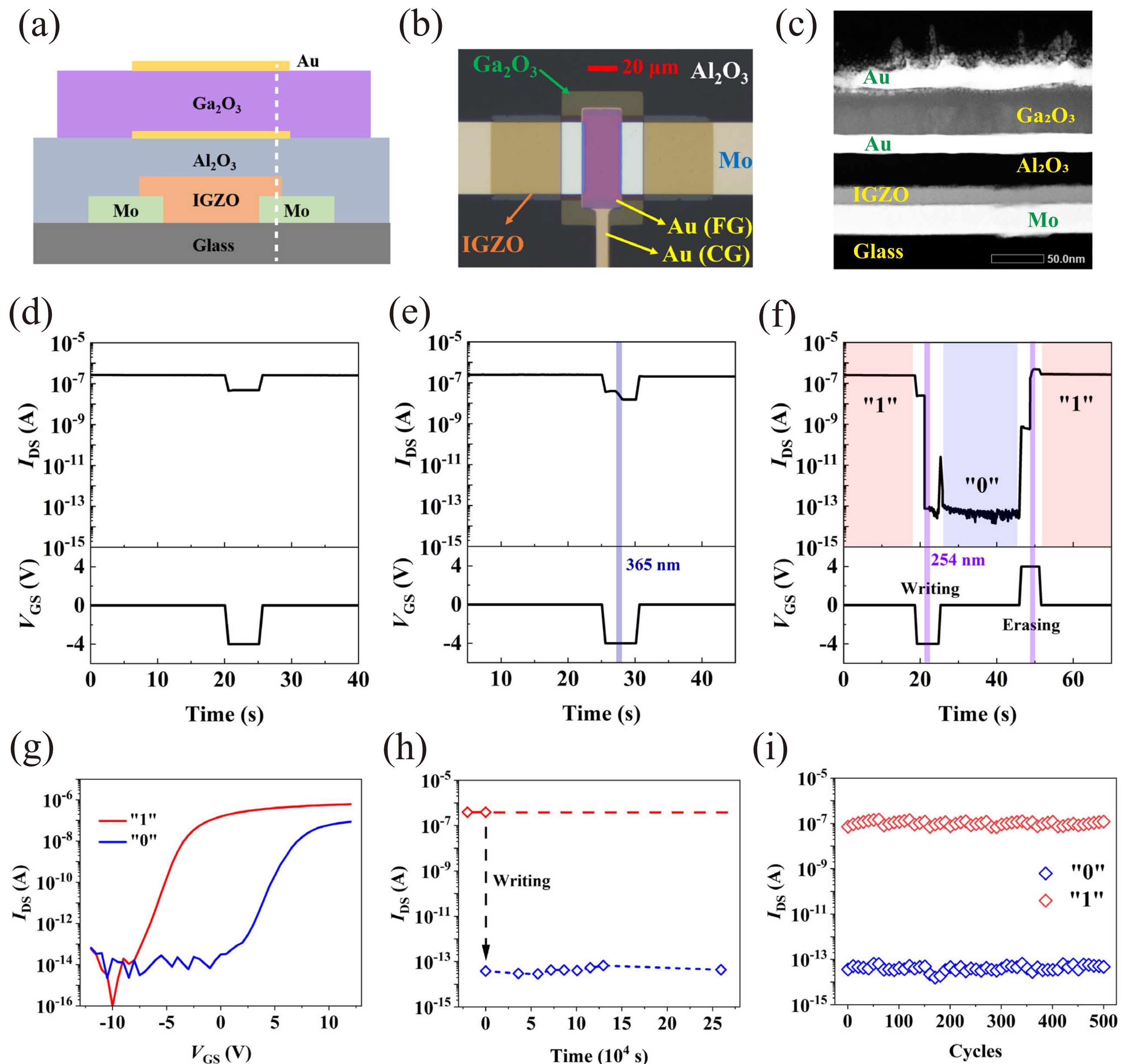

Fig. 3 | The structure and performance of the final PSD-based optoelectronic memory device. a Schematic diagram of the device. **b** Top view of the magnified optical micrograph of the fabricated device. **c** TEM cross-sectional image corresponding to the position of the white dashed line in (**a**). **d** The writing result by $V_{GS} = -4$ V pulse. **e** The writing result by a combination of $V_{GS} = -4$ V pulse and a 365 nm of 160 μW cm^{-2} optical pulse. **f** The single write/erase process and corresponding results. (optical pulse: 254 nm, 160 μW cm^{-2}, 1 s; V_{GS} pulse: −4 V / 4 V). **g** Transfer characteristic curves in states "0" and "1". **h** Retention test for up to 72 h. (optical pulse: 254 nm, 160 μW cm^{-2}, 1 s; V_{GS} pulse: −4 V). **i** Fatigue test result for 500 cycles. (optical pulse: 254 nm, 160 μW cm^{-2}, 1 s; V_{GS} pulse: −4 V/4 V). **g**–**i** Blue represents "0", and red represents "1".

For the ultimate demonstration, we constructed a top-gate InGaZnO (IGZO) thin film transistor (TFT), the bottom part of the PSD-based optoelectronic memory. The schematic diagram and the top view magnified micrograph of the fabricated device are shown in Supplementary Fig. S3a, S3b, respectively. The initial linear region of the output characteristic curve (Supplementary Fig. S3c) clearly indicates the formation of a good ohmic contact between the source/drain electrodes and the channel. The transfer characteristic curve (Supplementary Fig. S3d) shows that the device has normal TFT performance with a high on-off ratio (>10^8), which is the precondition for a large memory window.

The two-terminal Ga_2O_3 vertical structure and top-gate IGZO TFT are stacked together to compose the final PSD-based optoelectronic memory device. Figure 3a, b show the schematic diagram and top view of the magnified micrograph of the final device, respectively. Figure 3c is the cross-sectional TEM image, where Au, Ga_2O_3, Au, Al_2O_3, IGZO, and Mo layers are clearly observed exhibiting sharp interfaces. To avoid the possible contaminations of the photoresist at the interfaces, each lithography process is optimized as shown in Supplementary Fig. S4. Importantly, the band alignment of this memory structure matches the new conception introduced in Fig. 1d, as confirmed in Supplementary Fig. S5.

The transfer characteristics of the PSD-based optoelectronic memory (Supplementary Fig. S6) basically retain the performance of the isolated IGZO TFT, except slightly larger subthreshold swing (*SS*) value and more negative threshold voltage (V_{th}). That is ascribed to a smaller capacitance caused by the series connection of the two capacitors (CG/PSD/FG + FG/ND/channel) in the device.

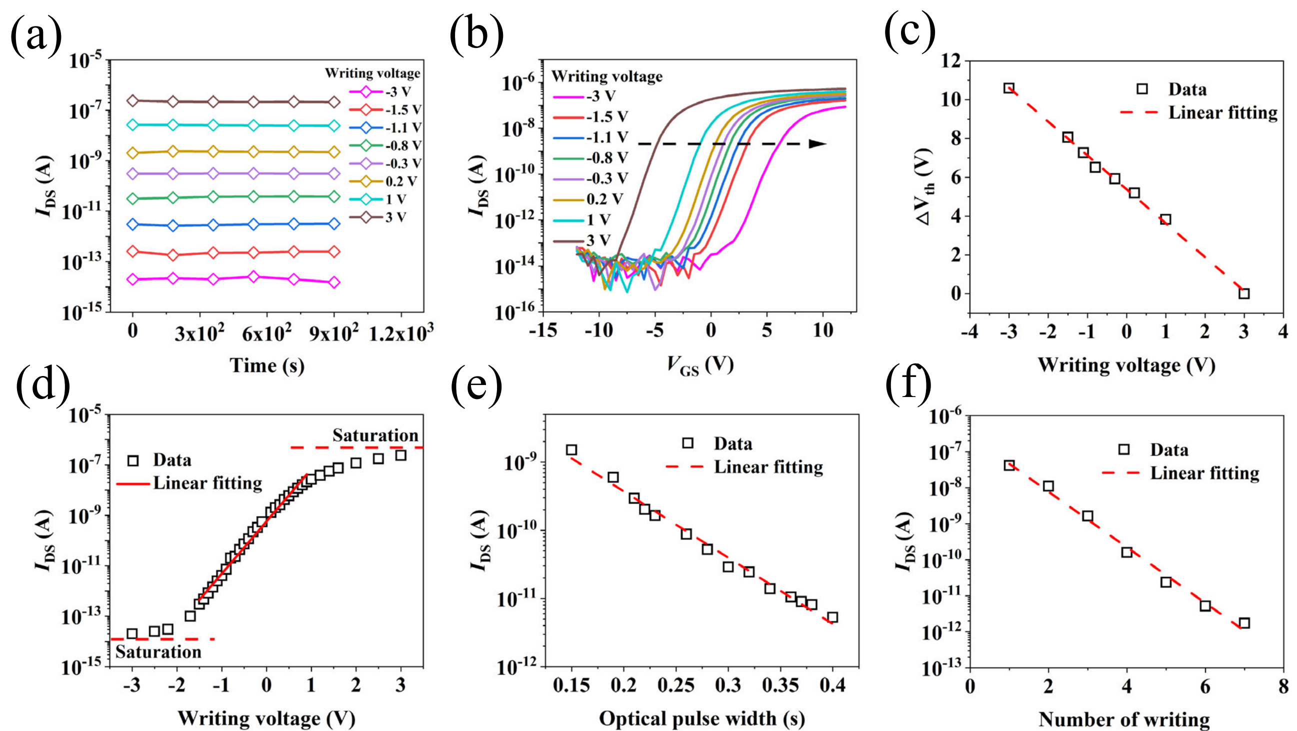

Fig. 4 | Tests of the multilevel storage. a Retention test of different states formed by different V_{GS} pulses (keeping the optical pulse at 254 nm, 160 μW cm^{-2}, 1 s). The corresponding relationship between color and writing voltage is shown in the legend. **b** Transfer curves of different states formed by different V_{GS} pulses. The corresponding relationship between color and writing voltage is shown in the left legends. **c** Linear fitting of ΔVth for different states formed by different V_{GS} pulse. The V_{th} is defined as the value of V_{GS} when $I_{DS} = (W/L) \times 1$ nA, W and L are width and length of the channel, respectively. **d** Linear fitting of I_{DS} for different states formed by different V_{GS} pulse. **e** Linear fitting of I_{DS} for different states formed by different optical pulse width (optical pulse: 254 nm, 160 μW cm^{-2}; V_{GS} pulse: −4 V). **f** Linear fitting of I_{DS} for different states formed by different number of writing (optical pulse: 254 nm, 60 μW cm^{-2}, 50 ms; V_{GS} pulse: −3 V).

It is clearly demonstrated that only applying negative V_{GS} pulses is not sufficient to inject charges into the FG, as shown in Fig. 3d, as there is no light to turn on the PSD. Moreover a combination of the negative V_{GS} pulse with a 365 nm optical pulse cannot cause the carriers' injection either (Fig. 3e), since 365 nm does not match the bandgap of Ga_2O_3.

The single writing and erasing process and their results are shown in Fig. 3f to verify the memory function of the final device. V_{GS} and the drain voltage (V_{DS}) under read status were 0 V and −0.5 V, respectively. In the initial state "1", the drain current (I_{DS}) is stably maintained at ~3×10^{-7} A. After applying a V_{GS} pulse = −4 V and a 254 nm optical pulse with as low as 160 μW cm^{-2} power, I_{DS} is stably maintained at ~5×10^{-14} A, corresponding to "0" state with a memory window >10^6. As expected, the electrons are injected into the FG from the CG and trapped in the FG in this process, causing a right shift of the threshold voltage (Fig. 3g). Then we apply a V_{GS} = 4 V pulse and an identical optical pulse, and the I_{DS} recovered to the initial value, ~3×10^{-7} A. The phenomenon indicates that after the 254 nm light "turns on" Ga_2O_3, the electrons stored in the FG are rapidly released back to the CG under the electric field induced by the small positive V_{GS} and net electrons in FG. Apparently, the electrons' transport direction can be discerned from the synchronous variation of the gate current (I_{GS}) during the writing and erasing operations of I_{DS}, as shown in Supplementary Fig. S7. During the writing process, the negative I_{GS} (process "B") proves that electrons flow from CG to FG, while the positive I_{GS} (process "C") proves that electrons flow from FG to CG during the erasing process. The in-situ monitoring results of the electrons' transport behavior perfectly is in accordance with the designed injection/extraction processes highlighted by green and red arrows in Fig. 1d, solidly corroborating the feasibility of the working principle in PSD-based optoelectronic memory.

The data retention time is an important parameter of the device reliability. As shown in Fig. 3h, the memory window constantly keeps >10^6 even after 72 h. The original data of retention test are shown in Supplementary Fig. S8. Fatigue characteristic is another important parameter of the device reliability. The cyclic program/erase (P/E) endurance of the device was examined and exhibited in Fig. 3i. After 500 cycles, the memory window has almost not changed.

Compared with conventional three-terminal transistor devices, the addition of optical pulse provides a new route to multilevel storage in nonvolatile memories. Here, three different methods are explored to illustrate the multilevel storage capability. First, we change the amplitude of the V_{GS} pulse to implement multilevel storage. As shown in Fig. 4a, the more negative V_{GS} is, the more electrons are injected into the FG, and the lower I_{DS} is. During the 15 min retention test, every state keeps stable. Figure 4b shows the transfer curves corresponding to every state. The more negative the V_{GS} is, the more the curve right shifts. Figure 4c shows that V_{th} shifts (ΔV_{th}) extracted from Fig. 4b have a good linear relationship with the amplitude of V_{GS} pulse. Linear fitting result of I_{DS} for different states indicates in a write voltage between −2 V and 1 V, corresponding to a current storage window range of approximately 6 orders of magnitude, we can obtain a large number of linearly related storage states, as shown in Fig. 4d. Then, by changing the optical pulse width and the number of writings, we can also obtain a linearly related multilevel storage states, as shown in Fig. 4e, f.

Table 1 compares key parameters of the PSD-based optoelectronic memory proposed by us with previously reported ones. The new memory exhibits comparable performance regarding memory window, retention time, and fatigue cycles. The programming voltage

Table 1 | Comparison of key parameters with previously reported optoelectronic memories

Working principle	Photosensitive material	Programming voltage	OPD [mW/cm^2]	Programming time	Memory window	Tested retention time	Tested fatigue cycles	Ref.
Photochromic	DAEs	60 V	–	5 s	>10^5	500 days	70	10
Tunneling	MoS_2	100 V	5×10^4	1 s	>10^7	10^4 s	70	18
Tunneling	SnS_2	40 V	–	5 s	>10^4	–	–	1
Tunneling	PtS_2	30 V	41	100 ms	>10^3	–	–	19
Defects	BTBT	120 V	40	12 s	>10^6	2×10^4 s	–	11
Defects	MoS_2/PbS	40 V	0.027	5 s	<3	10^4 s	2000	12
Defects	WSe_2	80 V	210	5 s	10^6	4.5×10^4 s	200	13
Defects	Penance	60 V	71.59	120 s	10^4	100 days	3	14
Defects	PDVT-10:N2200	40 V	5	1 s	10^5	2×10^4 s	500	15
Defects	MoS_2	80 V	501	10 s	10^7	10^4 s	250	16
Defects	TiO_2	50 V	1	30 s	<2	10^4 s	–	17
PSD	Ga_2O_3	4 V	0.16	1 s	>10^6	2.6×10^5 s	500	This work

OPD optical power density.

and optical power density are particularly far lower than those ever-reported values, which reveals the contribution of PSD in the novel structure.

To get closer to the practical application, we use an AlGaN UV-LED[27] as the light source to realize the programming function of the PSD-based optoelectronic memory. The electroluminescence spectrum of the UV-LED is shown in Supplementary Fig. S9a. The photograph of the test configuration is exhibited in Supplementary Fig. S9b. As seen from these data, the function of writing and erasing has been successfully achieved by using the combination of AlGaN UV-LED and Ga_2O_3 PSD-based optoelectronic memory (Supplementary Fig. S9c). This demonstration paves the way for future integration of optoelectronic memory circuits.

Discussion

The optoelectronic memory with IGZO as a channel and Ga_2O_3 as the PSD is the first example of PSD-based device architecture not only conceptually proposed, but also tested in experimental conditions. It paves the way to explore more PSD candidates and various channel materials. In addition, the memory performance can be further optimized. For instance, longer retention and faster writing speed may be potentially achieved by reducing the defect in PSD. By optimizing the *SS* parameter of the transistor, a larger memory window can be obtained under the same write conditions, or a smaller programming voltage and optical power density be obtained under the same memory window. The number of multi-level storages can also increase with more subdivided write methods or larger memory windows.

Results and discussion

In summary, with the booming development of ultra-wide-bandgap semiconductors, the boundary between semiconductors and insulators has become more and more blurred. Here, Ga_2O_3 is opted as the PSD material in novel nonvolatile optoelectronic memory, considering its admirable insulating property in dark and semiconducting performance under illumination. Via integrating the Ga_2O_3 PSD with the common floating gate device, unique programming methods are established with low programming voltage (4 V), low optical power density (160 μW cm^{-2}), and multilevel storage (storage window of approximately six orders of magnitude with good linear relationship). This memory may potentially fill the gap between big data and limited storage capacity as well as reducing the energy consumption. Meanwhile, the new structure and mechanism can be readily extended to other FETs compatible with photolithography, such as Si-based, organic or 2D materials-based FETs, to achieve high-performance solid-state memory and flexible memory. Remarkably, the device can also be used as a multi-function sensor, integrating the sensing and storage abilities together[28,29].

Methods

Preparation of a two-terminal vertical structure based on Ga_2O_3

First, the glass substrate is sonicated with acetone, alcohol, and deionized water for 10 min in sequence. After drying the glass substrate with nitrogen, 10 nm Cr layer is deposited by radio-frequency (RF) magnetron sputtering to improve the adhesion of Au (32 nm) on glass, followed by using photolithography and etching into bottom electrode pattern. Then Ga_2O_3 (45 nm) is deposited by RF magnetron sputtering (60 W) in an oxygen-rich condition, and 15 nm Au is then sputtered on Ga_2O_3. Patterning of the top electrode and gallium oxide is completed in sequence. Finally, the device is annealed at 200 °C for 30 min in air.

Preparation of IGZO top-gate TFT

First, use the same method to clean the glass substrate. Then grow Mo (30 nm) by magnetron sputtering, and define the channel length (20 μm) and width (50 μm) by photolithography. Then grow IGZO (20 nm) by RF magnetron sputtering. After IGZO is patterned, Al_2O_3 (30 nm) is grown by atomic layer deposition (ALD) at 200 °C. Then Au (15 nm) is deposited by RF magnetron sputtering. After that, Au is etched to form the gate pattern, and the aluminum oxide is etched to expose the source and drain electrodes for testing. Similarly, the device is annealed at 200 °C for 30 min in air.

Preparation of PSD-based optoelectronic memory device

Based on the TFT manufacturing process, the original Au (10 nm) is etched to form the FG pattern. Then follow the same method to grow 45 nm Ga_2O_3 as the PSD layer and 15-nm semitransparent Au as the CG. Finally, Au, Ga_2O_3 and Al_2O_3 are etched in sequence. Similarly, the device is annealed at 200 °C for 30 min in air.

Material characterization

The XPS measurements were conducted using a multifunctional X-ray Photoelectron Spectroscopy analysis platform (ESCALAB Xi+, ThermoFisher), where an electron source was used for charge compensation. TEM cross-sectional image was obtained by TEM (JEM-F200). The transmission spectrum was measured by UV–Vis–NIR Spectrophotometer (UH4150, Hatachi). The XRD

curve was measured by an X-ray diffractometer (D8-ADVANCE, Bruker).

Device characterization

Except for C–V test performed by Keysight B1500A and current source of AlGaN UV-LED provided by Keithley 2400, all other electrical tests were conducted by Keithley 2636B. The light source other than the LED is generated by an UV-enhanced xenon lamp, and the wavelength is adjusted by a monochromator. The generation of optical pulses is achieved by placing an electric switch between the xenon lamp and the monochromator. The optical power density is calibrated by a standard Si photodetector.

Data availability

All raw data are available from the author upon request. Almost all of testing data shown in this manuscript are themselves raw I–V or I–t data instead of being processed.

References

1. Gao, F. et al. Low optical writing energy multibit optoelectronic memory based on SnS_2/h-BN/graphene heterostructure. *Small* **17**, 2104459 (2021).
2. Bez, R., Camerlenghi, E., Modelli, A. & Visconti, A. Introduction to flash memory. *Proc. IEEE* **91**, 489–502 (2003).
3. Pavan, P., Bez, R., Olivo, P. & Zanoni, E. Flash memory cells-an overview. *Proc. IEEE* **85**, 1248–1271 (1997).
4. Meena, J., Sze, S., Chand, U. & Tseng, T.-Y. Overview of emerging nonvolatile memory technologies. *Nanoscale Res Lett.* **9**, 526 (2014).
5. Gallagher, W. J. & Parkin, S. S. P. Development of the magnetic tunnel junction MRAM at IBM: from first junctions to a 16-Mb MRAM demonstrator chip. *IBM J. Res. Dev.* **50**, 5–23 (2006).
6. Auciello, O., Scott, J. F. & Ramesh, R. The physics of ferroelectric memories. *Phys. Today* **51**, 22–27 (1998).
7. Atwood, G. & Bez, R. Current status of chalcogenide phase change memory. in *63rd Device Research Conference Digest, 2005. DRC '05*. 29–33 (IEEE, 2005).
8. Xu, C, Dong, X, Jouppi, N. P. & Xie, Y Design implications of memristor-based RRAM cross-point structures. in *2011 Design, Automation & Test in Europe* 1–6 (IEEE, 2011).
9. Zhai, Y. et al. Toward non-volatile photonic memory: concept, material and design. *Mater. Horiz.* **5**, 641–654 (2018).
10. Leydecker, T. et al. Flexible non-volatile optical memory thin-film transistor device with over 256 distinct levels based on an organic bicomponent blend. *Nat. Nanotech* **11**, 769–775 (2016).
11. Pei, K. et al. A high-performance optical memory array based on inhomogeneity of organic semiconductors. *Adv. Mater.* **30**, 1706647 (2018).
12. Wang, Q. et al. Nonvolatile infrared memory in MoS_2/PbS van der Waals heterostructures. *Sci. Adv.* **4**, eaap7916 (2018).
13. Xiang, D. et al. Two-dimensional multibit optoelectronic memory with broadband spectrum distinction. *Nat. Commun.* **9**, 2966 (2018).
14. Chen, J.-Y., Chiu, Y.-C., Li, Y.-T., Chueh, C.-C. & Chen, W.-C. Non-volatile perovskite-based photomemory with a multilevel memory behavior. *Adv. Mater.* **29**, 1702217 (2017).
15. Gao, C. et al. Heterostructured vertical organic transistor for high-performance optoelectronic memory and artificial synapse. *ACS Photonics* **8**, 3094–3103 (2021).
16. Liu, C. et al. Polarization-resolved broadband MoS_2/black phosphorus/MoS_2 optoelectronic memory with ultralong retention time and ultrahigh switching ratio. *Adv. Funct. Mater.* **31**, 2100781 (2021).
17. Sun, Z., Li, J., Liu, C., Yang, S. & Yan, F. Trap-assisted charge storage in titania nanocrystals toward optoelectronic nonvolatile memory. *Nano Lett.* **21**, 723–730 (2021).
18. Lee, D. et al. Multibit MoS_2 photoelectronic memory with ultrahigh sensitivity. *Adv. Mater.* **28**, 9196–9202 (2016).
19. Chen, Y. et al. Asymmetric hot carrier tunneling van der Waals heterostructure for multibit optoelectronic memory. *Mater. Horiz.* **7**, 1331–1340 (2020).
20. Cui, S., Mei, Z., Zhang, Y., Liang, H. & Du, X. Room-temperature fabricated amorphous Ga_2O_3 high-response-speed solar-blind photodetector on rigid and flexible substrates. *Adv. Opt. Mater.* **5**, 1700454 (2017).
21. Han, Z. et al. Boosted UV photodetection performance in chemically etched amorphous Ga_2O_3 thin-film transistors. *Adv. Opt. Mater.* **8**, 1901833 (2020).
22. Qin, Y. et al. Ultra-high performance amorphous Ga_2O_3 photodetector arrays for solar-blind imaging. *Adv. Sci.* 2101106 https://doi.org/10.1002/advs.202101106 (2021).
23. Zhu, R., Liang, H., Hu, S., Wang, Y. & Mei, Z. Amorphous-Ga_2O_3 optoelectronic synapses with ultra-low energy consumption. *Adv. Electron. Mater.* **8**, 2100741 (2021).
24. Zheng, J. F. et al. $Ga_2O_3(Gd_2O_3)/Si_3N_4$ dual-layer gate dielectric for InGaAs enhancement mode metal-oxide-semiconductor field-effect transistor with channel inversion. *Appl. Phys. Lett.* **91**, 223502 (2007).
25. Kaya, A. et al. Ga_2O_3 as both gate dielectric and surface passivation via sol-gel method at room ambient In *Proc. SPIE*, Vol. 9957, Wide Bandgap Power Devices and Applications 995709 https://doi.org/10.1117/12.2239177 (2016).
26. Mohamed, M. et al. Schottky barrier height of Au on the transparent semiconducting oxide β-Ga_2O_3. *Appl. Phys. Lett.* **101**, 132106 (2012).
27. Liu, S. et al. Drive high power UVC-LED wafer into low-cost 4-inch era: effect of strain modulation. *Adv. Funct. Mater.* 2112111 https://doi.org/10.1002/adfm.202112111 (2022).
28. Zhang, X. et al. An artificial spiking afferent nerve based on Mott memristors for neurorobotics. *Nat. Commun.* **11**, 51 (2020).
29. Zhou, F., Chen, J., Tao, X., Wang, X. & Chai, Y. 2D materials based optoelectronic memory: convergence of electronic memory and optical sensor. *Research* **2019**, 1–17 (2019).

Acknowledgements

This work is supported by the National Natural Science Foundation of China (Grants Nos. 12174275, 62174113, 61874139, 61904201, and 11875088), Guangdong Basic and Applied Basic Research Foundation (Grants No. 2019B1515120057). The work at the University of Oslo was enabled by the M-ERA.NET funds administrated by the Research Council of Norway via project number 337627 as well as the INTPART program at the Research Council of Norway via project number 322382.

Author contributions

R.Z. designed and conducted the experiments, and prepared the manuscript. Z.M. and H.L. guided the experiments and revised the manuscript. S.L., Y.Y., and X.W. provided the AlGaN LED and related EL characterization. F.C.C.L., A.K., and G.Z. provided valuable advices on the optimization of device interface and related tests. All authors discussed the results and contributed to the final version of the paper.

Competing interests

The authors declare no competing interests.

Additional information

Supplementary information The online version contains supplementary material available at https://doi.org/10.1038/s41467-023-40938-y.

Correspondence and requests for materials should be addressed to Rui Zhu or Zengxia Mei.

Peer review information *Nature Communications* thanks Jiajiu Zheng, and the other, anonymous, reviewer for their contribution to the peer review of this work. A peer review file is available.

Reprints and permissions information is available at http://www.nature.com/reprints

Publisher's note Springer Nature remains neutral with regard to jurisdictional claims in published maps and institutional affiliations.

Open Access This article is licensed under a Creative Commons Attribution 4.0 International License, which permits use, sharing, adaptation, distribution and reproduction in any medium or format, as long as you give appropriate credit to the original author(s) and the source, provide a link to the Creative Commons licence, and indicate if changes were made. The images or other third party material in this article are included in the article's Creative Commons licence, unless indicated otherwise in a credit line to the material. If material is not included in the article's Creative Commons licence and your intended use is not permitted by statutory regulation or exceeds the permitted use, you will need to obtain permission directly from the copyright holder. To view a copy of this licence, visit http://creativecommons.org/licenses/by/4.0/.

© The Author(s) 2023