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Multifilamentary switching of Cu/SiO$_x$ memristive devices with a Ge-implanted a-Si underlayer for analog synaptic devices

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Abstract

Various memristive devices have been proposed for use in neuromorphic computing systems as artificial synapses. Analog synaptic devices with linear conductance updates during training are efficiently essential to train neural networks. Although many different analog memristors have been proposed, a more reliable approach to implement analog synaptic devices is needed. In this study, we propose the memristor of a Cu/SiO$_x$/implanted a-SiGe$_x$/p^{++} c-Si structure containing an a-Si layer with properly controlled conductance through Ge implantation. The a-SiGe$_x$ layer plays a multifunctional role in device operation by limiting the current overshoot, confining the heat generated during operation and preventing the silicide formation reaction between the active metal (Cu) and the Si bottom electrode. Thus, the a-SiGe$_x$ interface layer enables the formation of multi-weak filaments and induces analog switching behaviors. The TEM observation shows that the insertion of the a-SiGe$_x$ layer between SiO$_x$ and c-Si remarkably suppresses the formation of copper silicide, and reliable set/reset operations are secured. The origin of the analog switching behaviors is discussed by analyzing current-voltage characteristics and electron microscopy images. Finally, the memristive-neural network simulations show that our developed memristive devices provide high learning accuracy and are promising in future neuromorphic computing hardware.

Introduction

As we enter a new era of big data, it is becoming increasingly important to find more efficient ways to process vast amounts of data. The current standard von Neumann computing architecture, however, is facing limitations in performance due to difficulties in data transfer between the central processing unit and memory[1–6]. To address this issue, neuromorphic computing systems, which are based on biological human brains, have been proposed as an alternative technology[7–11].

Various neural networks consisting of artificial neurons and synapses quickly and efficiently perform intelligent functions in parallel computing architectures. Artificial neuromorphic computing systems mimicking the human brain achieve intelligent tasks, such as recognition, reasoning, and learning. Inspired by biological brains that handle complex tasks at low power, neuromorphic computing systems are in the spotlight as a way to overcome these limitations[12].

Neuromorphic computing systems consist of artificial neurons and synaptic devices as fundamental building blocks. Among the synaptic devices, memristive devices are one of the most popular approaches to mimic biological synapses[13–18]. Memristors generally use a metal-insulator-metal structure, and the commonly proposed model for conductance switching is the formation and

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rupture of conductive filaments inside an active layer. When one or more filaments are connected between the top and bottom electrodes, memristive devices produce a low-resistance state (LRS), while they produce a high-resistance state (HRS) when the filaments break. These memristive devices can be divided into valence change memory (VCM) and conductive bridging random access memory (CBRAM) based on the formation mechanism of conductive filaments[19–21]. The conductive filaments in VCM devices mainly consist of oxygen-deficient metal oxide phases modulated by oxygen vacancy concentrations, while CBRAM devices have conductive filaments composed of reduced metal ions provided by the active electrode. CBRAM devices typically consist of an insulating layer sandwiched between one active metal electrode and another inert electrode. Active electrodes, such as Cu, Ag, or Ni, are mainly used as the top electrodes, and metal oxide-based insulators, such as SiO_x, a-Si, or SiN_x, have been used as the switching layer[7,22]. CBRAM typically has a longer retention and a higher on/off ratio than VCM[23]. CBRAM has shown promising performance as a nonvolatile memory device and has commercial applications[24]; however, it has struggled for use as artificial synaptic devices in neuromorphic computing applications[7,25,26]. One of the challenging issues for synaptic devices for high-performance computing is analog switching to mimic biological synapses with multilevel conductance levels. Gradual analog switching of the synaptic devices ensures multilevel conductance states with repetitive voltage pulses, which is one of the essential requirements for high-accuracy recognition in artificial neural network computing[12].

Conventional CBRAM devices, however, have faced challenges in their use as artificial synaptic devices in neuromorphic computing applications, such as exhibiting an abrupt switching behavior caused by the so-called positive feedback effect[20]. Once metal clusters or filaments are formed in a switching layer, the formation of conductive filaments is accelerated by increases in device temperature induced by Joule heating, resulting in very sharp switching near a threshold set voltage. This abrupt switching causes difficulty to precisely modulate the conductance levels of the synaptic devices, resulting in poor performance in neuromorphic computing. To suppress abrupt switching and induce gradual switching in CBRAM devices, various approaches have been attempted, such as modification of program schemes[27,28], seeding of filament formation sites[29,30], incorporation of thermal enhancement layers[31] or graded metal composition layers[4,32]. Many previous approaches have shown promising results; however, considering the complexities of the fabrication process and CMOS compatibilities, a novel approach to address these issues is needed.

Accordingly, in this study, we propose a multilayered memristor consisting of $Cu/SiO_x/a\text{-}SiGe_x/c\text{-}Si$ that exhibits gradual switching behavior induced by a multiple weak filament formation mechanism[33]. An amorphous Si layer was inserted as a current limiting layer under the switching layer, SiO_x, to suppress the positive feedback effect and in turn prevent abrupt switching. In this study, the resistance of the current limiting layer was precisely controlled by varying the implantation dose of Ge ions. The implanted Ge ions induced structural defects in the amorphous Si-based current limiting layer, which served as carrier transport sites[34]. We demonstrated that the optimal resistance of the current limiting layer could be obtained by Ge implantation for reliable analog switching of CBRAM devices. The suppression of the second phase formation at the electrode interface was another key factor. We confirmed that no second phase was formed at the interface of an active metal electrode and a switching layer by electron microscopy. Our proposed Cu-based bilayer device exhibited promising analog behavior in terms of gradual switching characteristics while maintaining high on-off ratios through the insertion and conductivity tuning of the current limiting layer. Finally, we performed MNIST (Modified National Institute of Standards and Technology) recognition simulations of memristive neural networks considering the actual behaviors of the memristor devices developed in this study and demonstrated a high recognition efficiency approaching 90%. This result showed that Cu-based bilayer memristor devices could have potential applications in memristive neuromorphic computing systems as artificial synapses.

Experimental

The membrane was a $Cu/SiO_x/a\text{-}SiGe_x/p^{++}$ c-Si structure featuring a via-hole design. An a-Si was deposited onto the p^{++} c-Si wafer using a low-pressure chemical vapor deposition (SHF-150 L) process, with a thickness of 70 nm. The pressure and temperature during the deposition were maintained at 150 mTorr and 550 °C, respectively, and the flow rate of SiH_4 gas was 60 sccm.

Ge ion implantation was performed after LPCVD a-Si was formed on a Si wafer substrate. For the ion implantation process, a 400 kV ion implanter owned by the Korea Institute of Science and Technology was utilized. The Ge ions were accelerated by the ion acceleration part of the implantation system, moved along the ion beam line and were implanted into the a-Si thin film fixed to the ion chamber. The Ge ions were accelerated to 70 kV at room temperature and irradiated with fluxes of 1×10^{10}, 1×10^{11}, 1×10^{12}, 1×10^{13}, 1×10^{14}, 5×10^{14}, 8×10^{14}, and 4×10^{15} fluxes/cm^2. The ion flux was measured using a Faraday cup and was maintained at a level of less than 50 nA/cm^2 s.

To measure the conductance of the a-SiGe$_x$ thin film under different flow rates, a via-hole-type device with an Ag/a-SiGe$_x$/c-Si structure was manufactured. A 100 nm SiN$_x$ thin film was deposited on the a-SiGe$_x$ layer using plasma-enhanced chemical vapor deposition. The SiN$_x$ thin film was patterned with a photoresist mask with a circular hole array shape and selectively etched in a 1:6 BOE solution to form a via-hole structure. The photoresist was removed with acetone, and 300-nm thick Ag top electrodes were made using the lift-off process and thermal evaporation equipment. The device, prepared as described above, utilized a source measuring device (Keithley 236) connected to the probe station to measure the conductance of the a-SiGe$_x$ thin film. The oscillation current–voltage (I–V) characteristic curve was obtained through a voltage sweep of $0 \rightarrow +5$ V and $0 \rightarrow -5$ V.

The analog synaptic Cu-based bilayer device was manufactured by the above process. After the via-hole structure was formed, a SiO$_x$ layer of 5 nm was deposited through PECVD, and a 300-nm thick Cu top electrode was fabricated using the lift-off process and beam evaporation equipment.

TEM was conducted to observe the interface of the device and the cluster morphology. The specimen was analyzed using the Hitachi-NX5000 through the focused ion beam (FIB) technique. A device that was FIB milled enough to transmit an electron beam was observed through a Titan TM 80-300. Both conventional transmission electron microscopy and scanning transmission electron microscopy were performed via the above equipment. The Cu silicide at the a-Si or the c-Si interface with a switching layer was observed using TEM. The distribution of the metal cluster was also confirmed by visualizing the cross-sectional area of the device under an applied voltage.

The electrical properties of the device were tested using the source measurement devices Keithley 236 and Keithley 4200. To obtain the electrical properties of the Cu-based bilayer device, the voltages were repeatedly swept at $0 \rightarrow +7$ V and $0 \rightarrow -7$ V. To verify the analog characteristics of the device, repetitive pulse signals were applied. A potentiation/depression pulse was applied for 10 μs with an amplitude of 11 V/−8 V. The read pulse was applied with an amplitude of 1 V. To measure the synaptic retention time, we applied 50, 100, 200, 500, and 1000 times the same amplitude and width as the potentiation pulse.

The morphology of a-Si in Ge implants was simulated using the TRIM software package (SRIM 2003 ver.13). TRIM is software that uses the cascade Monte Carlo method to calculate the spatial distribution and number of vacancy defects of Si and Ge atoms on the injection amount of Ge ions. The simulation consisted of an a-Si (70 nm)/c-Si layer, and the density was set to 2.285 g/cm^3

and 2.329 g/cm^3 [35]. The acceleration voltage was adjusted to 70 kV, and the input values for displacement energy and lattice bonding energy were 12 eV and 2 eV, respectively.

$$Vancancy\ concentration = v_i \left(\frac{vacancies}{ions} \right)$$
$$\times fluence \left(\frac{ions}{cm^2} \right) \times \frac{1}{\rho \left(\frac{atoms}{cm^3} \right)} \times 0.01$$

Through the above equation, the vacuum concentration by depth was derived. Fluence is the number of ions injected per unit area. Y is the atomic density of the substrate. v_i is calculated by subtracting the replacement collisions from the target displacement from the number of vacancies generated when an ion was injected. The multiplication factor of 0.01 is used because ~99% of implant damage is immediately recovered during implantation at room temperature[36,37].

MNIST pattern recognition simulation was conducted with the Cu-based bilayer device as a hardware model. To reflect the experimental synaptic device characteristics, the limited number of states and nonlinearity were considered. The simulation was conducted with a multilayer perceptron with three neuron layers. The MNIST pattern consisted of 28×28 pixels and an input layer with a total of 784 neurons. The hidden layer had 128 neurons, and the output neurons were composed of 10 different labels. Initially, a random input value was entered, and the weight was gradually updated through the gradient descent method. The weight strength of the input was reflected by the hardware model and passed through the synapse to the next neuron. The collected values were transmitted to the next neural network using an activation function called ReLU (rectified linear unit). Finally, the softmax function produced a normalized probability distribution of each output value. A total of 60,000 MNIST training datasets were used to perform learning, and the learning was repeated 100 times.

Results and discussion

To investigate the insertion effect of a current limiting layer, I–V characteristics of the single-layer structure device of (a) Cu/SiO$_x$/p^{++} c-Si and the double-layer structure device of (b) Cu/SiO$_x$/a-Si/p^{++} c-Si were measured, as shown in Fig. 1. For both of the measurements, the compliance current was set at 1.0 mA. In the case of a single layer, when the device was formed, a strong single filament appeared to be made. This result was confirmed due to the abrupt current increase at the threshold switching voltage. Furthermore, once the devices were formed, the devices could not be reset and became stuck in a set state, as shown in Fig. 1a. The reasons for the set-stuck failure was the excessive formation of the filaments
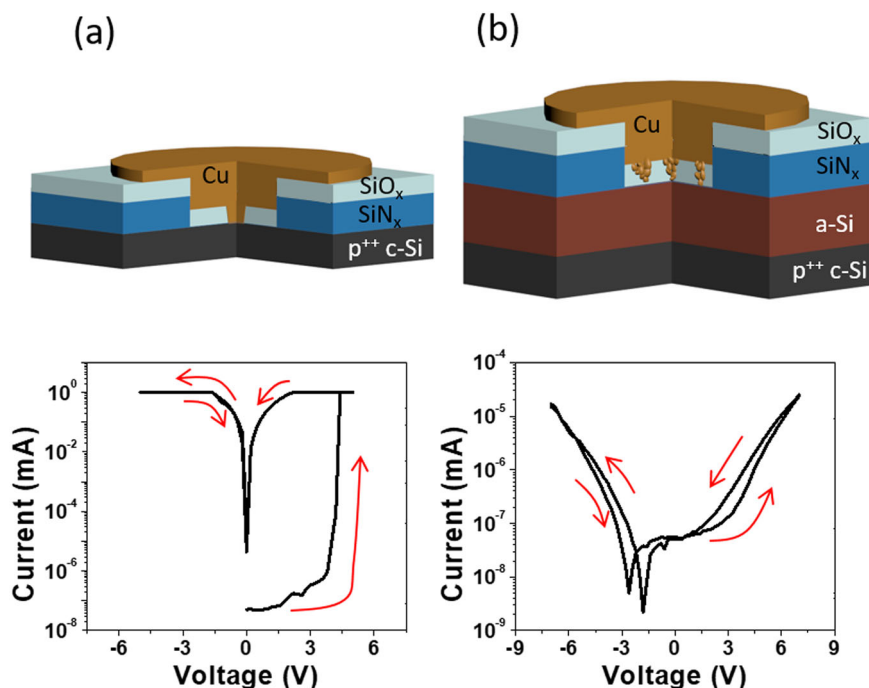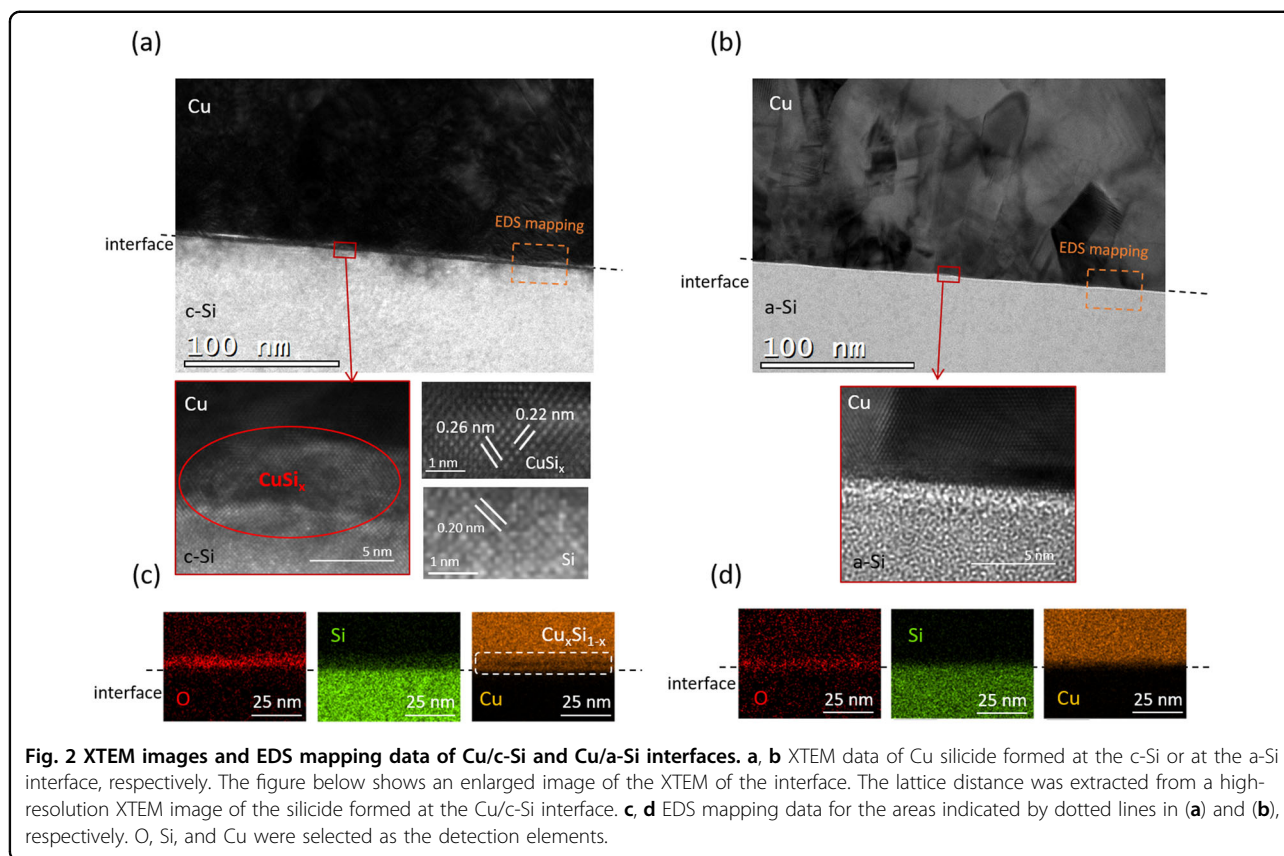
Fig. 1 Schematics and current-voltage curves for Cu/SiO$_x$/p^{++} c-Si and Cu/SiO$_x$/a-Si/p^{++} c-Si memristive devices. a Schematic view of a Cu/SiOx/p + + c-Si device with a via-hole structure. **b** Schematic diagram of a device in which a-Si is inserted as a buffered layer into the single-layer device of the structure. Graphs below the schematic diagrams of the devices are the characteristic current–voltage curves of the corresponding devices.

or irreversible chemical reactions at the electrode interface without the current limiting layer[38]. When an amorphous a-Si current limiting layer was inserted between a switching layer and a bottom electrode, the set switching exhibited a gradual transition, and reset failure was not observed, as shown in Fig. 1b. Additionally, the set-reset transition was repetitively enabled. The gradual set switching observed in the bilayer devices was potentially due to the formation of multiple filaments in an active layer, as illustrated in the device schematic. This will be clarified from the microscopic observation of the devices by transmission electron microscopy (TEM) later in this study. Different metal materials, such as Ag and Ni, were tested for the active electrode in the bilayer device structure. Considering the memory retention time and endurance of the devices, we used Cu as a suitable active electrode. Detailed device characteristics with Ag, Cu and Ni as active electrodes are provided in Figure S1. For the rest of this study, Cu was used as the active electrode.

To investigate whether a second phase, such as silicide, was formed at the interface between Cu/a-Si and Cu/c-Si, test samples were fabricated by depositing a Cu thin film on a c-Si wafer and on an a-Si-coated Si wafer. In Fig. 2, the XTEM images and EDS mapping of the test samples were measured to show the Cu/c-Si interface and Cu/a-Si interface. From Fig. 2a, a thin layer of Cu silicide was

formed at the Cu/c-Si interface. The Cu silicide phase was identified by analyzing the lattice constants in the HR-TEM images. A crystalline Si phase with a lattice constant of 0.20 nm was observed, as shown in in Fig. 2a, and a Cu silicide phase in the region between the Cu thin film and the Si wafer layer had lattice constant values of 0.26 nm and 0.22 nm. This result supported that the Cu silicide phase was Cu$_{15}$Si$_4$[39,40]. Figure 2c presents the EDS mapping images of the Cu/c-Si sample denoted in Fig. 2a. Copper silicides in the presence of oxygen incorporated during deposition of Cu are partially converted into SiO$_x$ and Cu, as discussed in more detail in the supplementary information (Fig. S2). The SiO$_x$ layer was uniformly distributed at the interface, as shown in Fig. 2c. Additionally, Si and Cu were intermixed in the region between the Si wafer and the Cu thin film where the silicide was formed. Figure 2b shows the cross-sectional TEM images of the test sample with the insertion of an a-Si thin film between the Cu thin film and the Si wafer. Different from the Cu/c-Si interface, a Cu silicide phase was not observed at the Cu/a-Si interface. The EDS mapping results of the Cu/a-Si/p^{++} c-Si interface in Fig. 2d showed that SiO$_x$ was rarely observed, and the distribution of Si and Cu devices was more abrupt compared to Fig. 2c. This effect was more evident in high-temperature experiments (Fig. S2). Memristor devices reach over 200 °C locally by Joule
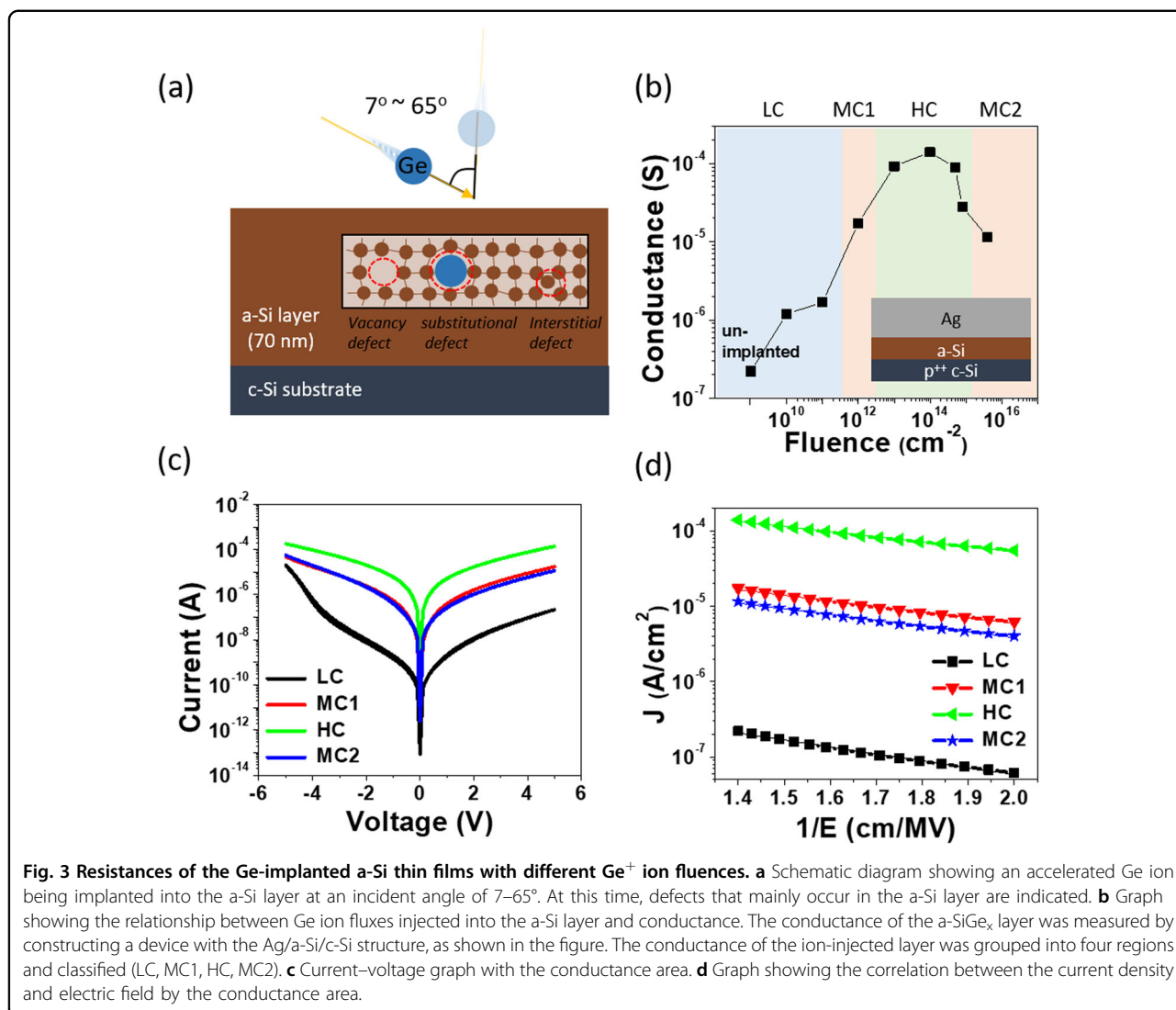
Fig. 2 XTEM images and EDS mapping data of Cu/c-Si and Cu/a-Si interfaces. a, b XTEM data of Cu silicide formed at the c-Si or at the a-Si interface, respectively. The figure below shows an enlarged image of the XTEM of the interface. The lattice distance was extracted from a high-resolution XTEM image of the silicide formed at the Cu/c-Si interface. **c, d** EDS mapping data for the areas indicated by dotted lines in (**a**) and (**b**), respectively. O, Si, and Cu were selected as the detection elements.

heating during forming and programming operations[31,39,41]. To mimic this heating effect, the test samples were annealed at 200 °C in a N_2 atmosphere for 20 min. Heat treatment accelerated the formation of Cu silicide, especially for the test sample without a-Si. In contrast, Cu silicide was not observed in the test sample with a-Si. The detailed TEM studies are presented in the supplementary information (Fig. 2S). The rich hydrogen contents of the a-Si thin film were considered to prevent silicide formation at the Cu/c-Si interface, ensuring reliable switching behavior of the CBRAM devices.

However, the LPCVD a-Si layer with a conductance value of 100 nS greatly limited the current. This excessive current limitation prevented sufficient filament formation in the switching layer. Therefore, the device using the a-Si layer as the underlayer provided a low on/off (LRS/HRS) ratio.

To adjust the conductance of the a-Si thin film, Ge ion implantation with varying influences and injection angles was conducted. The Ge ion was selected as an implantation element since it does not form a second phase with Si[42]. In addition, the Ge ion has a larger atomic size than Si, effectively inducing defect formation in the a-Si layer. To confine the implanted Ge ions within the a-Si underlayer, both the fluences and the injection angles were accordingly adjusted. The defect formation profiles

depending on the fluences and injection angles were calculated by a TRIM method and are presented in Fig. S3. Based on the TRIM simulation results, the proper implantation parameters were selected. The injection angles were adjusted in the range of 7–65° and the implantation dose or fluence was varied from $10^{10}–10^{15}$ flux/cm^2, as shown in Fig. 3a, b.

The conductivity of the ion-injected a-SiGe$_x$ thin film was measured and is presented in Fig. 3b. The conductance of the unimplanted a-Si thin film was 2×10^{-7} S, and the conductance value of the a-Si thin film increased as the ion implantation fluence increased. The highest conductance was obtained at a 1×10^{14} flux/cm^2 fluence, followed by decreases in the conductance with increasing fluence. This conductance decrease could potentially be attributed to the heat generated in the a-Si thin film during high fluence injection, resulting in self-annealing and then defect annihilation. The conductance of the a-SiGe$_x$ thin film by injection flux could be classified into four main ranges. The conductance below 2×10^{-6} S is classified as low conductance (LC), that above 2×10^{-5} S as high conductance (HC) and that between them as medium conductance (MC). MC can be classified further according to the fluence. MC1 is the injection range at 1×10^{12} fluence/cm^2, and MC2 is that at 1×10^{16} fluence/cm^2. In Fig. 3c, the *I–V*

Fig. 3 Resistances of the Ge-implanted a-Si thin films with different Ge⁺ ion fluences. a Schematic diagram showing an accelerated Ge ion being implanted into the a-Si layer at an incident angle of 7–65°. At this time, defects that mainly occur in the a-Si layer are indicated. **b** Graph showing the relationship between Ge ion fluxes injected into the a-Si layer and conductance. The conductance of the a-SiGe$_x$ layer was measured by constructing a device with the Ag/a-Si/c-Si structure, as shown in the figure. The conductance of the ion-injected layer was grouped into four regions and classified (LC, MC1, HC, MC2). **c** Current–voltage graph with the conductance area. **d** Graph showing the correlation between the current density and electric field by the conductance area.
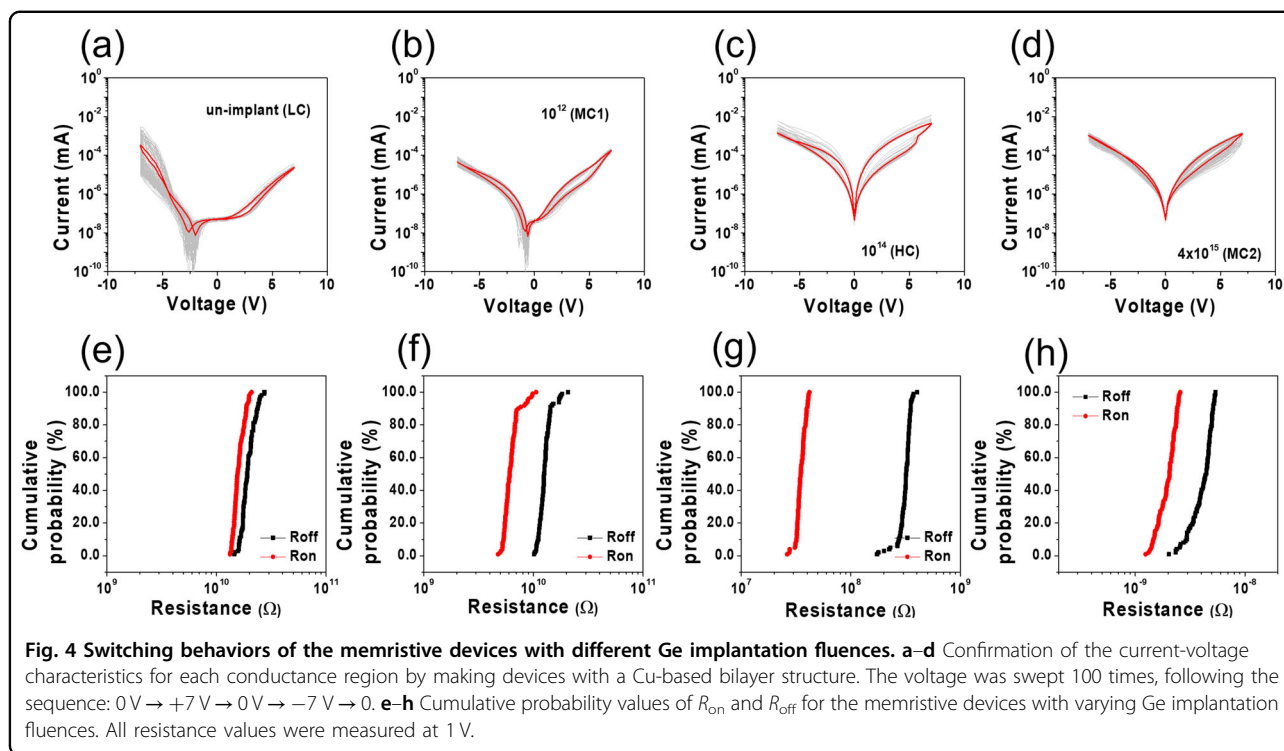
characteristics of the two-terminal devices with an Ag/a-SiGe$_x$/p^{++} c-Si structure were measured in each region of LC, MC1, HC, and MC2. The voltage was swept in the direction $0 \rightarrow 5\,V \rightarrow 0 \rightarrow -5\,V \rightarrow 0$. The currents of the device at the same voltage were proportional to the conductances of the a-SiGe$_x$ thin film with various fluences. The $I-V$ curves were symmetric on the MC1, HC and MC2 devices, while the curve of the LC device was not symmetric. The current transport mechanism of the Ge-implanted a-SiGe$_x$ thin film was confirmed by the slope of the J vs. $1/E$ curves in Fig. 3d, where E is an electric field applied in the device. The vacancy defects formed in the implanted a-SiGe$_x$ thin film acted as deep traps, and the current flowed through the trap-assisted-tunneling (TAT) phenomenon in which electrons were predominantly transported via the traps[43–46].

$$J_i \sim \exp\left(-\frac{4\sqrt{2qm_{ox}}}{3}\Phi_t^{\frac{3}{2}}/E\right)$$

The equation above shows the correlation between the current density and E when the device current flows in TAT mode. The linear relationship between $1/E$ and ln$J$ in a-SiGe$_x$ thin films in Fig. 3d showed that the currents in all test devices predominantly flowed by the TAT mechanism. This result supported the conductance increases with increasing fluence, as shown in Fig. 3b, which was attributed to the increased implantation-induced defects. The trap density as a function of the ion fluence could also be determined using the TAT model, and a good correlation between the conductance and the trap density was observed; more details can be found in the supplementary information (Fig. S5 and Table S1).

The effects of the conductance of the current limiting layer on the electrical characteristics of the devices were investigated. A Cu-based bilayer device, where the a-SiGe underlayer had various conductances of LC, MC1, HC,
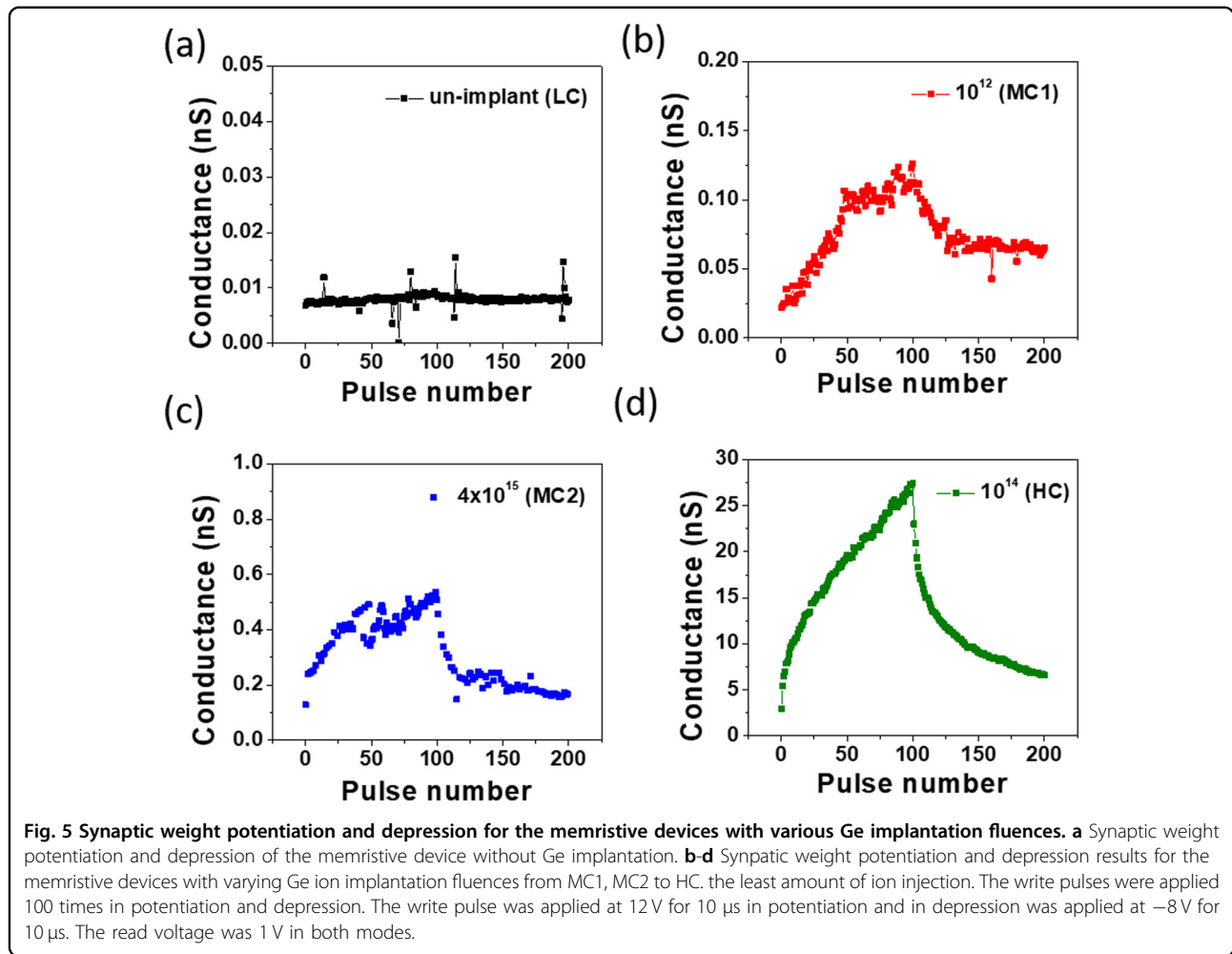
Fig. 4 Switching behaviors of the memristive devices with different Ge implantation fluences. a–d Confirmation of the current-voltage characteristics for each conductance region by making devices with a Cu-based bilayer structure. The voltage was swept 100 times, following the sequence: $0\,V \rightarrow +7\,V \rightarrow 0\,V \rightarrow -7\,V \rightarrow 0$. **e–h** Cumulative probability values of R_{on} and R_{off} for the memristive devices with varying Ge implantation fluences. All resistance values were measured at 1 V.

and MC2, was fabricated, and the $I–V$ characteristics were verified and are presented in Fig. 4a–d. The voltage was swept in the direction $0 \rightarrow 7\,V \rightarrow 0 \rightarrow -7\,V \rightarrow 0$, and the voltage sweep was repeated 100 times for all devices. Under all conditions, the devices exhibited gradual switching behaviors, and in both the HRS and LRS states, the device conductance depended on the conductance of the a-SiGe$_x$ underlayer. As expected, the increased conductances of the current limiting underlayer resulted in increased device resistances.

The cumulative probabilities of the resistances in the HRS and LRS states for all the devices are presented in Fig. 4e–h. Depending on the conductances of the a-SiGe$_x$ thin film, the on-resistance (R_{on}) and off-resistance (R_{off}) ratio of the devices varied. The R_{on}/R_{off} ratio represents a dynamic range of elements, and a larger R_{on}/R_{off} ratio is more beneficial in neural network computing. The R_{on}/R_{off} ratio of the device with an LC underlayer was 1.2, and the R_{on}/R_{off} ratio of the device with an HC underlayer was 8.9. This results showed that excessive current restriction inhibited strong filament formation in the switching layer, resulting in a lower R_{on}/R_{off} ratio. The device with an HC underlayer provided a relatively large R_{on}/R_{off} since a conductive path was sufficiently formed in the switching layer.

The synaptic potentiation and depression behaviors of memristive devices are crucial factors for the implementation of high-performance neuromorphic computing hardware. Synaptic potentiation and depression

were investigated by applying repetitive voltage pulses and measuring the conductances of the memristive devices. In Fig. 5a–d, the potentiation and depression tests of devices with different conductances of LC, MC1, HC, and MC2 were conducted. The pulse schemes in potentiation and depression were 12 V and -8 V amplitudes with the same pulse width of 10 μs, respectively. Conductance updates were barely observed for the LC device, as shown in Fig. 5a due to the excessive current limitation that prevented the formation of sufficiently conductive filaments in the switching layer. The devices with MC1 and MC2 conductances had a large on/off conductance ratios compared to devices with LC conductance and showed larger cycle-to-cycle variations since the stable filament formation was inhibited, as shown Fig. 5b, c. Finally, as shown in Fig. 5d, the device with HC conductance exhibited a larger on/off conductance ratio of (9.3) and reduced cycle-to-cycle variations, as shown in Fig. 5d.

Additional synaptic potentiation and depression tests were performed for the devices with HC conductance. As shown in Fig. 6a, in potentiation, a 10 μs pulse with an amplitude of 11 V was applied, and the conductance readings at 1 V were repeated several times. Similarly, in depression, a 10 μs pulse with an amplitude of -8 V was applied, and a read pulse was 1 V. In Fig. 6(b), potentiation and depression were repeated with 20, 50, 100, and 200 pulses. The on/off conductance ratio increased as the number of pulses applied increased. Potentiation and

Fig. 5 Synaptic weight potentiation and depression for the memristive devices with various Ge implantation fluences. a Synaptic weight potentiation and depression of the memristive device without Ge implantation. **b-d** Synaptic weight potentiation and depression results for the memristive devices with varying Ge ion implantation fluences from MC1, MC2 to HC. the least amount of ion injection. The write pulses were applied 100 times in potentiation and depression. The write pulse was applied at 12 V for 10 μs in potentiation and in depression was applied at −8 V for 10 μs. The read voltage was 1 V in both modes.

depression nonlinearity were extracted using the following equations[47–49].

$$G_P = B\left[1 - e^{-v_P P}\right] + G_{\min}$$

$$G_D = G_{\max} - B\left[1 - e^{-v_D(P - P_{\max})}\right]$$

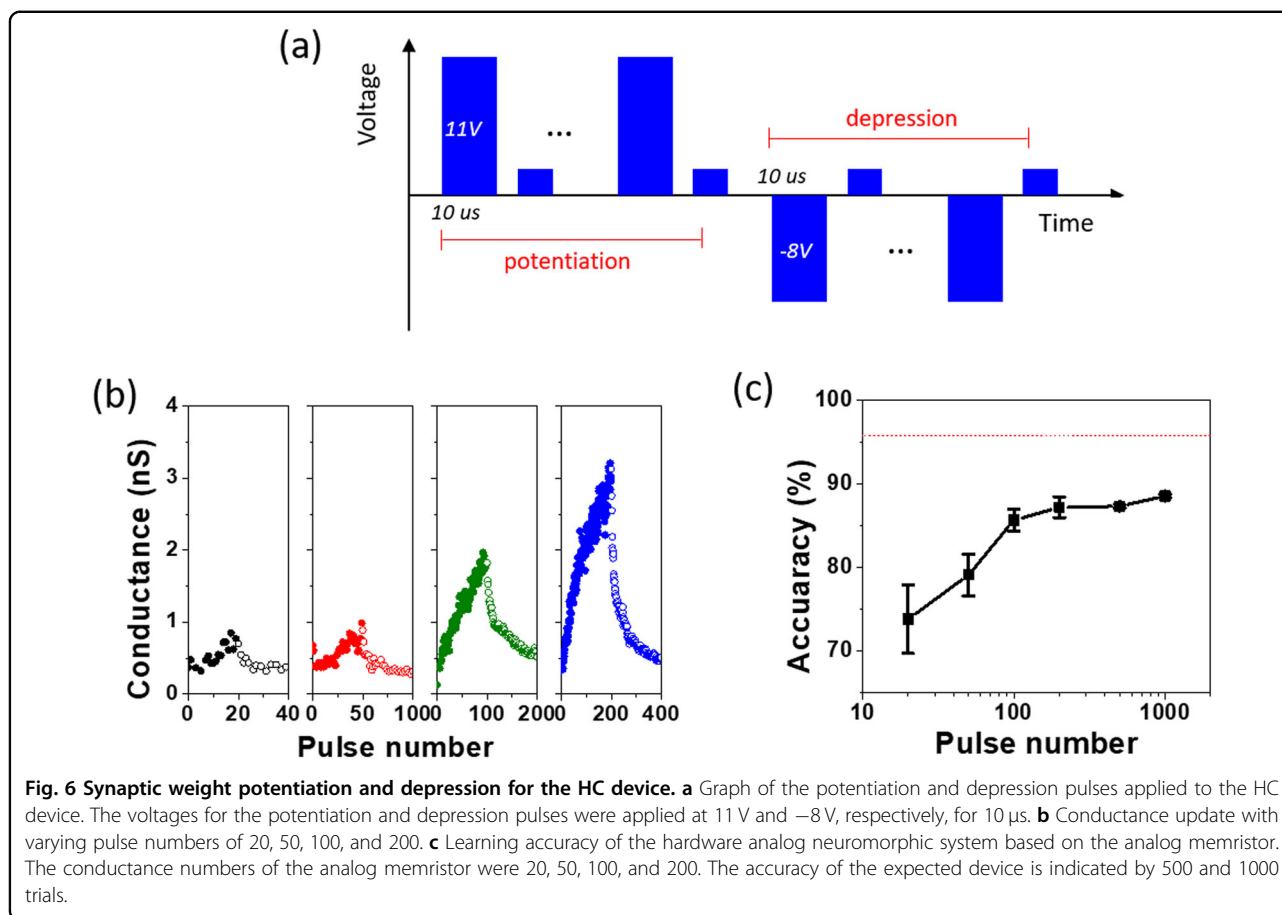$$B = \frac{G_{\max} - G_{\min}}{1 - e^{vP_{\max}}}$$

where G_P and G_D are the conductance values at the times of potentiation and depression, respectively; v_P and v_D are the nonlinear values when the conductance is updated during potentiation and depression, respectively; P and $P_{\max}$ are the number of pulses and the maximum number of pulses, respectively; and $G_{\max}$ and $G_{\min}$ are the maximum and minimum conductivities extracted from the actual potentiation/depression test results.

Memristive neural network hardware requires optimal synaptic devices for high-accuracy computing. The optimal synaptic device needs to have low nonlinearity below

2.0, a high on/off ratio over 10, multi-conductance levels over 2^5, and high symmetry[11,12]. The nonlinearity factor of the Cu-based bilayer device in potentiation maintains a value below 2.0 of 1.0, 2.0, 1.5, and 1.7 with increasing pulse number from 20, 50, 100, to 200 times, respectively. The nonlinearity values in the potentiation were similar to the optimal values. However, in the case of depression, relatively larger nonlinearity values of −3.8, −4.2, −4.3, and −6.3 were extracted with increasing pulse number from 20, 50, 100 to 200 times, respectively.

Multilayer perceptron (MLP) simulations based on the Modified National Institute of Standards and Technology (MNIST) database were performed with consideration of the experimental synapse parameters. In the MLP simulations, the Cu-based bilayer device with the HC conductance was used as a synapse hardware model. . The MNIST database simulation results with consideration of the nonlinearity of the synaptic devices and the conductance levels are presented in Fig. 6c. As shown in Fig. 6c, the MLP neural network architectures were constructed with 28 × 28 input neurons, a hidden layer, and

Fig. 6 Synaptic weight potentiation and depression for the HC device. a Graph of the potentiation and depression pulses applied to the HC device. The voltages for the potentiation and depression pulses were applied at 11 V and −8 V, respectively, for 10 μs. **b** Conductance update with varying pulse numbers of 20, 50, 100, and 200. **c** Learning accuracy of the hardware analog neuromorphic system based on the analog memristor. The conductance numbers of the analog memristor were 20, 50, 100, and 200. The accuracy of the expected device is indicated by 500 and 1000 trials.

10 output neurons. In each synapse weight update calculation, the nonlinearity of the actual devices was considered. When the number of pulses increased during potentiation and depression, the number of conductance levels accordingly increased. Therefore, the operation scheme with the increased number of pulses led to higher precision in the synapse weight values. Therefore, a higher recognition accuracy was expected with an increasing number of pulses.

As expected, as the number of pulses increased from 50 to 200, the recognition accuracy increased from 73.9 to 87.2%. While assuming the synapse parameters at the same values, we performed simulations with more pulses up to 1000 times. Further increases in the pulse number resulted in slight increases in the accuracy, as shown in Fig. 6c. In this case, the accuracy was limited by the nonlinearity rather than the number of conductance levels. Therefore, further device engineering is needed for higher performance.

Biological synapses are known to exhibit short-term forgetting followed by long-term forgetting, which can be suppressed by repetitive learning. Figure 7 shows the forgetting curves of the CBRAM devices with varying numbers of pulses. Voltage pulses of 100 ms with an amplitude

of 7 V were applied several times to a Cu-based bilayer device, and the retention time of the device was measured by reading the device conductance at a pulse with an amplitude of 1 V at equal time intervals. The memory decay behaviors resembled Ebbinghaus's forgetting curve, where short-term memory (STM) decay in an early stage of the retention test was dominant, followed by long-term memory (LTM) decay in a later stage[50]. As shown in Fig. 7b, the maximum conductance value increased as the number of pulses applied increased. This could be understood from the correlation between the filament size and the device retention time[33]. Filaments smaller than a threshold size tended to shrink in the short term by surface diffusion or bulk dissolution to reduce the surface energy, while filaments with larger sizes remained for a longer period of time, improving their retention time.

Further studies were performed to investigate the operation mechanism of the Ge-implanted memristive devices. Figure 8a, b shows the I–V characteristics, LRS and HRS of the CBRAM devices with varying via-hole size from 5 μm to 50 μm. The resistance was estimated from the current measured at 1 V of the I–V curves. From Fig. 8b, both the LRS and HRS resistances decreased with increasing device via-hole diameter (D) following $1/D^n$,
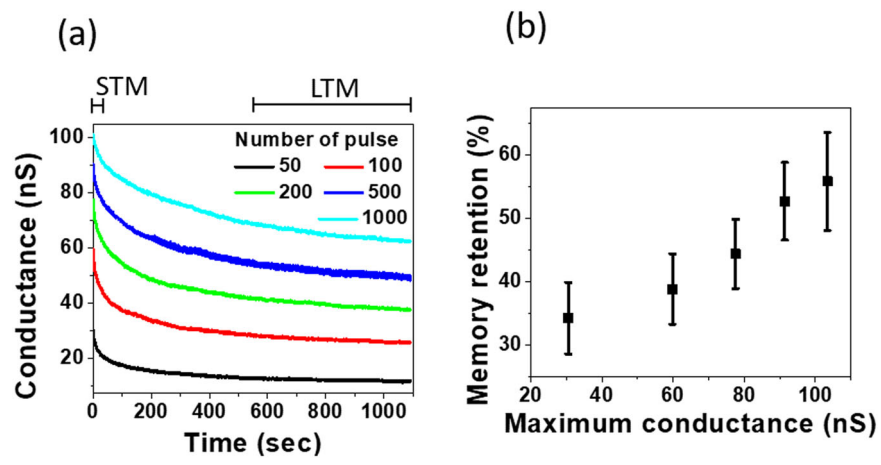
Fig. 7 Retention characteristics for the HC device with varying pulses. a Conductance decay curves appearing after repeated voltage for the HC device (11 V, 10 μs). The number of pulses applied was 50, 100, 200, 500 and 1000. A read pulse of 1 V was applied 2000 times. **b** Remaining conductance after memory loss was extracted from each decay curve by comparing it with the initial conductance and expressed as a percentage value. This value varied depending on the maximum conductance value in the corresponding decay curve.
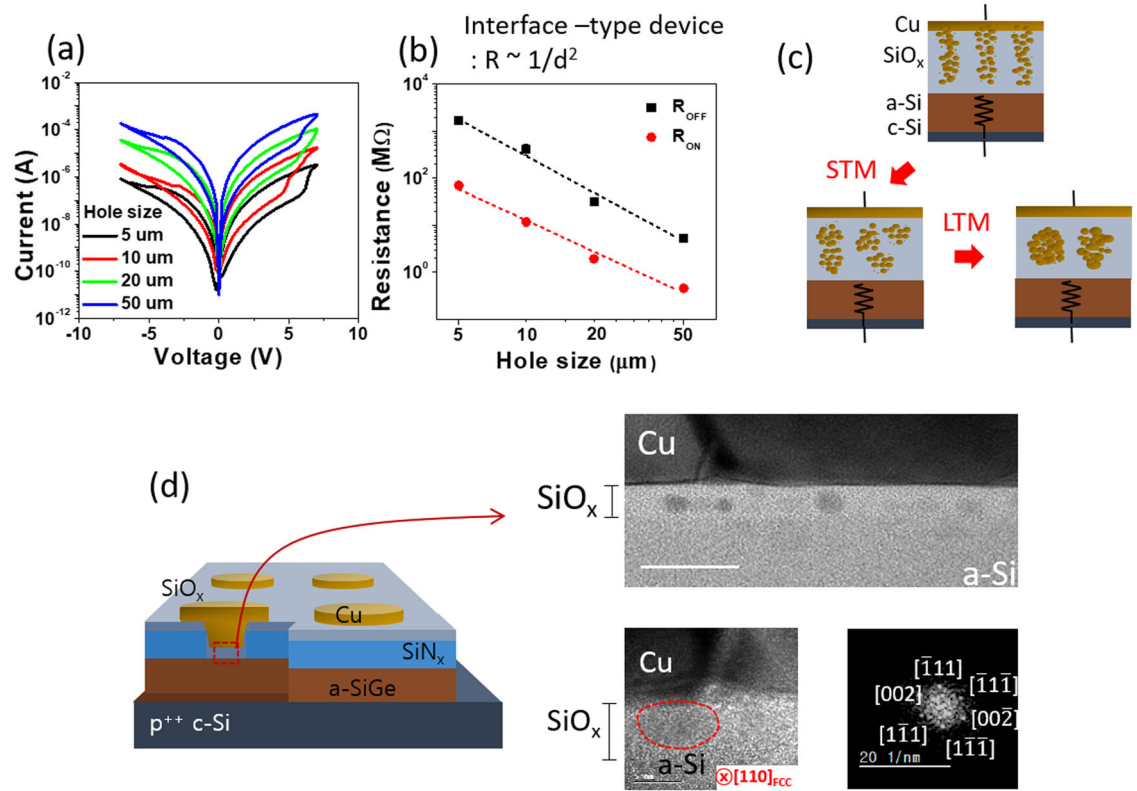
Fig. 8 Multi-filamentary swithing behaviors of the memristive devices. a Current–voltage characteristics of the HC Cu-based bilayer device, which vary with the via-hole size. **b** Via-hole size vs. resistance of the Cu-based bilayer device, where the resistance value was determined at 1 V. **c** Schematic diagram and cross-sectional view of the device, obtained through XTEM photos. FFT images were extracted from high-resolution TEM images to confirm that the shapes of the clusters were evenly distributed in the SiO_x layer. **d** Morphologies in which the device in the set state changes over time; STM and LTM refer to short time and long time, respectively.

where the exponents of the LRS and HRS states were 2.2 and 2.6, respectively[33]. The cell-size dependency of the device resistances with an exponent close to 2.0 supported that the Ge implanted devices operated as an interface type-like device. The XTEM images of the devices in the set state showed multiple nanoclusters in the switching layer, as observed in Fig. 8c. The nanoclusters were confirmed to be Cu from the lattice constants estimated from the HR-TEM image and the FFT image. The size of the Cu nanoclusters was uniformly distributed in the switching layer, and the interparticle distances were 3.9 nm and 2.6 nm on average, respectively. The Cu nanoclusters served as multiple conductive filaments or multi-weak filaments in the CBRAM devices. From the XTEM image, we could deduce the operation mechanism of the Ge-implanted devices. The schematics in Fig. 8d illustrate the formation of the multi-weak filaments. The STM and LTM forgetting behaviors observed in Fig. 7 could also be understood from the illustrations. When a positive voltage bias was applied to the Cu active electrode, a multi-weak filament was formed. Once the multi-weak filaments were formed and the applied bias was removed, the elongated Cu nanoclusters could shrink to be more spherical to reduce the surface energy. This shape change resulted in conductance decay in STM mode. In the later stage, the Cu nanoclusters became more spherical and retained their shape in the LTM mode. The abrupt switching was suppressed due to the resistive a-SiGe$_x$ underlayer inserted between SiO$_x$ and c-Si limiting abrupt current overshooting by a voltage dividing effect. The a-SiGe underlayer served as a current limiting layer. The resistance of the current limiting layer needed to be properly adjusted to obtain gradual switching behavior. In the reset mode, the voltage bias needed to be applied mainly to the switching layer, and in the set mode, the voltage needed to be divided into the switching layer and the current liming layer to suppress current overshooting. For this, the resistance of the current limiting layer was desirable to be in between the LRS and the HRS of the memristive devices. Otherwise, the current liming layer might not work properly. In this work, the resistance of the a-Si current limiting layer was modulated by implantation of the Ge ion, and gradual switching behavior with the current limiting layer of the HC conductance was successfully obtained. In addition to the voltage diving effect, other factors, such as heat confinement and suppressed field concentration, could help in multi-weak filament formations in the CBRAM devices with the SiGe underlayer. More detailed discussions are provided in the Supplementary information (Figs. S7, S8).

Conclusion

In this work, we proposed a novel scheme to implement memristive devices exhibiting the analog behavior required for neuromorphic computing hardware. A Cu active electrode was selected based on the switching layer and the type of active metal. To prevent the formation of Cu silicide at the SiO$_x$/c-Si interface, an a-Si underlayer was inserted as a buffer layer. Through this scheme, the device showed stable set and reset behaviors. In addition, the abrupt formation of the conductive filaments during the set switching operation was suppressed, resulting in gradual resistive switching due to the current limiting effect of the a-Si buffer layer. Analog characteristics were optimized by tuning the conductance through Ge ion implantation into the a-Si thin film. The formation of the conductive filaments was greatly suppressed when the resistance of the buffer layer was too large. Therefore, a properly tuned a-SiGe$_x$ thin film as a buffer layer was used and provided a relatively large R_{on}/R_{off} ratio while maintaining gradual switching. The analog synaptic characteristics of the Cu-based bilayer devices were confirmed by long-term potentiation and depression tests, and the nonlinearity parameters in synaptic potentiation and depression were extracted. MLP artificial neural network simulations for MNIST recognition were performed with consideration of the synapse nonlinearity of the memristor devices. In the case of the devices without the a-SiGe$_x$ underlayer, unstable switching behavior derived from the abrupt conductance change and Cu silicide formation was observed. However, the memristor devices with the a-SiGe$_x$ underlayer exhibited gradual analog switching and provided improved learning accuracy, especially with an increasing number of conductance states, approaching a value close to 90%.

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I.K. proposed the project. K.K. and J.G.L. performed the experiments. S.M.H., Y.J., J.P., J.K., S.P. performed the neural network simulations. S.L., J.Y.K., J.P. contributed to the data analysis. G.W.H., K.S.L., and W.S.L. contributed to the material characterizations. K.K., I.K., J.P. wrote the manuscript with input from all other authors. B.K.J. reviewed the manuscript.

Competing interests
The authors declare no competing interests.

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