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Positive-to-negative subthreshold swing of a MOSFET tuned by the ferroelectric switching dynamics of $BiFeO_3$

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Abstract

Ferroelectricity can reduce the subthreshold swing (*SS*) of metal-oxide-semiconductor field-effect transistors (MOSFETs) to below the room-temperature Boltzmann limit of ~60 mV/dec and provides an important strategy to achieve a steeper *SS*. Surprisingly, by carefully tuning the polarization switching dynamics of $BiFeO_3$ ferroelectric capacitors the *SS* of a commercial power MOSFET can even be tuned to zero or a negative value, i.e., the drain current increases with a constant or decreasing gate voltage. In particular, in addition to the positive *SS* of lower than 60 mV/dec, the zero and negative *SS* can be established with a drain current spanning for over seven orders of magnitude. These intriguing phenomena are explained by the ferroelectric polarization switching dynamics, which change the charge redistributions and accordingly affect the voltage drops across the ferroelectric capacitor and MOSFET. This study provides deep insights into understanding the steep *SS* in ferroelectric MOSFETs, which could be promising for designing advanced MOSFETs with an ultralow and tunable *SS*.

Introduction

Ferroelectric materials show high potential for use in various applications, such as nonvolatile memories[1–4], photoelectric detectors[5–8], and neuromorphic computing[9,10]. Recently, it was reported that ferroelectricity can be used to reduce the subthreshold swing (*SS*) of metal-oxide-semiconductor field-effect transistors (MOSFETs) to below 60 mV/dec at room temperature and break the "Boltzmann Tyranny", which may be beneficial to lowering power consumption[11–14]. For instance, *SS* values less than 60 mV/dec have been achieved, such as in $MoS_2/Al_2O_3/Hf_{0.5}Zr_{0.5}O_2$-based[14], $MoS_2/HfO_2/LiNbO_3$-based[15], and $PbZr_{1-x}Ti_xO_3$-based[16] ferroelectric MOSFETs.

To understand the important effect of reducing the *SS*, several explanations have been proposed from different aspects. One is based on the concept of a negative capacitance effect, i.e., the ferroelectric material can serve as a negative capacitor[17,18]. This is related to the double-well landscape of the free energy in a ferroelectric material, which inevitably leads to a region of negative capacitance when ferroelectricity switches from one polarization state to the other[19–22]. As a result, with a ferroelectric negative capacitor connected to the gate terminal, the channel surface potential of a MOSFET can be amplified to be even higher than the gate potential under capacitance matching conditions[12,17]. Hence, the ferroelectric MOSFET can be operated with an $SS < 60$ mV/dec at room temperature[11,12,14]. In addition to the steep *SS*, many distinctive phenomena, including a voltage drop across the ferroelectric capacitor with charges flowing, an "S"-shaped relation between polarization (*P*) and voltage (*V*), and a stepup conversion of internal voltage, have been reported by using various ferroelectric materials, and these effects

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can also be attributed to the negative capacitance[22–26]. On the other hand, some researchers found that it may not be necessary to introduce the concept of negative capacitance and proposed that an *SS* less than 60 mV/dec is related to the ferroelectric polarization reversal characteristics[16,27,28]. For example, as reported by Hwang et al., the voltage drop with flowing charges and the "S"-shaped *P-V* curve can be explained by a reversing ferroelectric domain, of which the charge effect cannot be fully compensated by the supplied charges from the external charge source[27]. Very recently, Li et al. observed stepwise jumps in the internal potential of a metal/ferroelectric/metal/paraelectric/metal-stacked system near the coercive voltage of the ferroelectric layer; furthermore, they experimentally confirmed the relationship of these jumps with the steep *SS* of the MOSFET. On this basis, a concise model was raised from the aspect of successive polarized domain flipping and depolarization feedbacks[16,28].

Regardless of whether the steep *SS* is due to the negative capacitance, at least ferroelectric polarization reversal can reduce the *SS* of a ferroelectric MOSFET. Considering that the ferroelectric switching dynamics can be controlled by voltage sweeping processes, it will be very interesting to investigate the tunability of *SS* and the corresponding dynamic characteristics in ferroelectric MOSFET devices. Not only can we obtain insights into the ferroelectric polarization switching dynamics affecting the *SS*, but an ultralow and tunable *SS* in MOSFETs may also be achieved, which is important for designing advanced electronic devices.

In principle, a ferroelectric material with a large polarization and controllable ferroelectric switching dynamics will be a good candidate for tuning the *SS* of ferroelectric MOSFETs. According to our previous studies[29,30], $BiFeO_3$ films (BFO) have a large polarization (>60 μC/cm^2)[31–33] and relatively clear ferroelectric switching dynamics. Therefore, in this work, we use an Au/BFO/$La_{0.6}Sr_{0.4}MnO_3$ (LSMO) ferroelectric capacitor connected in series with a commercial power MOSFET to tune its *SS* by varying the voltage sweeping sequences. Notably, the *SS* can be tuned to below 60 mV/dec at room temperature. In particular, an $SS = 0$ and even a negative *SS* can be realized with a drain current spanning over seven orders of magnitude. These results are highly related to the ferroelectric polarization switching dynamics, which redistribute the charges and accordingly affect the voltage drops across the ferroelectric capacitor and MOSFET.

Materials and methods

Sample preparation

The LSMO layer was grown on a (001)-oriented $SrTiO_3$ (STO) single-crystal substrate using a DC magnetron sputtering technique with a power of 40 W, a deposition temperature of 750 °C and an argon/oxygen (1:1) pressure of 4 Pa. For the BFO ferroelectric layer, an RF magnetron sputtering technique was used with a power of 40 W, a deposition temperature of 680 °C and an argon/oxygen (1:1) pressure of 4 Pa. After deposition, the heterostructure was slowly cooled at a rate of 5 °C/min to 250 °C under 10 Pa of oxygen pressure and then naturally cooled to room temperature. The top Au electrodes (300 μm in diameter) were deposited with a shadow mask.

Characterization

The film thicknesses were measured by cross-sectional scanning electron microscopy (SEM) (SU8200, Hitachi, Japan). The heterostructures were characterized by X-ray diffraction (XRD) using a Cu Kα1 radiation source (λ = 1.540598 Å) (X'Pert Pro diffractometer, Philips Analytical, Netherlands) as well as with high-angle annular dark field scanning transmission electron microscopy (HAADF-STEM) (JEM-ARM200F, JEOL, Japan). The surface morphology was investigated by atomic force microscopy (AFM) (MFP-3D, Asylum Research, USA). The ferroelectric characteristics were investigated by a ferroelectric tester (Precision Premier II, Radiant Technologies, USA). The transport measurements of the ferroelectric MOSFETs were obtained with a semiconductor parameter analyzer (4200A-SCS, Keithley, USA).

Results and discussion

Structural and ferroelectric characterization

Figure 1a shows the XRD pattern of the BFO (~200 nm)/LSMO (~50 nm) heterostructure grown on an STO single-crystal substrate (see Supplementary Fig. S1a) through a magnetron sputtering technique. Only (00 *l*) diffraction peaks appear, demonstrating the epitaxial nature of the rhombohedral-like BFO and LSMO layers grown on the (001)-oriented STO substrate[34]. Due to bulk BFO (~3.96 Å) having a larger in-plane lattice parameter than STO (~3.905 Å) and LSMO (~3.87 Å)[35–37], the BFO film demonstrates an in-plane compressive strain from the lattice mismatch. Thus, the out-of-plane lattice parameter of the BFO film (~4.01 Å, as determined from the XRD data), is larger than that of bulk BFO (~3.96 Å)[35]. The AFM results show that the material has a smooth surface with a small root mean square roughness of ~0.67 nm (see Supplementary Fig. S1b). Figure 1b shows the cross-sectional HAADF-STEM image. As the magnified image depicted in the inset of Fig. 1b, the visible ferroelectric displacements of the Fe ions projected along the [001] and [010] directions are ~20.4 pm and ~17.6 pm, respectively.

The ferroelectricity of BFO is also confirmed by the *P-V* hysteresis loops, as presented in Fig. 1c. The polarization of the BFO ferroelectric capacitor is ~60 μC/cm^2, which is consistent with previous reports[6,31]. With an increasing measuring frequency, the ferroelectric coercive voltage

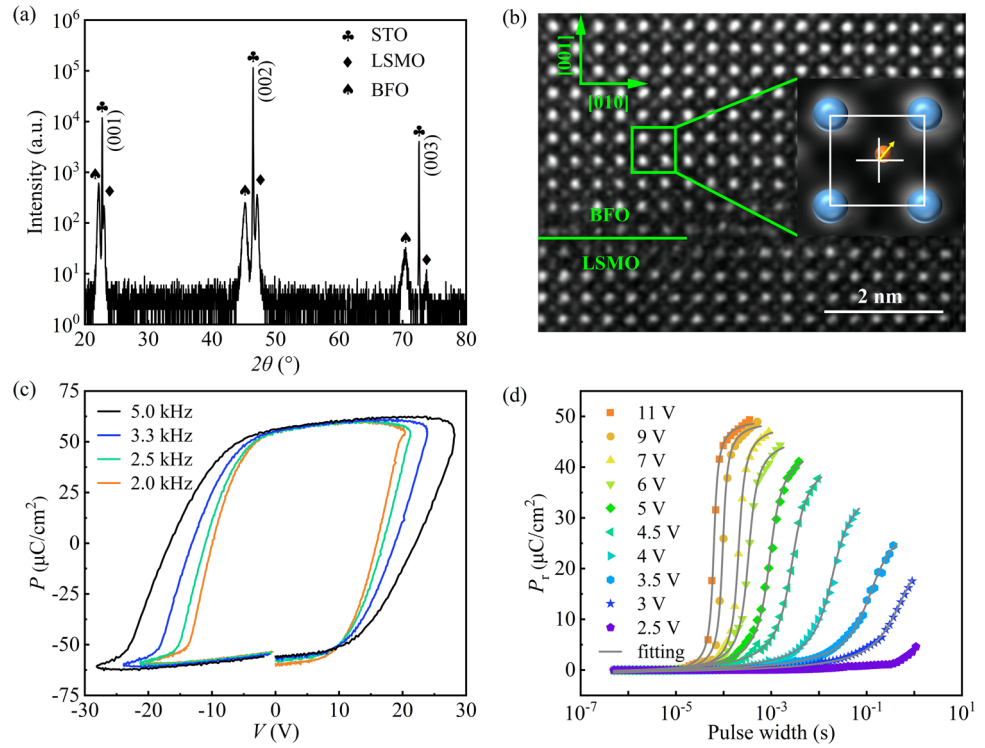

Fig. 1 Structural and ferroelectric characterizations. a XRD pattern of the BFO (~200 nm)/LSMO (~50 nm) heterostructure grown on an STO (001) substrate. **b** HAADF-STEM image of the BFO/LSMO interface. The inset shows the Fe-ion displacement in BFO, and the blue and orange spheres denote the Bi and Fe ions, respectively. **c** *P-V* loops measured at different frequencies. **d** Remnant polarization *vs.* voltage pulse width at different voltages. The solid lines are the fitting results by a nucleation-limited-switching model.

increases. This is essentially related to the kinetics of ferroelectric switching that at a higher frequency (i.e., with a shorter time for ferroelectric reversal), a larger voltage is needed to switch the polarization[38,39]. Then, the ferroelectric polarization switching dynamics were investigated using the positive-up-negative-down (PUND) polarization measurement mode[29,30] (see the details in Supplementary Fig. S2a), as shown in Fig. 1d. Here, the evolution of the ferroelectric up-to-down polarization switching in regard to the pulse width was tested at various voltage amplitudes. As expected, to achieve the same amount of ferroelectric polarization reversal, a longer pulse width is required for a lower pulse voltage[3,40,41]. In addition, a nucleation-limited-switching (NLS) model (see Supplementary Fig. S2b–d) can be used to describe the ferroelectric switching dynamics in Fig. 1d, as indicated by the solid lines[3,40,41]. Finally, the activation electric field of ~0.20 V/nm for ferroelectric switching is similar to that in an earlier report[29].

Ultralow *SS* of a MOSFET in series with a BFO ferroelectric capacitor

To investigate the ferroelectric polarization reversal-affected transfer characteristics of a MOSFET, a BFO ferroelectric capacitor was connected in series with the gate terminal of a commercial power MOSFET, as schematically presented in Fig. 2a. The gate voltage V_G was applied to the top Au electrode of the BFO ferroelectric capacitor, and a drain voltage V_{DS} of ~10 V was applied to the drain terminal of the MOSFET. The internal voltage V_{int} at the gate terminal of the MOSFET was measured. By sweeping V_G from −5 to +10 V (forward) and then back to −5 V (reverse) with a step of 0.5 mV, the drain current I_{DS} vs. V_G curves of the MOSFET with and without a connected BFO capacitor were tested, as illustrated in Fig. 2b. Regarding the standalone MOSFET, I_{DS} switches between the OFF and ON states when V_G changes between 1.4 and 4.0 V. In contrast, with the ferroelectric capacitor connected, the drain current I_{DS} switches more abruptly from the OFF to the ON state (V_G changes from 4.8 to 4.9 V) and from the ON to the OFF state (V_G changes from −1 to −1.05 V) in the switching regions. Here, the drain current of the ferroelectric MOSFET is very small in the OFF state, which is comparable with that of the standalone MOSFET. There is a small dip in I_{DS} in the reverse voltage sweep in the OFF state, similar to earlier reports[42–44], which may be related to the ferroelectric switching current. In addition, it is

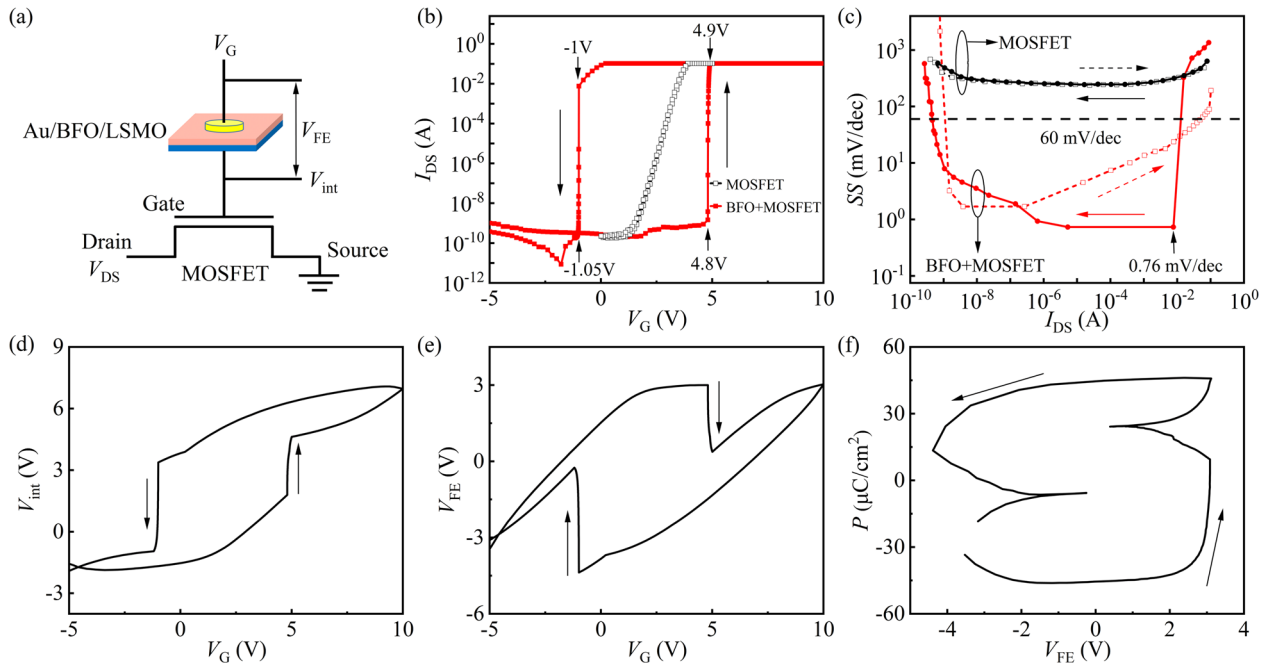

Fig. 2 Ultralow *SS* of a MOSFET in series with a 200 nm-thick BFO ferroelectric capacitor. a Schematic illustration of the BFO ferroelectric capacitor in series with the gate terminal of a commercial power MOSFET. **b** I_{DS} vs. V_G curves and **c** *SS* vs. I_{DS} curves of the MOSFET with and without a connected BFO capacitor. **d** V_{int} vs. V_G curve and **e** corresponding V_{FE} vs. V_G curve. **f** *P*-V_{FE} loop of the BFO ferroelectric capacitor under the voltage waveform of V_{FE} in **e**. The arrows indicate the sweep directions.

noted that the I_{DS}–V_G curve does not overlap for the forward and reverse voltage sweeps. This is because a certain voltage is needed to switch the ferroelectric polarization (see Fig. 1c, d), especially for the rather thick (~200 nm) BFO ferroelectric film. In fact, the voltage hysteresis can be reduced by using a thinner ferroelectric film[42,45], as demonstrated by the ferroelectric MOSFET based on a thinner ~150 nm-thick BFO film in Supplementary Figs. S3–S6.

The steepness of switching from the OFF to the ON state or the ON to the OFF state in the I_{DS} vs. V_G curves in Fig. 2b can be quantified by the subthreshold swing, *SS*, which is defined as the change in V_G required to tune the I_{DS} by an order of magnitude[12,17]:

$$SS = \frac{\partial V_G}{\partial \log_{10} I_{DS}}. \quad (1)$$

As shown in Fig. 2c, the calculated *SS* of the standalone MOSFET is ~260 mV/dec for over seven orders of magnitude of I_{DS}. With the BFO capacitor connected, the *SS* of the MOSFET in the series system is greatly reduced in the switching regions. The minimum *SS* values are as low as ~1.69 mV/dec and ~0.76 mV/dec for the forward and reverse voltage sweeps, respectively. This record-low *SS* (thus far) obtained by using a common sweeping voltage measurement mode[14,15] is well below the room-temperature Boltzmann thermodynamics limit of ~60 mV/dec. With the reduced *SS*, the power consumption for turning on the BFO capacitor-connected MOSFET is lower than that of the standalone MOSFET (Supplementary S4, Table S1). To understand the ultralow *SS* in the series circuit, the V_{int} at the gate terminal of the MOSFET was directly measured, as shown in Fig. 2d. Clearly, the internal voltage gains $dV_{int}/dV_G > 1$ in the switching regions experimentally demonstrate voltage amplification (i.e., the internal voltage amplification effect[25,46–48]), as shown in Supplementary Fig. S7. As a consequence, owing to the amplified V_{int}, a steeper *SS* than that of a standalone MOSFET is established[25,46–48].

To investigate the effect of polarization switching on the *SS*, the voltage V_{FE} across the BFO ferroelectric capacitor was calculated by:

$$V_{FE} = V_G - V_{int}. \quad (2)$$

The result is shown in Fig. 2e. Clearly, for both the forward and reverse sweeps, the absolute amplitude of V_{FE} first increases to a high voltage level and then decreases sharply around the switching points at V_G values of ~4.8 V and −1.0 V and then increases back again with a further increase in V_G to the positive and negative maximums. Considering the series circuit containing the BFO ferroelectric capacitor and MOSFET, the sudden

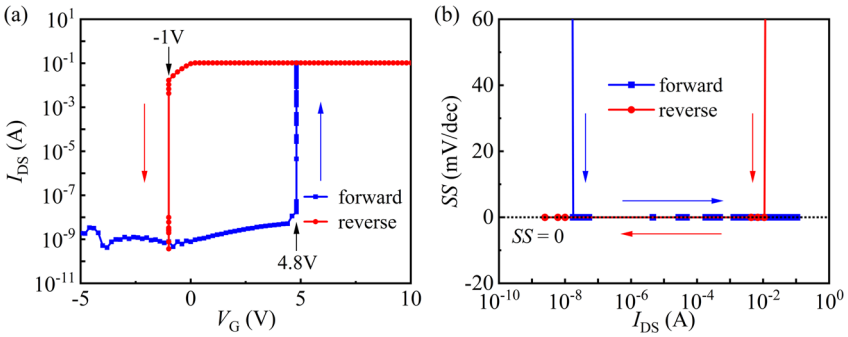

Fig. 3 Zero *SS* with a fixed V_G at the switching points. a I_{DS} vs. V_G curve of the MOSFET connected in series with the 200 nm-thick BFO capacitor with V_G unchanged at the switching points and the **b** corresponding *SS* vs. I_{DS} curve. $SS = 0$ is obtained for six orders of magnitude of the I_{DS} of both the forward and reverse branches. The arrows indicate the sweep directions.

variations in V_{int} and V_{FE} at the switching points can be understood based on ferroelectric switching-induced charge redistributions[16,49]. During the forward branch measurement, the ferroelectric polarization up-to-down switching around a V_G value of ~4.8 V requires more negative screening charges at the bottom electrode of the ferroelectric capacitor, which come from the gate terminal of the MOSFET. This charge redistribution will result in more positive charge accumulation at the gate terminal of the MOSFET, thus leading to an increase in V_{int} and a drop in V_{FE}. Similarly, an abrupt drop in V_{int} and an increase in V_{FE} can be observed around a V_G value of ~−1.0 V when the ferroelectric polarization switches from down to up. Consequently, the stepup conversion of V_{int} and the corresponding reduction of *SS* can be understood in terms of charge redistributions mediated by ferroelectric switching. It should be noted that the amplified V_{int} and reduced *SS* in the ferroelectric MOSFETs may also be explained in terms of the negative capacitance effect[19–22], as discussed in Supplementary S6. The underlying mechanism of the reduced *SS* and amplified V_{int} by ferroelectric switching has drawn considerable interest from both experimental and theoretical researchers[12,16,50–52], and further in-depth investigations are necessary to reveal its comprehensive physical process. Other mechanisms for the reduction of the *SS*, such as filament forming/rupture in BFO[53], can be excluded in our work. If filament forming/rupture[53] occurs in BFO, an amplified V_{int} and reduced *SS* will appear as a result. However, if the conducting filament forms in a ferroelectric layer, the ferroelectric polarization can hardly be reversed because of the conductive filaments connecting both electrodes[54,55]. Regarding our ferroelectric MOSFET, the ferroelectric hysteresis of the BFO capacitor can still be measured after the characterization of the steep *SS*.

The sudden drop in V_{FE} at the switching points suggests the famous "S"-shaped *P-V* loop of the ferroelectric capacitor. By directly applying the voltage waveform of V_{FE} in Fig. 2e to the standalone BFO ferroelectric capacitor through a ferroelectric analyzer, the "S"-shaped-like P-V_{FE} loop can be experimentally obtained (Fig. 2f), which is similar to the experimental results in the literature[26,56,57]. This corresponds to the real-time ferroelectric domain switching process during the measurement of the I_{DS} vs. V_G curves. As the V_{FE} is close to the coercive voltage, the polarization begins switching, and as long as polarization switching occurs, even when V_{FE} decreases in certain switching regions, *P* keeps increasing, possibly because less energy is needed for further switching[58]. In addition, the measured P-V_{FE} loop in Fig. 2f shows that the maximum V_{FE} values on the positive and negative voltage sides are ~3.0 and ~−4.4 V, respectively. Because the *SS* in MOSFETs can be efficiently tuned by ferroelectric polarization switching dynamics, the forward and reverse voltage sweeps demonstrate different polarization switching processes (see Fig. 1d and Supplementary Fig. S2), resulting in the different *SS* values in Fig. 2c.

Zero *SS* and dynamic characteristics of the ferroelectric MOSFET

By tuning the sweeping process of V_G to control the ferroelectric polarization switching dynamics, even sharper ramping of I_{DS} can be achieved, as shown in Fig. 3. According to the ferroelectric switching dynamics in Fig. 1d, the polarization can be continuously switched with an increasing pulse width of the applied voltage. Thus, by sweeping V_G to 4.8 V or −1 V and then fixing V_G at the switching point of the forward or reverse branch (see the waveforms of V_G in Supplementary Fig. S8a), I_{DS} keeps changing until it reaches the ON or the OFF state, as shown in Fig. 3a. Figure 3b indicates the corresponding relationship between the *SS* and I_{DS}, and a record-low *SS* down to zero is obtained for over six orders of magnitude of the I_{DS} of both the forward and reverse branches.

To further understand the ferroelectric polarization switching dynamics affecting the I_{DS} vs. V_G curves with an

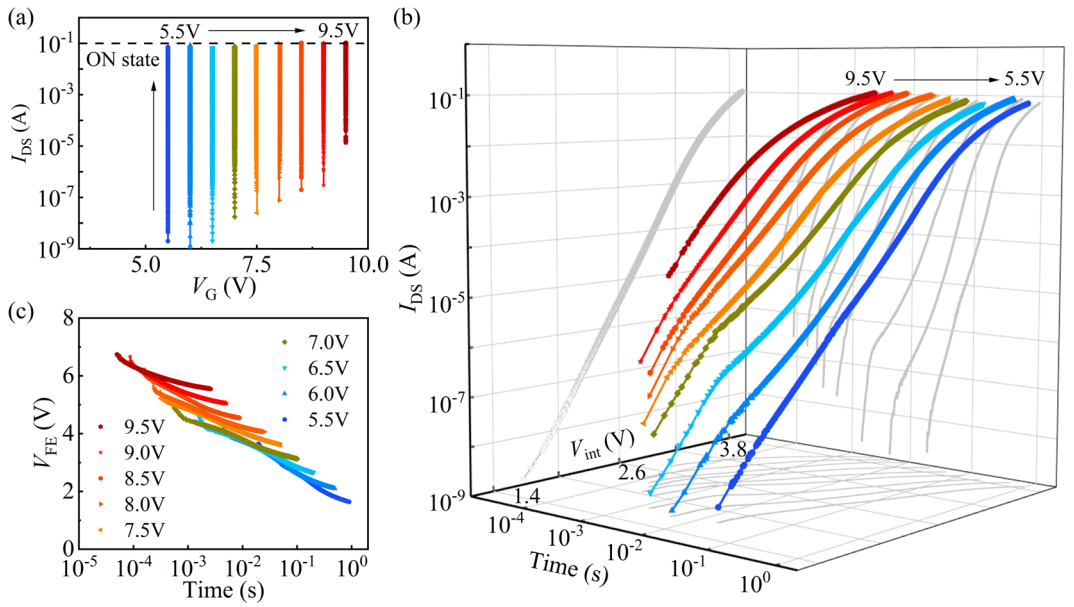

Fig. 4 Dynamic characteristics of the ferroelectric MOSFET. a I_{DS} vs. V_G curves at various constant V_G amplitudes. $SS = 0$ is obtained for seven orders of magnitude of I_{DS}. **b** Three-dimensional diagram of the MOSFET with the 200 nm-thick BFO capacitor connected for V_{int}, time, and I_{DS} and the projections onto the I_{DS}-V_{int}, I_{DS}-time, and V_{int}-time planes. **c** Evolution of V_{FE} over time at various constant V_G amplitudes.

$SS = 0$, the I_{DS} switching dynamics of the MOSFET with a connected BFO capacitor were investigated by applying square voltage waveforms of V_G (schematically shown in Supplementary Fig. S8b) with different amplitudes, as displayed in Fig. 4. Before each measurement, the BFO capacitor was initialized to the up state. Through the application of a different pulsed V_G from 5.5 to 9.5 V, I_{DS} increases gradually from the OFF state to the ON state, as shown in Fig. 4a, and an $SS = 0$ is established for over seven orders of magnitude of I_{DS}. Figure 4b shows the relationship among the I_{DS}, V_{int} and time windows from the OFF state to the ON state. Clearly, with increasing V_G, the I_{DS} changes more quickly from the OFF to the ON state, similar to the BFO ferroelectric switching dynamics in Fig. 1d, which show that at higher voltages, ferroelectric polarization switches more quickly from the up to the down state. By applying a V_G as high as 40 V, the ferroelectric MOSFET starts to turn ON with a time delay of 525 ns (see Supplementary Figs. S9-S10), which is longer than that of the standalone MOSFET[59]; this result is similar to earlier reports[60,61]. These results imply that there is a close relation between the ramping of I_{DS} with an $SS = 0$ and the ferroelectric polarization switching dynamics.

Furthermore, the evolution of V_{FE} calculated by using Eq. (2) is displayed in Fig. 4c. It is found that when a certain V_G is applied, V_{FE} decreases gradually as the applied V_G increases. This can be due to continuous ferroelectric polarization switching, which leads to more charge accumulation on the MOSFET and results in an increase in V_{int} and a decrease in V_{FE} over time. It is worth mentioning that the evolution trend of V_{FE} with a constant V_G in BFO-based MOSFETs is different from that of the ferroelectric capacitor in series with a resistor (another classic circuit for investigating the ferroelectric negative capacitance effect). Regarding a system with a resistor-connected circuit, the V_{FE} decreases first over time and then increases back to $\sim V_G$. In other words, the stepup conversion of V_{int} ($=V_G - V_{FE}$) disappears after ferroelectric switching finishes[23,56,62]. Regarding the system with a MOSFET (comparable to a capacitor) connected with a ferroelectric capacitor, the ferroelectricity-tuned *SS* of the MOSFET can be revealed, and the V_{FE} does not recover after ferroelectric switching is finished. Although the phenomena in both systems are different, the underlying mechanisms for the decreasing V_{FE} are consistently linked with ferroelectric switching. Different from the resistor, the gate of the MOSFET (or capacitor) will accumulate charges that will not disappear when ferroelectric switching finishes; thus, V_{int} across the gate of the MOSFET remains even when V_{FE} does not increase back to $\sim V_G$.

Negative *SS* tuned by the ferroelectric switching dynamics

From the above results, it can be seen that by varying V_G, the *SS* can be tuned to zero. In fact, by further manipulating the V_G waveform by sweeping V_G back by a small voltage V_{return} when the V_G is close to the switching points (see the waveform of V_G in Supplementary Fig. S5a), the *SS* can even be tuned to be negative, as shown in

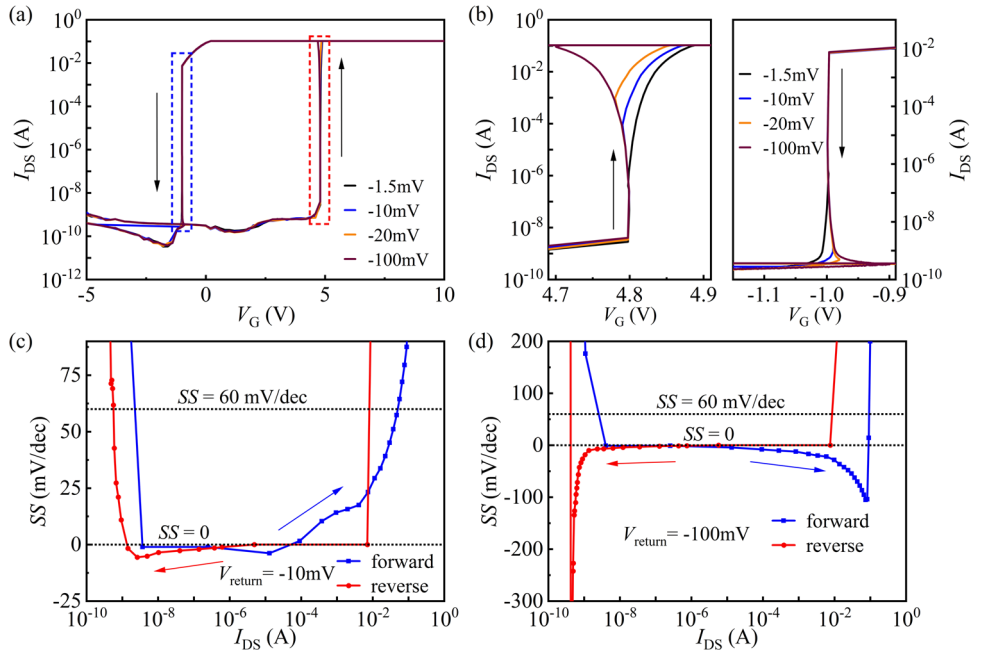

Fig. 5 Negative *SS* of the ferroelectric MOSFET tuned by the ferroelectric switching dynamics of the 200 nm-thick BFO capacitor. a I_{DS} vs. V_G curves with manipulated voltage waveforms. **b** Magnified images of the region in the red and blue dashed-lined boxes in **a**. **c** *SS* vs. I_{DS} curve for $V_{return} = -10$ mV. A positive *SS* well below 60 mV/dec (over three orders of magnitude of I_{DS}) to a negative *SS* (over three orders of magnitude of I_{DS}) is observed. **d** *SS* vs. I_{DS} curve for $V_{return} = -100$ mV. A negative *SS* for over seven orders of magnitude of I_{DS} is obtained. The arrows indicate the sweep directions.

Fig. 5a, b. Figure 5c plots the *SS vs.* I_{DS} curves with $V_{return} = -10$ mV. Surprisingly, although V_G drops in the region of V_{return}, I_{DS} still increases because of the ongoing ferroelectric domain reversal; thus, a negative *SS* occurs for over three orders of magnitude of the I_{DS} of both the forward and reverse branches, as shown in Fig. 5c. It should be noted that a negative *SS* can even be obtained for over seven orders of magnitude of I_{DS} when V_{return} is ~ −100 mV, as shown in Fig. 5d. The discovered negative *SS* in the MOSFETs, which corresponds to the decrease in gate voltage with the increase in internal voltage, provides an interesting method for tuning the drain current of the MOSFET and reduces the gate power consumption; this method may be helpful for understanding the working principles of ferroelectric MOSFETs.

The tunable and even negative *SS* obtained by setting V_{return}, as shown in Fig. 5 and Supplementary Fig. S11, can be understood based on the "S"-shaped *P*-V_{FE} curve observed in Fig. 2f; for example, when V_{FE} decreases in certain switching regions, *P* keeps increasing. This is because even with V_{return}, V_{FE} is still large enough to trigger further ferroelectric switching. Consequently, a polarization reversal-induced ramping of I_{DS} still occurs within the V_{return} region, and a negative *SS* is achieved as a result. The tunable, ultralow, and even negative *SS* not only enhances the functionality and performance of ferroelectric MOSFETs but also demonstrates the importance of the ferroelectric domain switching dynamics in explaining all the distinctive phenomena that was observed.

Here, a single-crystalline epitaxial BFO film with a large polarization of ~60 μC/cm^2 was used to investigate the principle of manipulating the *SS* by ferroelectric switching. Based on this principle, other ferroelectric materials with smaller polarizations, such as $Hf_{1-x}Zr_xO_2$ (~30 μC/cm^2)[14,63] and $BaTiO_3$ (~25 μC/cm^2)[64], could also be used to tune the *SS* of MOSFETs from positive to negative. Other ferroelectric field-effect transistors based on nanowire FETs, FinFETs, would have similar behavior to the zero or negative *SS* by tuning the switching dynamics of the ferroelectric materials. In addition, it is worth mentioning that the compatibility of ferroelectric materials with Si substrates is important for their practical application. According to earlier reports[65–67], a single-crystalline epitaxial BFO film with a polarization of ~45 μC/cm^2 can be obtained by using single-crystalline Si substrates. Recently, the use of Si substrates for growing $Hf_{1-x}Zr_xO_2$ offers a very important advantage to be more compatible with current CMOS processes than using a $SrTiO_3$ substrate, although realizing a single-phase $Hf_{1-x}Zr_xO_2$ ferroelectric film is still challenging[68–70]. Therefore, further detailed and systematic investigations are necessary for practically applicable devices.

Conclusion

In summary, by connecting a Au/BFO/LSMO ferroelectric capacitor with the gate terminal of a commercial power MOSFET, the *SS* can be flexibly tuned by manipulating the ferroelectric polarization switching process. In addition to a positive *SS* of lower than 60 mV/dec, an $SS = 0$ and even a negative *SS* can be obtained for over seven orders of magnitude of the drain current. The results are closely related to the ferroelectric polarization switching dynamics, which affect the charge redistributions and accordingly decrease (increase) the voltage drop on the ferroelectric capacitor (MOSFET). Our work is helpful to understand the steep and tunable *SS* in ferroelectric MOSFETs and provides a possible strategy to further improve the performance of MOSFET devices by designing ferroelectric switching dynamics.

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Author contributions

C.C.L. prepared the samples and performed the measurements. Y.C.W. prepared a thinner ~150 nm-thick BFO film and measured the properties of the corresponding ferroelectric MOSFET. H.Y.S. and Z.L. performed the ferroelectric domain dynamics and the corresponding fittings. C.M. analyzed the HAADF-STEM result. Z.L. conducted the AFM measurements. H.W. performed the XRD and SEM measurements. X.G.L. and Y.W.Y. designed and supervised the experiments. All the authors contributed to the refinement of the manuscript.

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Conflict of interest

The authors declare no competing interests.

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References

1. Khan, A. I., Keshavarzi, A. & Datta, S. The future of ferroelectric field-effect transistor technology. *Nat. Electron.* **3**, 588–597 (2020).
2. Jiang, A. Q. & Zhang, Y. Next-generation ferroelectric domain-wall memories: principle and architecture. *NPG Asia Mater.* **11**, 2 (2019).
3. Ma, C. et al. Sub-nanosecond memristor based on ferroelectric tunnel junction. *Nat. Commun.* **11**, 1439 (2020).
4. Wang, Z. R. et al. Resistive switching materials for information processing. *Nat. Rev. Mater.* **5**, 173–195 (2020).
5. Zheng, M., Sun, H. L. & Kwok, K. W. Mechanically controlled reversible photoluminescence response in all-inorganic flexible transparent ferroelectric/mica heterostructures. *NPG Asia Mater.* **11**, 52 (2019).
6. You, L. et al. Enhancing ferroelectric photovoltaic effect by polar order engineering. *Sci. Adv.* **4**, eaat3438 (2018).
7. Chakrabartty, J., Harnagea, C., Celikin, M., Rosei, F. & Nechache, R. Improved photovoltaic performance from inorganic perovskite oxide thin films with mixed crystal phases. *Nat. Photonics* **12**, 271–276 (2018).
8. Tan, Z. W. et al. Thinning ferroelectric films for high-efficiency photovoltaics based on the Schottky barrier effect. *NPG Asia Mater.* **11**, 20 (2019).
9. Berdan, R. et al. Low-power linear computation using nonlinear ferroelectric tunnel junction memristors. *Nat. Electron.* **3**, 259–266 (2020).
10. Li, J. K. et al. Reproducible ultrathin ferroelectric domain switching for high-performance neuromorphic computing. *Adv. Mater.* **32**, 1905764 (2020).
11. Salahuddin, S. & Datta, S. Use of negative capacitance to provide voltage amplification for low power nanoscale devices. *Nano Lett.* **8**, 405–410 (2008).
12. Íñiguez, J., Zubko, P., Luk'yanchuk, I. & Cano, A. Ferroelectric negative capacitance. *Nat. Rev. Mater.* **4**, 243–256 (2019).
13. Krivokapic, Z. et al. 14nm ferroelectric FinFET technology with steep subthreshold slope for ultra low power applications. In *2017 IEEE International Electron Devices Meeting (IEDM)* 15.1.1–15.1.4 (IEEE, 2017).
14. Si, M. W. et al. Steep-slope hysteresis-free negative capacitance MoS_2 transistors. *Nat. Nanotechnol.* **13**, 24–28 (2018).
15. Wang, Y. et al. Record-low subthreshold-swing negative-capacitance 2D field-effect transistors. *Adv. Mater.* **32**, 2005353 (2020).
16. Li, X. Y. & Toriumi, A. Stepwise internal potential jumps caused by multiple-domain polarization flips in metal/ferroelectric/metal/paraelectric/metal stack. *Nat. Commun.* **11**, 1895 (2020).
17. Tu, L. Q., Wang, X. D., Wang, J. L., Meng, X. J. & Chu, J. H. Ferroelectric negative capacitance field effect transistor. *Adv. Electron. Mater.* **4**, 1800231 (2018).
18. Alam, M. A., Si, M. W. & Ye, P. D. A critical review of recent progress on negative capacitance field-effect transistors. *Appl. Phys. Lett.* **114**, 090401 (2019).
19. Zubko, P. et al. Negative capacitance in multidomain ferroelectric superlattices. *Nature* **534**, 524–528 (2016).
20. Yadav, A. K. et al. Spatially resolved steady-state negative capacitance. *Nature* **565**, 468–471 (2019).
21. Khan, A. I. et al. Differential voltage amplification from ferroelectric negative capacitance. *Appl. Phys. Lett.* **111**, 253501 (2017).
22. Hoffmann, M. et al. Unveiling the double-well energy landscape in a ferroelectric layer. *Nature* **565**, 464–467 (2019).
23. Khan, A. I. et al. Negative capacitance in a ferroelectric capacitor. *Nat. Mater.* **14**, 182–186 (2015).
24. Saeidi, A. et al. Nanowire tunnel FET with simultaneously reduced subthermionic subthreshold swing and off-current due to negative capacitance and voltage pinning effects. *Nano Lett.* **20**, 3255–3262 (2020).
25. Jo, J. et al. Negative capacitance in organic/ferroelectric capacitor to implement steep switching MOS devices. *Nano Lett.* **15**, 4553–4556 (2015).
26. Wang, H. M. et al. New insights into the physical origin of negative capacitance and hysteresis in NCFETs. In *2018 IEEE International Electron Devices Meeting (IEDM)* 31.1.1–31.1.4 (IEEE, 2018).
27. Kim, Y. J. et al. Voltage drop in a ferroelectric single layer capacitor by retarded domain nucleation. *Nano Lett.* **17**, 7796–7802 (2017).
28. Li, X. Y. & Toriumi, A. Direct relationship between sub-60 mV dec subthreshold swing and internal potential instability in MOSFET externally connected to ferroelectric capacitor. In *2018 IEEE International Electron Devices Meeting (IEDM)* 31.3.1–31.3.4 (IEEE, 2018).
29. Huang, W. C. et al. Ferroelectric domain switching dynamics and memristive behaviors in $BiFeO_3$-based magnetoelectric heterojunctions. *J. Phys. D Appl. Phys.* **51**, 234005 (2018).
30. Sun, H. Y. et al. $BiFeO_3$-based flexible ferroelectric memristors for neuromorphic pattern recognition. ACS Appl. Electron. *ACS Appl. Electron Mater* **2**, 1081–1089 (2020).
31. Liu, Y. K., Yao, Y. P., Dong, S. N., Yang, S. W. & Li, X. G. Effect of magnetic field on ferroelectric properties of BiFeO3/La5/8Ca3/8MnO3 epitaxial heterostructures. *Phys. Rev. B* **86**, 075113 (2012).

32. Zhang, J. X. et al. Microscopic origin of the giant ferroelectric polarization in tetragonal-like $BiFeO_3$. *Phys. Rev. Lett.* **107**, 147602 (2011).
33. Kan, D., Anbusathaiah, V. & Takeuchi, I. Chemical substitution-induced ferroelectric polarization rotation in $BiFeO_3$. *Adv. Mater.* **23**, 1765–1769 (2011).
34. Liu, C. C. et al. Nonvolatile ZnO-based ferroelectric field effect transistors for active-matrix organic light-emitting diode display. *IEEE Electron Device Lett.* **41**, 42–45 (2020).
35. Seidel, J. et al. Conduction at domain walls in oxide multiferroics. *Nat. Mater.* **8**, 229–234 (2009).
36. Guo, H. Z. et al. Interfacial-strain-induced structural and polarization evolutions in epitaxial multiferroic $BiFeO_3$ (001) thin films. *ACS Appl. Mater. Interfaces* **7**, 2944–2951 (2015).
37. Izumi, M. et al. Atomically defined epitaxy and physical properties of strained $La_{0.6}Sr_{0.4}MnO_3$ films. *Appl. Phys. Lett.* **73**, 2497–2499 (1998).
38. Tang, Y. Y. et al. A multiaxial molecular ferroelectric with highest curie temperature and fastest polarization switching. *J. Am. Chem. Soc.* **139**, 13903–13908 (2017).
39. Yang, S. M. et al. Ac dynamics of ferroelectric domains from an investigation of the frequency dependence of hysteresis loops. *Phys. Rev. B* **82**, 174125 (2010).
40. Boyn, S. et al. Learning through ferroelectric domain dynamics in solid-state synapses. *Nat. Commun.* **8**, 14736 (2017).
41. Jo, J. Y. et al. Domain switching kinetics in disordered ferroelectric thin films. *Phys. Rev. Lett.* **99**, 267602 (2007).
42. Khan, A. I. et al. Negative capacitance in short-channel FinFETs externally connected to an epitaxial ferroelectric capacitor. *IEEE Electron Device Lett.* **37**, 111–114 (2015).
43. Si, M. W. et al. Steep-slope WSe_2 negative capacitance field-effect transistor. *Nano Lett.* **18**, 3682–3687 (2018).
44. Han, T. et al. Probing the field-effect transistor with monolayer MoS_2 prepared by APCVD. *Nanomaterials* **9**, 1209 (2019).
45. Hu, C. M., Salahuddin, S., Lin, C. I. & Khan, A. 0.2 V adiabatic NC-FinFET with 0.6 mA/μm I_{ON} and 0.1 nA/μm I_{OFF}. In *2015 73rd Annual Device Research Conference (DRC)* 39–40 (IEEE, 2015).
46. Saeidi, A., Jazaeri, F., Stolichnov, S., Enz, C. C. & Ionescu, A. M. Negative capacitance as universal digital and analog performance booster for complementary MOS transistors. *Sci. Rep.* **9**, 9105 (2019).
47. Zhou, J. R. et al. Incomplete dipoles flipping produced near hysteresis-free negative capacitance transistors. *IEEE Electron Device Lett.* **40**, 329–332 (2018).
48. Li, J., Liu, Y., Han, G. Q., Zhou, J. R. & Hao, Y. Comparative study of negative capacitance field-effect transistors with different MOS capacitances. *Nanoscale Res. Lett.* **14**, 171 (2019).
49. Verhulst, A. S. et al. Experimental details of a steep-slope ferroelectric InGaAs tunnel-FET with high-quality PZT and modeling insights in the transient polarization. *IEEE Trans. Electron Devices* **67**, 377–382 (2020).
50. Cao, W. & Banerjee, K. Is negative capacitance FET a steep-slope logic switch? *Nat. Commun.* **11**, 196 (2020).
51. Hoffmann, M., Slesazeck, S., Schroeder, U. & Mikolajick, T. What's next for negative capacitance electronics? *Nat. Electron.* **3**, 504–506 (2020).
52. Wang, F. et al. Subthermionic field-effect transistors with sub-5 nm gate lengths based on van der Waals ferroelectric heterostructures. *Sci. Bull.* **65**, 1444–1450 (2020).
53. Wang, X. F. et al. Two-mode MoS_2 filament transistor with extremely low subthreshold swing and record high On/Off ratio. *ACS Nano* **13**, 2205–2212 (2019).
54. Yao, Y. P. et al. Multi-state resistive switching memory with secure information storage in $Au/BiFe_{0.95}Mn_{0.05}O_3/La_{5/8}Ca_{3/8}MnO_3$ heterostructure. *Appl. Phys. Lett.* **100**, 193504 (2012).
55. Pilch, M. & Molak, A. Resistivity switching induced in ferroelectric phase of $PbTiO_3$ studied by XPS and electric conductivity tests. *J. Alloy. Compd.* **586**, 488–498 (2014).
56. Hoffmann, M. et al. Ferroelectric negative capacitance domain dynamics. *J. Appl. Phys.* **123**, 184101 (2018).
57. Pintilie, L. et al. Polarization switching and negative capacitance in epitaxial $PbZr_{0.2}Ti_{0.8}O_3$ thin films. *Phys. Rev. Appl.* **14**, 014080 (2020).
58. Shin, Y. H., Grinberg, I., Chen, I. W. & Rappe, A. M. Nucleation and growth mechanism of ferroelectric domain-wall motion. *Nature* **449**, 881–884 (2007).
59. Vries, I. D. D., Nierop, J. H. V. & Greene, J. R. Solid state class DE RF power source. In *IEEE International Symposium on Industrial Electronics 2*, 524–529 (IEEE, 1998).
60. Kobayashi, M., Ueyama, N., Jang, K. & Hiramoto, T. Experimental study on polarization-limited operation speed of negative capacitance FET with ferroelectric HfO2. In *2016 IEEE International Electron Devices Meeting (IEDM)* 12.3.1–12.3.4 (IEEE, 2016).
61. Kobayashi, M. A perspective on steep-subthreshold-slope negative-capacitance field-effect transistor. *Appl. Phys. Express* **11**, 110101 (2018).
62. Hoffmann, M. et al. Direct observation of negative capacitance in polycrystalline ferroelectric HfO_2. *Adv. Funct. Mater.* **26**, 8643–8649 (2016).
63. Goh, Y., Hwang, J., Lee, Y., Kim, M. & Jeon, S. Ultra-thin $Hf_{0.5}Zr_{0.5}O_2$ thin-film-based ferroelectric tunnel junction via stress induced crystallization. *Appl. Phys. Lett.* **117**, 242901 (2020).
64. Kim, Y. J. et al. Time-dependent negative capacitance effects in $Al_2O_3/BaTiO_3$ bilayers. *Nano Lett.* **16**, 4375–4381 (2016).
65. Wang, J. et al. Epitaxial $BiFeO_3$ thin films on Si. *Appl. Phys. Lett.* **85**, 2574–2576 (2004).
66. Rao, S. S. et al. Interface magnetism in epitaxial $BiFeO_3$-$La_{0.7}Sr_{0.3}MnO_3$ heterostructures integrated on Si(100). *Nano Lett.* **13**, 5814–5821 (2013).
67. Chu, Y. H. et al. Low voltage performance of epitaxial $BiFeO_3$ films on Si substrates through lanthanum substitution. *Appl. Phys. Lett.* **92**, 102909 (2008).
68. Ryu, H., Wu, H. N., Rao, F. B. & Zhu, W. J. Ferroelectric tunneling junctions based on aluminum oxide/zirconium-doped hafnium oxide for neuromorphic computing. *Sci. Rep.* **9**, 20383 (2019).
69. Goh, Y. & Jeon, S. The effect of the bottom electrode on ferroelectric tunnel junctions based on CMOS-compatible HfO_2. *Nanotechnology* **29**, 335201 (2018).
70. Lomenzo, P. D. et al. Universal Curie constant and pyroelectricity in doped ferroelectric HfO_2 thin films. *Nano Energy* **74**, 104733 (2020).