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Artificial synapses with a sponge-like double-layer porous oxide memristor

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Abstract

Closely following the rapid development of artificial intelligence, studies of the human brain and neurobiology are focusing on the biological mechanisms of neurons and synapses. Herein, a memory system employing a nanoporous double-layer structure for simulation of synaptic functions is described. The sponge-like double-layer porous (SLDLP) oxide stack of Pt/porous $LiCoO_2$/porous SiO_2/Si is designed as presynaptic and postsynaptic membranes. This bionic structure exhibits high ON–OFF ratios up to 10^8 during the stability test, and data can be maintained for 10^5 s despite a small read voltage of 0.5 V. Typical synaptic functions, such as nonlinear transmission characteristics, spike-timing-dependent plasticity, and learning-experience behaviors, are achieved simultaneously with this device. Based on the hydrodynamic transport mechanism of water molecules in porous sponges and the principle of water storage, the synaptic behavior of the device is discussed. The SLDLP oxide memristor is very promising due to its excellent synaptic performance and potential in neuromorphic computing.

Introduction

The development of deep learning is closely associated with the advancement of artificial intelligence, which is inseparable from brain science and neurobiology. Many recent research activities are fog on the biological mechanisms of neurons and synapses[1,2], and a good understanding of the biological brain is crucial to the design of intelligent machines[3–6]. The synaptic signal is transmitted from one neuron to the next, while the signal passing through the neural pathway is remembered through the stimulation of a pulsed signal[7,8]. Memristors with a small size, low energy consumption, and non-volatile performance are vital to many applications related to information storage, analog circuits, artificial intelligence, and analog neural networks[9,10]. Because of the similarity between the memristor and synapse, studies on the mechanisms and materials simulating the behavior and functions of nerve cells are crucial to the development of biologically inspired devices and prototypes[10,11].

Materials suitable for memristors mainly include oxides[12], sulfides[13], perovskites[14,15], two-dimensional materials[16,17], and related materials[18,19], and in particular, oxide-based memristors have been widely studied due to their high switching speed, large density, and compatibility with complementary metal–oxide–semiconductor processing[20,21]. The conduction mechanism of most of these materials is based on the formation and breakage of conductive metallic filaments via the accumulation of oxygen vacancies or metal atoms, such as Cu or Ag[22–25]. However, the stochastic and unpredictable formation process results in device variability, fluctuation of resistance states, and excessive "write" noise, consequently undermining the stability of the materials[23,25]. Therefore, it is necessary to control the switching filament formation and dynamics of memristors. To overcome these hurdles, approaches, including stoichiometry control[26], thermal annealing[27], and insertion of thin metal layers[28], have been suggested, and the control of filaments and their

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formation at desirable locations must be improved and better understood. Introducing a porous structure into the resistive layer is one of the viable methods to provide channels for ion transport. For example, Wang et al. prepared multiple nanoporous (NP) SiO_x layers to control filament formation[29,30], and Tour et al. proposed a three-dimensional NP Ta_2O_{5-x} structure with graphene boasting high-density storage and low power consumption[31,32]. Obviously, a porous structure can regulate the conducting channel and enhance the device performance[33].

Combining bionic ideas with device design is an effective way to study defects in electronic devices and the underlying mechanisms. Zhang et al. proposed a three-dimensional spiral microstructure as the basic unit and constructed bionic soft three-dimensional mesh materials with defect-insensitive characteristics, by varying the spatial topology to reproduce the anisotropic nonlinear mechanical response of biological tissues[34]. Fan et al. prepared perovskite nanowires for an electrochemical eye with a hemispherical retina that can imitate the photoreceptors in the human retina[11]. Furthermore, the transport characteristics of water in a natural cave structure have been combined with hydrodynamics and ion transport to design a karst-like hierarchical porous structure with good characteristics[35]. However, the nonuniform pore diameters in the silicon oxide layer cause large variations in the essential switching elements, and random and nonuniform ion migration in $LiCoO_2$ hampers the optimal switching functionalities. Lithium ion migration in $LiCoO_2$-based memristors is similar to the information exchange process between synapses and neurons in the brain[36–40]. $LiCoO_2$ is used in Li-ion batteries to improve the capacity and mitigate the volume expansion during deintercalation of lithium ions under repetitive charging and discharging[41–43]. It is also important to investigate the relationship between the device performance and NP structure, as well as potential device applications. In fact, it is advisable to adopt the bionic route in designing and utilizing the functions of natural porous structures in memristor devices to better simulate the functions of synapses and elucidate the associated mechanisms.

In this work, a bionic double-layer NP structure comprising a Pt/porous $LiCoO_2$/porous SiO_2/Si stack is designed. The device delivers high memristive performance due to the unique electrochemical properties of porous SiO_2 ($PSiO_2$) and porous $LiCoO_2$ ($PLiCoO_2$), such as a high ON–OFF ratio[44–48]. The typical synaptic functions of the sponge-like double-layer porous (SLDLP) memristor are simulated, and a model is proposed to describe the mechanism of the synaptic behavior by considering the hydrodynamic transport of water molecules in porous spongy structures, as well as the principle of water storage. The memristor with the SLDLP structure has great potential in areas, such as artificial intelligence and neuromorphic computing (Scheme 1).

Results and discussion

The microstructure of the materials determines the device characteristics[49,50]. Oxide-based memristors with a porous structure have recently been demonstrated to have promising functionalities that improve the device performance, such as scalability[51,52]. Based on the bionic structure and principle, it is meaningful to design and construct a device with a porous structure. Natural sponges have many interesting and unique properties, such as porosity, elasticity, pressure resistance, water absorption, and water penetration. Hence, a buffer layer of porous silicon oxide is designed and fabricated according to the structure of a sponge. $PLiCoO_2$ is incorporated into the $PSiO_2$ structure by radio frequency (RF) magnetron sputtering to provide conduction channels for ion transport[53,54]. Moreover, a porous interface is fabricated between the $PSiO_2$ layer and $PLiCoO_2$ layer to provide conduction channels to enhance the electrochemical reactions.

The preparation process of the double-layer porous device is illustrated in Fig. 1. Figure 1a shows a diagram of the primary functionalized materials, and the lower right picture depicts the sponge and enlarged microstructure. Figure 1b, c illustrates the preparation process of $PSiO_2$, and thorough mixing of the two solutions is shown in Fig. 1d. The SiO_2 solution is spin-coated on a highly doped p-type Si (100) wafer, and annealed at a reduced pressure of 10^{-1} Pa and a temperature of 400 °C. The 3D spongy SiO_2 structure (~70 nm) is prepared as shown in Fig. 1e, and Fig. 1f presents the structure of the memristor.

Scheme 1 Schematic showing the functionalized sponge-like porous materials and potential applications to electronics devices.

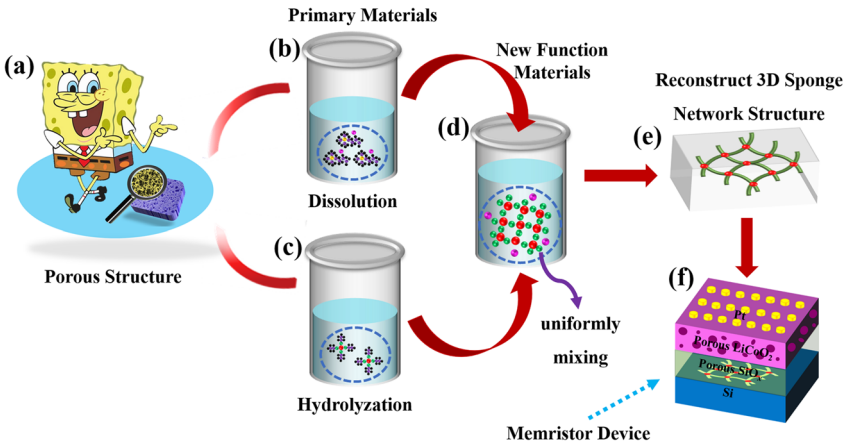

Fig. 1 Preparation of a sponge-like double layer porous oxide memristor.

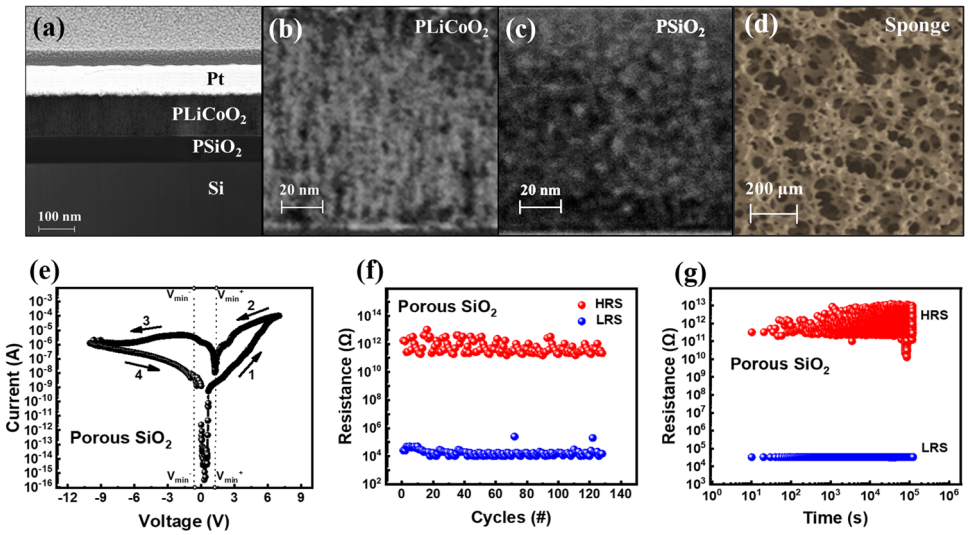

Fig. 2 The microstructures and electrical properties of the sponge-like double-layer porous oxide memristor.

The $PLiCoO_2$ film (~100 nm) and Pt electrode film (~80 nm) are prepared by magnetron sputtering.

The dependence of the memristive behavior on the double-layer porous structure is investigated. A TEM image of the Pt/$PLiCoO_2$/$PSiO_2$/Si memristor is displayed in Fig. 2a, and Fig. 2b presents a cross-sectional image of $PLiCoO_2$, revealing that pores with sizes of 2–20 nm are distributed throughout the $LiCoO_2$ layer. Figure 2c shows a cross-sectional TEM image of the porous SiO_2, and pores 2–5 nm in size are evenly distributed throughout the SiO_2 layer. The porous structure in each oxide layer is similar to that in Fig. 2d, which shows an electron micrograph of the natural sponge structure[55]. To evaluate whether the device has basic synaptic functions, the storage and memory functions are studied in the direct current (DC) mode using a Keithley S4200. To characterize the electrochemical performance of the $PSiO_2$/$PLiCoO_2$ memristor, the current–voltage (I–V) characteristics, stability, and retention are determined and shown in Fig. 2e–g, respectively. As shown in Fig. 2e, the device does not show a forming process. The switching parameters for various porous-based memristors, such as single porous, array porous, and NP memristors, are compared. The V_{set}, V_{reset}, endurance cycles, ON–OFF ratio and retention are summarized in Table S1 as Supporting Information. Interestingly, the minimum currents in the switching I–V plot exist at certain positive and negative voltages, but not at zero voltage, indicating that the electric field through the porous layer becomes a minimum when a voltage is applied, so charge transfer can be suppressed[31,32]. No electrical shorts are found in the device, as there is no direct contact between Pt and Si.

In the experiment, different positive voltages from 5 to 14 V are applied, and the voltage step and current compliance are 0.01 and 0.01 A, respectively. As $V_{applied}$ is increased, V_{min} increases, as shown in Fig. S1a. The linear relationship confirms the idea that the switching mechanism is related to lithium ions in the pores and depends on the external electric field, because a larger V_{set} drives more lithium ions to the pores[31,35]. A larger applied voltage traps a mass of charges and produces a higher internal electric field during programming. Therefore, a higher external electric field is needed to control the charge transfer and neutralize it through the porous silicon oxide[31,35,50]. The nanopores with nonuniform diameters affect the device-to-device uniformity, causing a large variation in the essential switching elements, and programming paths and restricting the optimal switching functionalities.

To further analyze the uniformity of switching in the $PSiO_2/PLiCoO_2$ memristor, we statistically investigate the relationship of $V_{applied}$–V_{min} for >40 devices by sweeping the voltage from −8 to 0 V. The V_{min} range is from −0.21 to −3.51 V, and the fitting parameter is 0.98 ≈ 1, as shown in the plot in Fig. S1b. The maximum resistance is ~10^{12} Ω, as shown in Fig. S1c. The durability is determined to study the stability of the $PSiO_2/PLiCoO_2$ memristor. The voltage is swept from 10 to −10 V in the DC mode, and the voltage step and current compliance are ±0.01 and 0.01 A, respectively. The high resistive state (HRS) and low resistive state (LRS) during 128 switching cycles show a high ON–OFF ratio of up to 10^8, as shown in Fig. 2f. The retention of the HRS and LRS is measured at a low voltage of 0.5 V, and the retention time is up to 10^5 s, as shown in Fig. 2g, showing alleviation of short data retention. The memristor properties of the nonporous structure are determined and shown in Fig. S2. The device exhibits an obvious forming behavior at a voltage of 6.55 V, mainly due to the disordered movement of lithium ions in the silicon oxide layer, as shown in Fig. S2a. The ON–OFF ratio is ~10^5, and the LRS retention time increases gradually with time, reaching a stable value of 10^7 Ω, as shown in Fig. S2b, c. Field-emission scanning electron microscopy (FE-SEM) images of the nonporous SiO_2 and porous SiO_2 are depicted in Fig. S3a, b. The porous structure has the following advantages. The porous structure in the $LiCoO_2$ layer and SiO_2 layer can relieve the volume expansion of $LiCoO_2$ and SiO_2 during cycling, and the pores in the $LiCoO_2$ layer provide channels for ion transport and increase the concentration of lithium ions under the action of the same electric field. The pores in SiO_2 provide channels for fast ion transport, and adequate contact between lithium ions and silicon oxide; by removing the external electric field, the porous channels increase the diffusion path of lithium ions, and the retention of the LRS is longer.

There are small pores in a piece of sponge, and upon exposure to water, water infiltrates along the tubular walls. When the upward pulling force is equal to the gravity of the liquid, the liquid stops rising according to the capillary phenomenon, and water fills the sponge gaps. Because the sponge has many small voids, it is originally filled with air. When water is applied, the sponge experiences a pressure that expels air, and when the pressure is released, the sponge returns to its original shape by taking in air. The water is subjected to atmospheric pressure, and at times, the pressure in the sponge is relatively small such that water enters the sponge. In our device, the porous layer also has many small pores. Under the action of an electric field, the electric field is concentrated around the pores, and ions migrate along the pores. After the electric field is removed, the small tortuous pores resemble the porous structure of a sponge, the ions can be stably stored in the porous layer, and the device exhibits stable performance. Therefore, the $PSiO_2/PLiCoO_2$ device is quite stable, and repeated charging–discharging ensures that sufficient lithium ions react with $PSiO_2$, so that the device reaches a lower resistance state compared to the nonporous structure. After the external voltage is turned off, the porous structure has a negative charge, thus providing more adsorption sites for lithium ions and making it difficult for them to diffuse out of the silicon oxide layer, consequently improving the retention time of the device[50].

The flexibility of the memory functions of the memristor is similar to that of the synapse of organisms. While transmitting a signal, the segment is processed, and the signal is memorized. Because many functions of the memristor are very close to those of biological synapses, the memristor works like synapses and can form the basis for a simulated neural network. Accordingly, the use of memristors to conduct biological synapse simulation is desirable because the density of synapses in artificial neural networks is close to that in biological neural networks, thereby achieving low power consumption and high integration in neural network simulation[56–58]. Biological research shows that the strength of the synaptic weights is closely related to neural memory, and in our device, the top and bottom electrodes can be regarded as presynaptic and postsynaptic neurons, respectively, with the $PLiCoO_2$ layer and $PSiO_2$ being the presynaptic and postsynaptic membranes, respectively.

The increase/decrease in synaptic weights is controlled by the concentration of ions, and release/suppression of these ions is associated with release/suppression under certain conditions. Here, the conductivity is considered a synaptic weight, and behavior similar to the nonlinear transmission characteristics of biological synapses is simulated. The changes in conductance are indirectly related to the current. Figure 3 shows the current

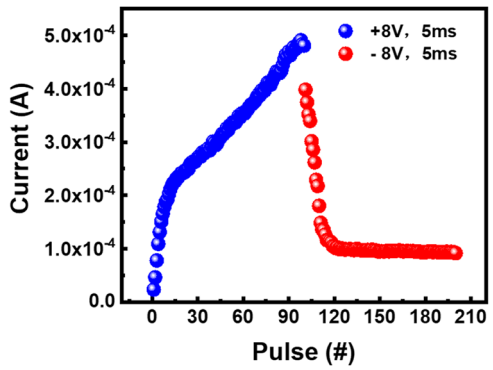

Fig. 3 Device conductivity increased or decreased by consecutive pulses.

modification in response to a stimulus. Under the stimulation of positive voltage pulses (8 V, 5 ms), the current of the device increases as the pulse sequence is applied. Conversely, under the stimulation of negative voltage pulses (−8 V, 5 ms), the current of the device decreases as the pulse sequence is applied. Regulation of the current is considered to be associated with migration of lithium ions in the lithium cobalt oxide layer and silicon oxide layer, as well as the electrochemical reaction process with silicon oxide. With a gradual increase in the stimulation pulse frequency, lithium ions are released from the $PLiCoO_2$ layer, and holes are formed in the t_{2g} orbital of Li_xCoO_2 and $PLiCoO_2$, causing a change from insulating to semiconducting or even conducting[58–61]. Lithium ions migrate along the porous channels of the $LiCoO_2$ layer and SiO_2 layer, and react electrochemically with SiO_2 to form Li_ySiO_2. The conductance increases gradually under stimulation by positive voltage pulses, but when a negative voltage pulse is applied, lithium ions are released from the $PSiO_2$ layer to recombine with holes in the t_{2g} valence band of Li_xCoO_2. The conductance decreases gradually under the stimulation of negative voltage pulses[37].

Plasticity is an important characteristic of a synapse. Synaptic plasticity is time dependent when applying different pulse signals. Here, different tests are performed to simulate the changes in the synaptic weights, as shown in Fig. 4. Figure 4a, b shows that longer pulse widths produce larger changes in the synaptic weights for the same pulse interval of 5 ms and pulse voltage of 8 V. Figure 4c, d shows that shorter pulse intervals result in larger changes in the device synaptic weights for the same pulse width of 5 ms. Figure 4e, f shows that a larger pulse amplitude causes larger changes in the synaptic weights for the same pulse interval of 10 ms and pulse width of 5 ms. The adjustment of synaptic weights is associated with the migration of lithium ions between the $PLiCoO_2$ layer and $PSiO_2$ layer, as well as the reaction rate with $PSiO_2$. In the case of larger voltage or longer stimulation, the larger flow in the ion conductive channels from one electrode to another causes larger changes in the synaptic weights.

According to memory retention, synaptic plasticity can be classified as short-term plasticity (STP) and long-term plasticity (LTP), consistent with short-term memory and long-term memory in biology. By applying a continuous voltage pulse signal to the synaptic device to complete the learning process and then a small read voltage pulse to the device to complete the forgetting process, the device can be changed from STP to LTP[62,63]. The memory retention characteristics of our device are shown in Fig. 5. Figure 5a shows that as the synaptic device is stimulated sequentially with 100 positive voltage pulses, the synaptic weights increase gradually. There is an interesting phenomenon that after turning off the external electric field, the synaptic weights decay spontaneously with time. In the beginning, the decay is rapid and then slows gradually. This phenomenon is similar to the learning–forgetting process of the brain[63]. The synaptic weights do not return to the initial state but rather remain in a stable intermediate state. This means that the change in the synaptic weights consists of two parts: STP and LTP. A model is thus proposed to explain the phenomenon. Figure 5b, c corresponds to rectangular areas (1) and (2) in Fig. 5a, respectively. By applying positive pulses continuously, lithium ions are released from the $PLiCoO_2$ layer and transported along the pore channels. At the $PSiO_2/PLiCoO_2$ interface, the small holes are surrounded by large holes, as shown in Fig. 6a, b, corresponding to the rectangular area in Fig. 6a. Under the electric field, the porous structure concentrates the electric field, and the field strength is the strongest at the tangent point of two holes. Hence, ions migrate along the field strength direction, and an ion current is formed at the interface of the double-layer porous structure. A model is proposed to explain ion migration at this interface, as shown in Fig. S4a, with ions entering the $PSiO_2$ layer and reacting with SiO_2. When a positive voltage is applied to the device, it can be clearly seen that there exists a higher electric field density around the area of the pores at the $PLiCoO_2/PSiO_2$ interface. At the tangent point between pores at the interface of the two layers of porous materials, the electric field exhibits a high field strength due to superposition, confirming the electrical field concentration capability around the nanopores. Then, ions migrate around the pores[50]. After turning off the electric field, the partly free lithium ions in the porous silicon oxide layer diffuse to the lithium cobalt oxide layer, and the device exhibits STP behavior, as shown in Fig. S4b. The model in Fig. 5d corresponding to rectangular area (3) in Fig. 5a explains the phenomenon. The main reason for the water storage capacity of the sponge structure is that the many small pores act as capillaries. The combined effects of surface tension, cohesion, and adhesion of the liquid allow water

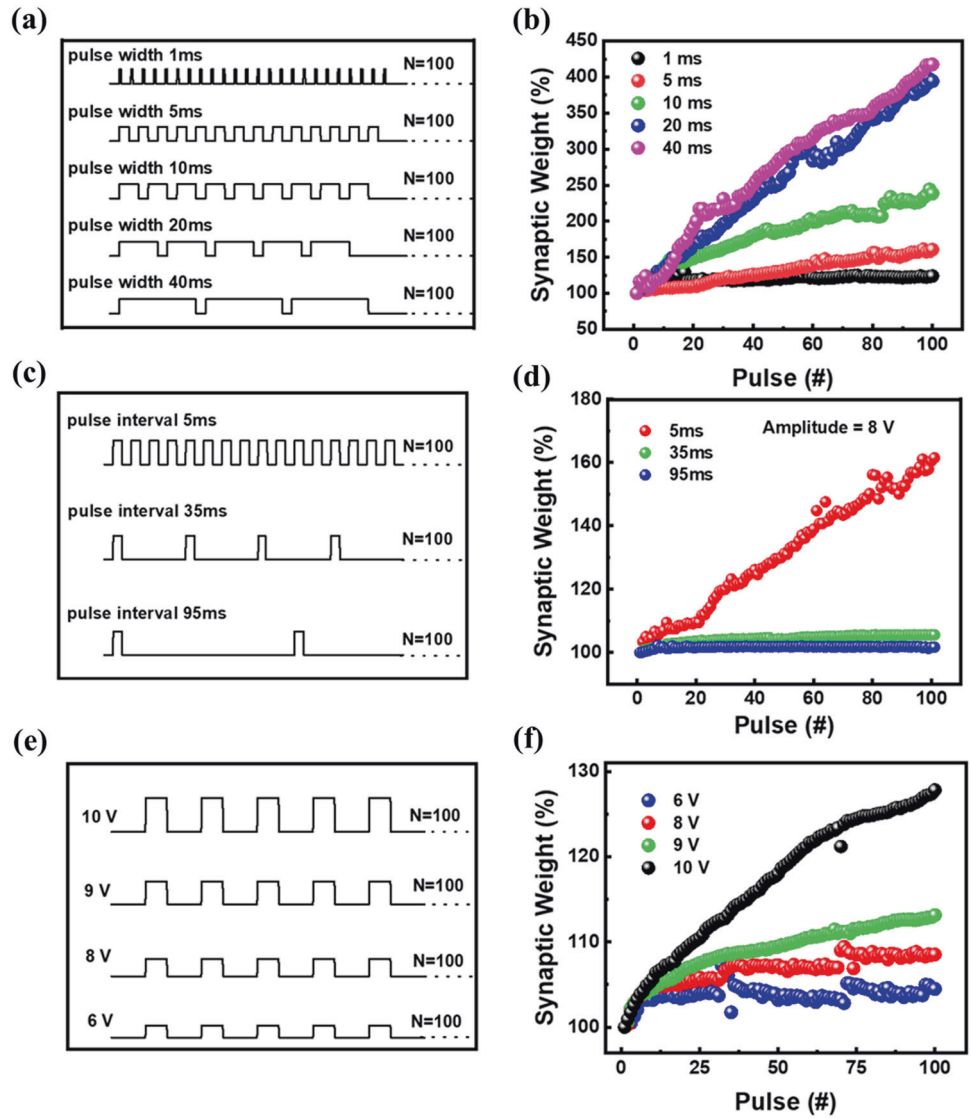

Fig. 4 Synaptic plasticity is studied by applying different pulse signals.

to be stored in the sponge. In the $PSiO_2$ layer, owing to the small pores, the diffusion path of lithium ions adsorbed around the porous channel increases. At the $PSiO_2$/$PLiCoO_2$ interface, small pores surround large pores, and under capillary action, ions are adsorbed at the interfaces. Hence, there are more adsorption sites for ions and hindrance of diffusion of lithium ions, resulting in the improved lithium storage capacity and stable LTP behavior.

Preservation of the memory information in the brain is related to time and learning frequency. After repeated and timely learning of input information, short-term memory can become long-term memory and remain in the human brain for a long time[63]. Herein, a repeat learning process is tested. Figure 7 shows the learning experience for a four repetitive pulse stimulation. The time interval between each pulse is 20 s, and the synaptic weight corresponds to the amount of memory information. First, 100 consecutive positive voltage pulses are applied to the device, and the voltage pulses are turned off for 20 s. Afterward, 80 consecutive positive voltage pulses are applied, and the synaptic weight changes by 18.09%. By applying 60 and 40 consecutive positive voltage pulses, the synaptic weight changes by 4.16% and 7.82%, respectively. After the four consecutive voltage pulse stimulation, the synaptic weight is maintained >60%. The learning experience is similar to the repeated learning and memory process in the human brain.

Spike-timing-dependent plasticity (STDP) is another important performance indicator of biological synapses

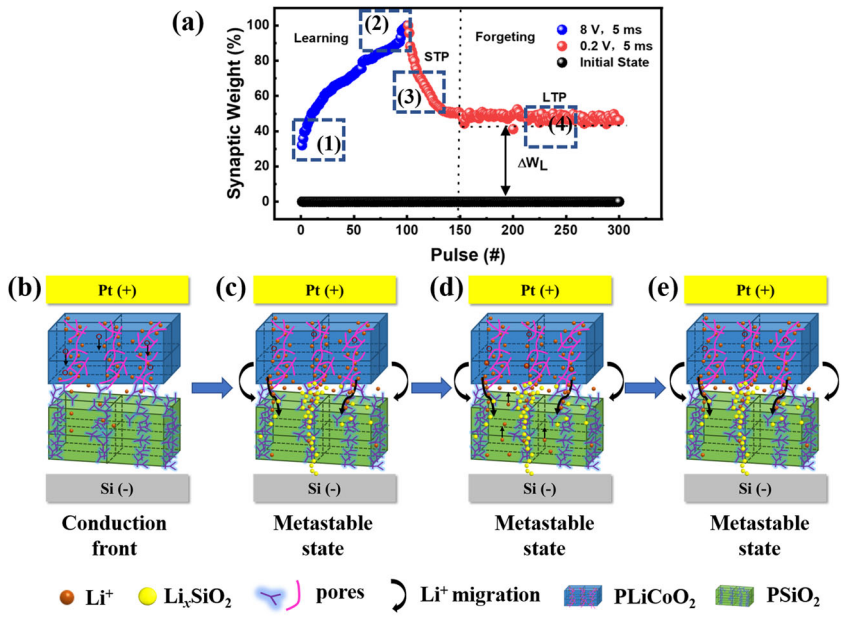

Fig. 5 The characteristics of learning-forgetting behaviors of the device and a model is proposed to explain the phenomenon.

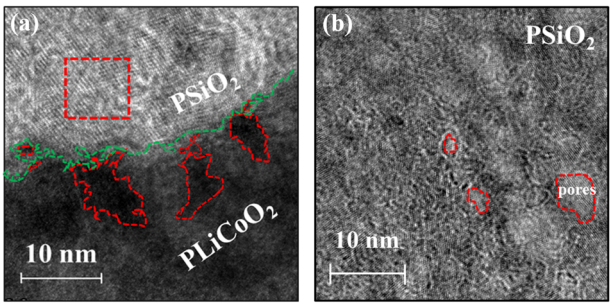

Fig. 6 Cross-sectional HR-TEM images of $PSiO_2/PLiCoO_2$ and $PSiO_2$ layers.

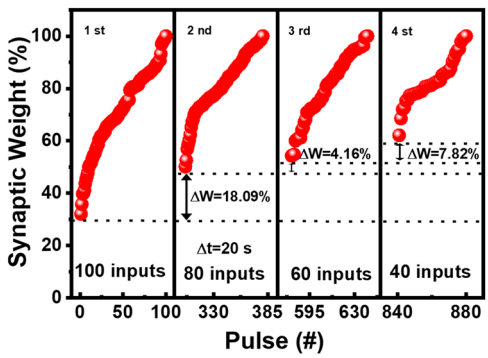

Fig. 7 Learning experience of four repetitive pulse stimulation.

according to the Hebbian learning rule[64,65]. To implement STDP, a pair of pulses is applied to the top and bottom electrodes as presynaptic and postsynaptic spikes with $V^+/V^- = 8\,V/-8\,V$, as shown in Fig. 8. There is an interval of 3 s between V^+ and V^-, and the time interval between the spikes is denoted $\Delta t > 0$ ($\Delta t < 0$; where Δt is the time interval of the pulse stimulations before and after the synapse. According to the asymmetric Hebbian learning rule, when the activity of presynaptic neurons precedes that of postsynaptic neurons, $\Delta t > 0$; otherwise, $\Delta t < 0$). The STDP characteristics of the $PSiO_2/PLiCoO_2$ memristor are shown in Fig. 8a, and the synaptic weight changes are presented in Fig. 8b. Figure 8b also shows the fitted curves of the STDP synaptic weight change ΔW, which is defined as the percentage change in the cell conductance after the STDP event. The fitting curve is described by Eq. (1).

$$\Delta W = A \exp(-\Delta t/\tau) + \Delta W_0 \quad (1)$$

where A and τ are the scale factor and time constant of the STDP function, respectively, and ΔW_0 is a constant representing unassociated synaptic regulation. The pre-spike is sent to the Pt electrode, and the postspike is sent to the Si electrode. It takes ~1–3 ms to complete the STDP function, which is similar to the time consumed by the biological neural circuit to complete the STDP function (10 ms).

Conclusion

The $Pt/PLiCoO_2/PSiO_2/Si$ stack delivers good electrical performance and exhibits typical synaptic functions under

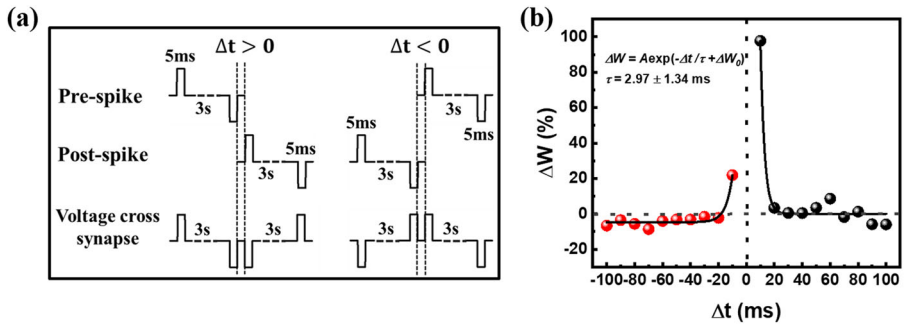

Fig. 8 STDP behavior of the device.

stimulation. The migration mechanism of lithium ions in the $PLiCoO_2$ layer and $PSiO_2$ layer is investigated. Electrical tests show that the SLDLP structure has improved stability, an ON–OFF ratio of 10^8, and a retention time of 10^5 s. The typical synaptic functions, such as LTP, STP, STDP, and learning experience, are achieved. The device provides pathways for transport of lithium ions and retains lithium ions in the porous structure to improve the device characteristics. The conductance can be regulated by changing the external conditions, such as pulse voltage or stimulation time. The device with the NP structure that exhibits uniform switching characteristics has great potential in scalable memristor arrays, and the memristor with the bionic SLDLP structure can be readily implemented in neuromorphic computing.

Experimental section

Preparation of the porous silicon oxide solutions

Solution A was prepared with 1.6 ml of C_2H_5OH, 0.16 ml of HCl (3×10^{-3} mol), and 2 ml of tetraethyl orthosilicate ($C_8H_{20}O_4Si$). They were mixed and stirred at room temperature for 24 h. Solution B was prepared with 0.3 g of cetyltrimethylammonium chloride ($C_{19}H_{42}Cl$ N), 8.88 ml of C_2H_5OH, and 0.16 ml of HCl (5.5×10^{-2} mol). They were mixed and stirred at room temperature for 24 h until the powder dissolved. Solution C was prepared by stirring solutions A and B at room temperature for 24 h. Mother liquor C was prepared with 1 mL of solution C and 7 mL of C_2H_5OH, and stirred at room temperature for 1 h.

Preparation of the porous silicon oxide films

A highly doped p-type Si (100) wafer (2×2 cm^2) was put into equal volumes of hydrogen peroxide, acetone, and anhydrous ethanol, sonicated for 30 min to remove surface impurities, and dried with nitrogen gas. It was then rinsed with DI water, dried with nitrogen, and spin-coated by pipetting 200 μL of solution D onto the substrate. A $PSiO_2$ film was formed by spin coating (9000 r.p.m. for 16 min) and annealing at 400 °C at a reduced pressure of 10^{-1} Pa under a 10 s.c.c.m. Ar flow for 1 h.

Preparation of the porous $LiCoO_2$ films

A $LiCoO_2$ (~100 nm) film was deposited on $PSiO_2$/Si by magnetron sputtering. The $PSiO_2$/Si substrate was fixed on the sample stage, and a crystalline (003) lithium cobaltite target was the target positioned at a distance of 6 cm from the substrate. The equipment was evacuated to a pressure of 10^{-4} Pa, and a mixture of Ar:O_2 (3:1) was introduced at a flow rate of 30 s.c.c.m. to reach a working pressure of 2.0 Pa. Deposition was carried out at an RF power of 200 W and a rotation speed of 30 r.p.m. for 1 h.

Preparation of the Pt electrodes

Pt (~80 nm) films were deposited on $PLiCoO_2/PSiO_2$/Si by magnetron sputtering. A mask with an aperture of 200 μm, an array structure of 8×8, and an area of 2×2 cm^2 was fixed on the $PLiCoO_2/PSiO_2$/Si surface. A high-purity Pt target was placed 6 cm from the substrate. The vacuum chamber was evacuated to 10^{-4} Pa after Ar was blown into the chamber at a flow rate of 30 s.c.c.m. to reach a working pressure of 2 Pa. The sputtering current was 0.45 A, the sample rotation speed was 30 r.p.m., and the deposition time was 3 min.

Device characterization

The morphology and structure of $PSiO_2$, $PLiCoO_2$, and nonporous SiO_2 were investigated by FE-SEM, and the cross-section of Pt/$PLiCoO_2/PSiO_2$/Si was prepared with a focused ion beam. The morphology and porous features of $LiCoO_2$ and SiO_2 were examined by taking bright-field images at 200 keV on a field-emission TEM (FEI TECNAI-F20). The electrical properties and synapse behavior were determined using a Keithley 4200 semiconductor parameter analyzer and an arbitrary function generator (AFG31000, Tektronix), respectively.

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Conflict of interest
The authors declare that they have no conflict of interest.

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