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Negative capacitance transistors with monolayer black phosphorus

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Quantum transport properties of negative capacitance transistors (NC-FETs) with monolayer black phosphorus (ML-BP) are theoretically studied. Our calculations show that atomistic thin ML-BP can enhance the amplification effect of the ferroelectric layer, and subthreshold swing is effectively reduced to 27 mV per decade in ML-BP NC-FETs. Device performance can be further improved by increasing the thickness of ferroelectric layer and using thinner or high-*k* insulate layer. Due to the temperature dependence of ferroelectric layer ML-BP NC-FETs have higher on-state current at low temperature, which is different from that of MOSFETs. By considering the metal–ferroelectric interface layer, our calculations show that the device performance is degraded by the interface. Compared with the International Technology Roadmap (ITRS) 2013 requirements, ML-BP NC-FETs can fulfil the ITRS requirements for high-performance logic with a reduced supply voltage. The new device can achieve very low power delay product per device width at $V_D = 0.3$ V, which is just 44% of that in ML-BP FETs.

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INTRODUCTION

The development of complementary metal-oxide-semiconductor (CMOS) technology in the past half century has followed the Moore's law[1] to a very good extent. This path is however reaching the physical limit where power dissipation in circuits has become the game-breaker. Even though various technologies have been applied to improve device performance in CMOS—strained silicon, high-*k* metal gate, FinFET, etc.,[2] these do not change the operation principle of metal oxide semiconductor field effect transistor (MOSFET) in which the current is controlled by modulating the thermionic carriers over the potential barrier of the transistor channel. A consequence is that the subthreshold swing (SS) can not be made smaller than the thermal limit of 60 mV per decade,[3] which is a limit dictated by the fundamental physics of the Boltzmann distribution. On the other hand, if somehow SS could break this limit, one would be able to reduce the external voltages for the transistor operation, thereby reducing power dissipation and prolonging the Moore's law scaling. The economic impact of such a scenario would be enormous.

To this end, an extremely interesting idea is the negative capacitance field effect transistor (NC-FET), which was theoretically proposed to achieve SS below the 60 mV per decade limit.[4] In NC-FETs, a ferroelectric (FE) gate layer is applied and couples with a positive capacitor to realise a bistable state. The combination of the external electric field and the polarisation in the FE material gives rise to a negative voltage drop through the FE layer and, in effect, results in a 'voltage amplification' that improves the subthreshold characteristics. This possibility of achieving sub 60-mV per decade has excited great interests on NC-FETs.[5–11] Experimentally, a sub-60 mV per decade has been achieved in polymer FE MOSFETs[5] and the capacitance of FE-dielectric bilayer has been enhanced due to the negative capacitance effect.[6] Very recently, a direct measurement of negative differential capacitance has been achieved,[12] and negative capacitance FinFETs have be realised to achieve extremely low-steep swings.[13]

In this work, we show that the voltage amplification effect in NC-FETs can be further enhanced if the transistor channel is made of two-dimensional (2D) materials because 2D channels have better gate control to begin with. More importantly, it turns out that SS can be expressed by a transport factor multiplying a body-factor, and the use of 2D materials decreases the latter (see below) thus reduces the SS. From the practical point of view, the thin layer of 2D materials makes them a natural choice for producing flexible structures due to their out-of-plane flexibility and, for flexible and wearable consumer electronics.[14] Therefore, in this work we propose and theoretically investigate the interesting device physics of a new class of emerging nanoelectronics where FE is combined with 2D materials leading to the 2D NC-FETs.

To be more specific but without losing generality, we consider the newly discovered monolayer (ML) black phosphorus (BP) as the channel material. ML-BP is a direct gap semiconductor and has a relatively high mobility.[15–20] Therefore, higher on-state current and faster switching speed can be achieved in ML-BP devices compared with monolayer transition metal dichalcogenides (TMDCs) FETs.[20] We predict that the proposed device has a good gate control and can achieve low-power performance at the drain voltage $V_D = 0.3$ V, which is much smaller than that of the Si FETs. The power delay product per device width is predicted to be much smaller than the requirement of the International Technology Roadmap (ITRS) 2013 for high-performance (HP) applications in the 2024 horizon.[21] We present design

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considerations for optimising the performance, namely by using thicker FE layer and thinner or high-*k* insulator layers. The temperature dependence, electrode–FE interface effects and scaling behaviour of NC-FETs are also determined.

RESULTS

We consider a device with a 400 nm FE layer, 3 nm equivalent oxide thickness (EOT) layer and 20 nm thickness substrate as shown in Figure 1a. We first compared the device characteristics of FETs and NC-FETs. The drain current I_D versus V_G characteristic is presented in Figure 2a. From the figure, we can clearly see that the device performance is greatly improved in NC-FETs. When the FE layer is applied, the SS is reduced from 130 to 72 mV per decade and the current at $V_G = 0.5$ V is increased by 713 times as demonstrated in Figure 2a. Even though the SS is improved, it is still greater than the thermal limit. For Equation (2), there are three different ways to further improve device performance: decreasing C_{FE} and increasing C_{INS1} or C_B. We first analyse the effects of the FE layer thickness. Increasing the thickness, the device performance is improved as shown in Figure 2b. With a fix I_{ON}/I_{OFF} ratio, higher I_{ON} can be obtained in NC-FETs with thicker FE layer. Here, on-state and off-state currents are calculated with a fixed V_G window equal to the supply voltage V_D of 0.5 V. Another improvement of device performance is achieved by increasing the capacitance of the insulator layer. Here different EOT and gate oxide layer materials are applied. When the thickness of FE layer reaches 700 nm, SS smaller than 60 mV per decade is obtained in NC-FETs with 3 nm EOT as shown in Figure 2c. It is also found that the performance of NC-FETs can be improved by using high-*k* gate oxide layer. Seven different gate oxide materials are applied and smaller SS can be achieved at the same I_{ON} current in NC-FETs with high-*k* gate oxide layer as shown in Figure 2d.

Regarding the design guidelines of NC-FETs as low power devices, the temperature effect on device performance is studied. It is well known that the polarisation of FE layer greatly depends on the temperature and the state of transistor is modulated by controlling the thermionic carrier over the barrier. Therefore, the temperature has a great impact on the performance of NC-FETs. The dynamic of FE polarisation can be described by the Landau–Khalatnikov (LK) equation[4]

$$\rho \frac{d\vec{P}}{dt} + \nabla_{\vec{P}} U = 0 \quad (1)$$

where the free energy of FE material is the function of a series expansion of polarisation:[4]

$$U = \alpha P^2 + \beta P^4 + \gamma P^6 - \vec{E}_{ext} \cdot \vec{P} \quad (2)$$

where α, β and γ are laudau coefficients and P is the polarisation,

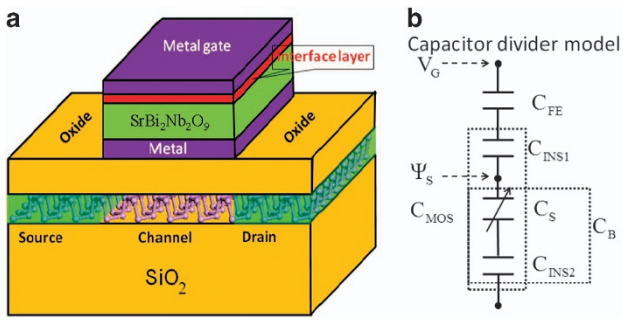

Figure 1. The negative capacitance (NC) transistor (FET) based on monolayer black phosphorus (ML-BP). (**a**) Sketch of the simulated ML-BP NC-FET. Transport direction is assumed to be the armchair direction of ML-BP. (**b**) Equivalent capacitor divider model of ML-BP NC-FETs.

$\alpha = -3.74 \times 10^8$, $\beta = -9.4 \times 10^7$, $\gamma = 1.18 \times 10^9$, for $SrBi_2Nb_2O_9$ at room temperature.[22] The α is a coefficient with a temperature dependence: $\alpha = \alpha_0(T - T_c)$, $\alpha_0 = -1.03 \times 10^6$, $T_c = 663$ K is curie temperature. On the basis of the model, the temperature dependence of NC-FETs can be simulated. Due to the existence of the FE layer, NC-FETs have different temperature dependence of the drain current from FETs. For a classical FET, the carrier follows Fermi–Dirac distribution. As the temperature increases, the Boltzmann tail broadens and more thermionic carriers transport over the barrier, and the drain current increases at all gate voltages as shown in Figure 3a, which shows the I_D as a function of T for 15 nm ML-BP FETs at different gate voltages. With the decreasing of temperature, the current is markedly reduced. The NC-FETs have different temperature dependence due to the existence of FE layer as shown in Figure 3b. We observe that at lower T, the drain current is reduced at $V_G < 0.3$ V and is increased at $V_G > 0.5$ V, which results in smaller SS at lower temperature as shown in Figure 3c. NC-FETs also work on the control of thermionic current over the barrier but with additional FE layer. Hence, the phenonmena can be attributed to the temperature dependence of the FE layer. The polarisation of FE layer has a phase change with the evolution of temperature. There is a transition temperature T_c. At a lower temperature below T_c, the polarisation of the $SrBi_2Nb_2O_9$ layer is very large and the material is in FE phase and the gate voltage is greatly amplified. Even though the carrier is partly frozen with the decreasing temperature, the lowered barrier due to the amplification effect leads to large current as shown in Figure 3b. As the temperature is increased to T_c, the material reaches phase change point and would change from the FE state to a paraelectric phase. With the increasing of temperature, the sign of laudau parameter α will be changed from negative to positive, and the free energy does not have the unstable equilibrium state. Therefore, above T_c, NC-FETs cannot work in the negative capacitance region and the amplification effect of the FE layer will disappear.

Although the device performance can be optimised in properly engineered devices and sub-60 mV per decade can be achieved, and ideal condition is assumed and many effects will deteriorate the performance of NC-FETs. Various interfacial effects including the strain, impurities, bonding and screening etc at both interfaces of the FE layer will inevitably change the ferroelectricity and further modulate the charge transport process.[23–25] Due to broken symmetry at the top and bottom interfaces of FE layer, there will be asymmetrical charge screening effects that can be modelled by a different extrapolation length of the interfacial polarisation. All these effects can be important especially for ultrathin FE layer. However, for our parameter space where the thickness of the FE layer is not too thin, the size-driven phase changes can be safely disregarded and the well-known interfacial capacitance model can be employed to study the interfacial effects for temperature and thickness space investigated in this work. In reality, perfect contact between the metal electrode and FE layer is hard to obtain and an interface layer is usually sandwiched between the two materials as shown in Figure 1a. Interface between metal electrodes and FE layer is an important effect, which leads to many abnormal behaviours of FE material. Interface capacitance model is applied to modelling the interface effect.[26] Here, just the interface between the top gate and the FE layer is considered and the interface under the FE layer is neglected. So, the effective capacitance C_{EFF} of the FE layer including interface effect can be described as a series connection of pure FE layer capacitance C_{FE} and interface layer capacitance C_{INT} as following:[26]

$$\frac{1}{C_{EFF}} = \frac{1}{C_{FE}} + \frac{1}{C_{INT}} \quad (3)$$

With the model, the interface impact on device performance can be simulated as illustrated in Figure 4. The figure presents the SS with different interface thicknesses. It can be seen that the SS

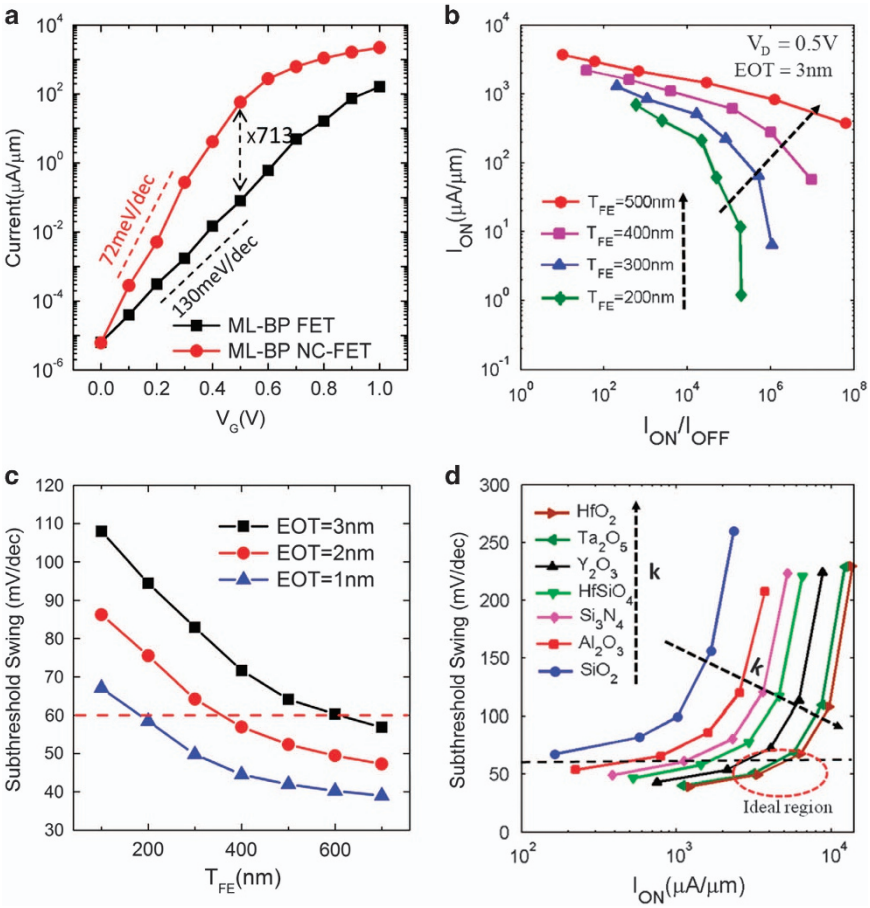

Figure 2. Device characteristics of FETs and NC-FETs. (**a**) I_D–V_G for 15 nm ML-BP NC-FETs and ML-BP FETs at $V_D = 0.5$ V and $T = 300$ K. The equivalent oxide thickness (EOT) is 3 nm and the thickness of ferroelectric layer is 400 nm. (**b**) $I_{ON} - I_{ON}/I_{OFF}$ for 15 nm ML-BP NC-FETs with different ferroelectric layer thickness (T_{FE}) and 3 nm EOT at $V_D = 0.5$ V and $T = 300$ K. (**c**) Subthreshold swing (SS) as the change of ferroelectric layer thickness for 15 nm ML-BP NC-FETs with different EOT at $V_D = 0.5$ V and $T = 300$ K. (**d**) SS versus I_{ON} of ML-BP NC-FETs with 400 nm ferroelectric layer, 3 nm insulator layer and different gate insulator materials with V_G window set at the supply voltage $V_D = 0.5$ V.

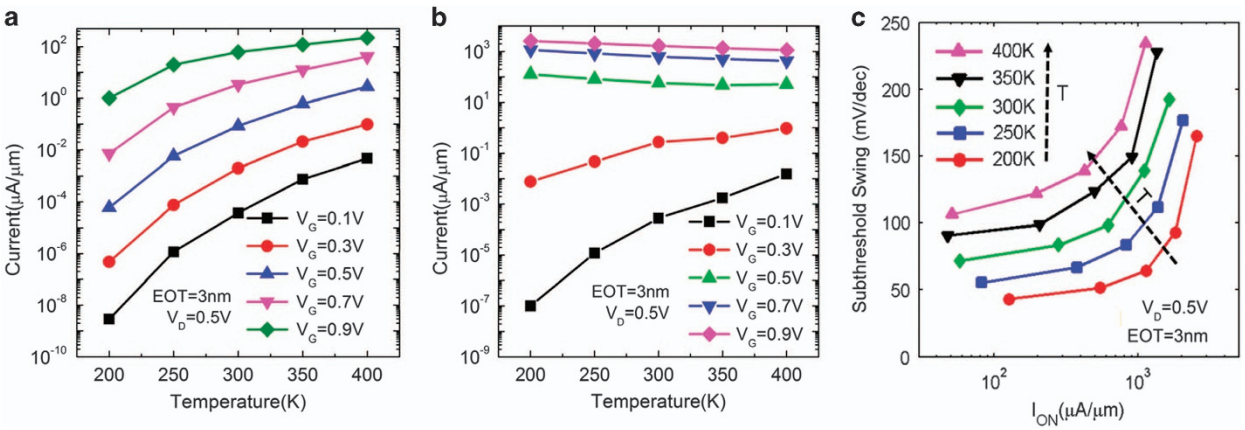

Figure 3. I_D as a function of temperature (T) for (**a**) 15 nm ML-BP FETs with 3 nm EOT and (**b**) 15 nm ML-BP NC-FETs with 400 nm ferroelectric layer and 3 nm EOT at different gate voltages. (**c**) SS versus I_{ON} of ML-BP NC-FETs with 400 nm ferroelectric layer and 3 nm EOT at different temperatures.

increases linearly with the thickness of the interface layer. Due to the existence of the interface layer, the effective thickness of FE layer is reduced and the amplification of FE layer is degraded. So, it is important to reduce the thickness of the interface layer to realise NC-FETs experimentally.

At last, we studied the scaling behaviour of NC-FETs and estimated the device performance for HP applications from ITRS 2013. The simulated channel length ranges from 5 to 15 nm. Figure 5a,b shows drain current of ML-BP FETs and ML-BP NC-FETs as a function of the gate voltage with a fixed $V_D = 0.5$ V,

respectively. I_D decreases with the increasing channel length L_C for the two kinds of devices, and for NC-FETs current becomes nearly independent of channel length for $V_G > 0.7$ V. SS decreases fast when the channel length increases as shown in Figure 5c and SS of ML-BP NC-FETs can be smaller than the 60 mV per decade limit. It has been shown that the ballistic performance of ML-BP FETs can meet the ITRS requirements for HP logic applications in 10 years horizon.[20] In ideal conditions, NC-FETs have better gate control compared with the FETs due to the amplification of FE layer. Hence, ML-BP NC-FETs are also suitable for logic applications. For lower-power consumption, reducing the supply voltage is critical, which determines the dynamic and static power dissipation. Figure 6 shows I_D–V_G characteristics for ML-BP NC-FETs and ML-BP FETs at different supply voltages. For ML-BP FETs, when V_D decreases from 0.69 to 0.3 V, the drain current drops clearly. Therefore, in FETs lowering the supply voltage is not an effective method to reduce the power dissipation because a reasonable-driven current cannot be kept. In NC-FETs, the control voltage can be amplified by the FE layer. Even though the supply voltage is reduced to 0.3 V, ML-BP NC-FETs can obtain good device performance than ML-BP FETs as shown in Figure 6. SS reaches 53 mV per decade in NC-FETs with 400 nm FE layer and can be further reduced to 27 mV per decade in NC-FETs with 600 nm FE layer. In Table 1, performance metrics of ML-BP NC-FETs with 400 nm FE layer and ML-BP FETs are compared with the requirements of ITRS 2013 for HP applications.[21] The off-state current is fixed at 0.1 μA/μm and the gate voltage windows are set to be equal to the value of bias voltage: $V_G^{ON} - V_G^{OFF} = V_D$. The intrinsic delay is computed as $\tau = (Q_{ON} - Q_{OFF})/I_D$ and the power delay product (PDP) per device width is calculated as $PDP = (Q_{ON} - Q_{OFF})V_D$. The two compared devices can meet technique requirements for HP applications of ITRS 2013 for the year 2024. In NC-FETs, PDP is effectively reduced and only 44% of that of FETs. Due to the low on-state current, the intrinsic delay is longer than that of ML BP FETs but still lower than the requirement of ITRS 2013.

DISCUSSION

Compared with the classical FETs, the NC-FETs have an additional FE layer deposited on the metal gate as shown in Figure1a. Therefore, the transport mechanism of NC-FETs is the same as that of FETs, and the NC-FET device can be viewed as a FET connected to a gate voltage 'amplifier'. The electrostatics due to the gate of NC-FETs can be roughly described by the capacitor divider model[4] of Figure1b where C_{FE}, C_{INS1} and C_B are capacitors due to the FE layer, the insulator layer and the body structure that includes the channel and the

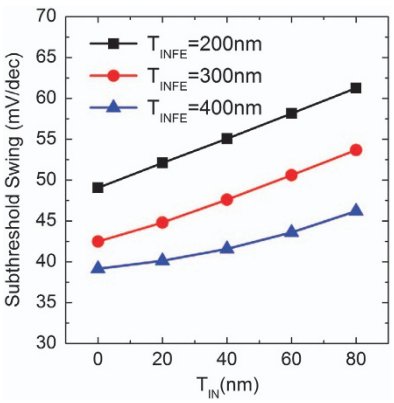

Figure 4. SS as a function of interface layer thickness (T_{IN}) for 15 nm ML-BP NC-FETs with 3 nm HfO_2 insulator layer and 400 nm ferroelectric layer at $V_D = 0.5$ V. $T_{INFE} = T_{IN} + T_{FE}$, where T_{FE} is effective ferroelectric layer thickness.

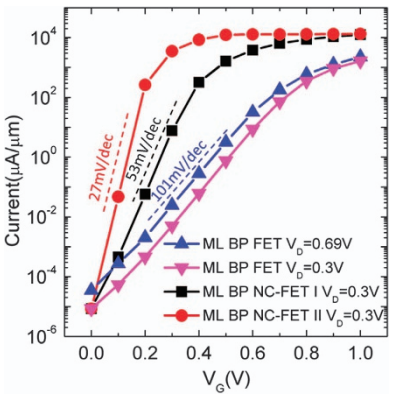

Figure 6. I_D–V_G for ML-BP NC-FETs and ML-BP FETs with 3 nm HfO_2 insulator layer and 7.3 nm channel. NC-FETs I and NC- FETs II have 400 and 600 nm ferroelectric layer, respectively.

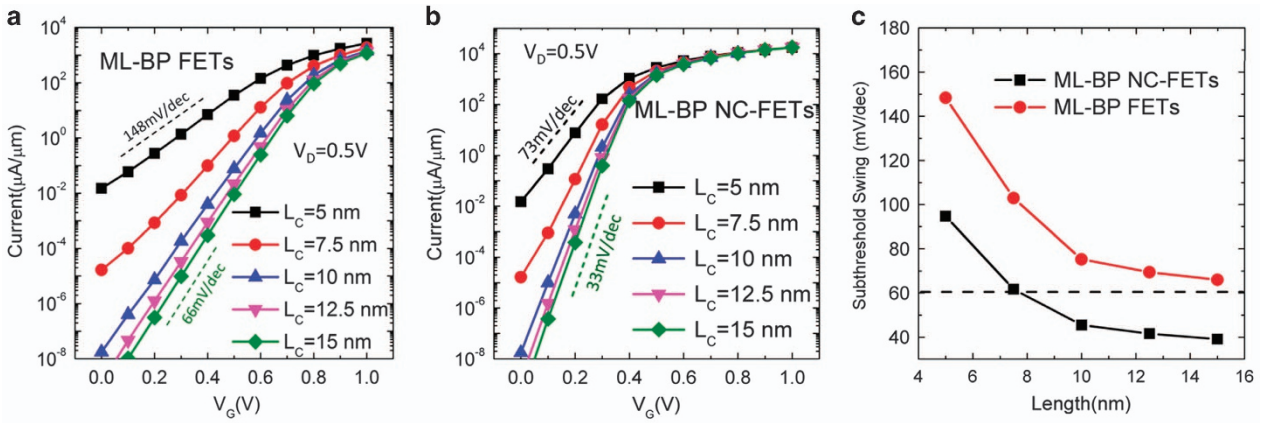

Figure 5. The scaling behaviour of NC-FETs. (**a**) I_D–V_G for ML-BP FETs with 3 nm HfO_2 insulator layer and different channel lengths (L_C) at $V_D = 0.5$ V and $T = 300$ K. (**b**) I_D–V_G for ML-BP NC-FETs with 400 nm ferroelectric layer, 3 nm HfO_2 insulator layer and different channel lengths at $V_D = 0.5$ V and $T = 300$ K. (**c**) SS as a function of channel length of 15 nm ML-BP FETs and ML-BP NC-FETs with 400 nm ferroelectric layer at $V_D = 0.5$ V and $T = 300$ K.

Table 1. Performance metrics of ML-BP NC-FETs with 400 nm ferroelectric layer, DG ML-BP FETs and the ITRS requirements for high-performance applications in the 2024 horizon

	Node 2024	*NC-FETs*	*DG FETs*
L_G (nm)	7.3	7.3	7.3
V_D (V)	0.69	0.3	0.69
EOT (nm)	0.49	0.49	0.49
I_{OFF} (μA/μm)	0.1	0.1	0.1
I_{ON} (μA/μm)	1170	1828	2798
τ (ps)	0.451	0.044	0.028
PDP (fJ/μm)	0.36	0.024	0.055

Compared with DG FETs, NC-FETs can work at lower driven voltage $V_D = 0.3$ V and power consumption can be effectively reduced. A fixed V_G window equals to the power supply voltage V_D.
Abbreviations: DG, double gate; EOT, equivalent oxide thickness; ITRS, International Technology Roadmap; ML-BP, monolayer black phosphorus; NC-FET, negative capacitance field effect transistor; PDP, power delay product.

substrate. The gate control can be quantified by the SS which is defined as:[4]

$$SS \equiv \frac{\partial V_G}{\partial(\log_{10} I_D)} = \frac{\partial \psi_s}{\partial(\log_{10} I_D)} \frac{\partial V_G}{\partial \psi_s} \equiv n \times m \quad (4)$$

where the last equality defines the parameters n and m: the parameter n is related to the transport mechanism (called the transport factor) and the parameter m is determined by the device structure (called the body factor). The quantity ψ_s is the surface potential in the transistor channel as shown in Figure 1b. In a classical FET, the current is mainly composed of thermionic carriers over the potential barrier that follows the Boltzmann distribution, hence the transport factor n is a constant of 60 mV per decade at room temperature. The ultimate value of SS therefore depends on the body-factor m, which turns out to be always greater than unity due to the positive capacitances in the capacitor divider model if there is no FE layer in Figure1b. Hence for traditional FETs, SS is always greater than the 60 mV per decade limit.

By adding a FE layer, it is possible to reduce the body-factor m smaller than unity, so that SS can be made smaller than 60 mV per decade. Using the capacitor divider model again, the body-factor m can be expressed as:

$$m = \frac{\partial V_G}{\partial \psi_s} = 1 + \frac{C_B(C_{INS1} + C_{FE})}{C_{INS1} C_{FE}}. \quad (5)$$

From this we obtain $0 < m < 1$ if the following inequality holds:[7]

$$C_{MOS} = \frac{C_{INS1} C_B}{C_{INS1} + C_B} < -C_{FE} < C_{INS1} \quad (6)$$

where C_{MOS} is the capacitance of the underlying transistor. Equation (3) can be used as the design rule for NC-FETs.

From Equation (2), noting that since C_{FE} is negative, the body-factor m can be further decreased by increasing C_B. Compared with bulk silicon or even ultrathin body FETs, 2D materials can reach larger capacitance C_B due to atomically thin structures. Therefore the idea of NC-FETs can in principle be better realised in 2D channels. In the rest of the paper, we focus on the ML-BP material as the channel and quantitatively investigate the device properties of the 2D NC-FETs.

In this work, monolayer BP is applied as the channel material of NC-FETs. Other 2D materials such as layered TMDCs can also be used in NC-FETs for achieving good gate control. Layered BP film undergoes degradation in ambient air, which will likely degrade the performance of BP devices. Recently, various methods have been proposed to keep a clean BP film, such as encapsulation by AO_x layers,[27] covering by copolymer capping layer,[28] graphene and hexagonal boron nitride.[29] It is theoretically predicted that monolayer BP can be well maintained on the HfO_2 (111) surface[30] and H-passivated Al_2O_3.[31] Further progress should make it feasible to manage the degradation of BP film for real device applications. The device performance of NC-FETs greatly depends on properties of the channel material and FE layer as well as the device structure. 2D materials with high carrier mobility and reasonable band gap are beneficial for achieving higher on-current and on/off current ratio of NC-FETs. The amplification effect of FE layer can be optimised by adjusting the FE material parameters such as increasing the FE layer thickness and coercive voltage, and decreasing the remnant polarisation.[32]

CONCLUSION

Negative capacitance transistor based on 2D material—monolayer black phosphorus is proposed, which combines 2D material—ML-BP with sub-60 mV per decade operation. By using 2D material amplification effect of FE layer can be enhanced. We show that the combination of ML-BP and negative capacitance transistor can effectively reduce subthreshold swing due to the atomistic thin structure and the amplification effect of the FE layer. The new device can achieve a subthreshold swing as small as 27 mV per decade at $V_D = 0.3$ V. Device performance of ML-BP NC-FETs can be optimised by increasing the thickness of FE layer and using thinner or high-k insulate layer. ML-BP NC-FETs show different temperature dependence from MOSFET and can reach higher on current at low temperature due to the polarisation of FE layer. By considering the metal–FE interface layer, our calculation shows that the device performance is degraded by the interface. Compared with the ITRS 2013 requirements, ML-BP NC-FETs can fulfil the ITRS requirements for HP applications in 2024 and the power delay product per device width can be effectively reduced. Therefore, the proposed ML-BP NC-FETs should be very helpful for designing low-power circuits.

MATERIALS AND METHODS

Figure 1 schematically shows the device structure of ML-BP NC-FETs. A $SrBi_2Nb_2O_9$ FE layer is deposited on the metallic gate of the underlying transistor. In our simulation hysteretic effect is neglected, corresponding to a relatively thick FE. In the underlying MOSFET, ML-BP is used as the channel material. The source/drain of FET is n-type doped with a density of $7.0 \times 10^{13} cm^{-2}$, and the channel under the gate is intrinsic. The length of source or drain is 10 nm and the channel length ranges from 5 to 15 nm. The ballistic transport of ML-BP is calculated by self-consistently solving the Schrodinger and Poisson equations within nonequilibrium Green's function formalism. A four band tight binding Hamiltonian is used to describe the ML-BP material and can well fit the low-energy band structures.[33] The amplifying effect of the FE layer is calculated by solving the 1D Landau model.[4] Landau parameters of $SrBi_2Nb_2O_9$ and temperature dependence model are taken from ref. 22 The effect of the electrode–FE interface is described by the interface capacitance model,[26] which is coupled with the 1D Landau model to study interface effect in ML-BP NC-FETs.

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CONTRIBUTIONS

F.L. and Y.Z. conceived and designed the research. F.L. and Y.Z. contribute to this work equally. Y.Z. developed the capacitor model. F.L. performed the calculations. Y.W. and X.L. assisted in simulation and physical analysis. J.W. and H.G. participated in the explanation of results. F.L., Y.Z., J.W. and H.G. wrote the manuscript.

COMPETING INTERESTS

The authors declare no conflict of interest.

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