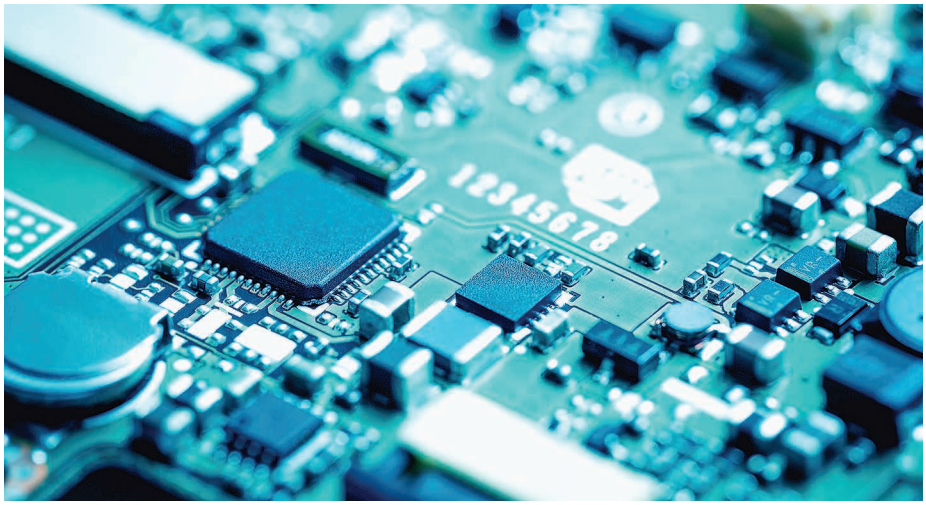
Moore's deviation

The pursuit of the 5-nm node continues amid increasing doubts over the long-term relevance of Moore's law.



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The inventions of the transistor and the integrated circuit set in motion the extraordinary progress of computing performance that has kept the number of transistors on a chip doubling every two years without increasing the price. Ever since the trend best known as Moore's law was postulated, it has served as a guide to identify long-term R&D targets for the semiconductor industry. For years, chip makers have been consistently able to figure out new ways to shrink the transistor size in time for the next node to hit the market. The downscaling of transistors has come a long way from the very first commercial 10-μm technology to the 10-nm node that is currently being introduced. These days, however, keeping pace with the traditional two-year cadence has become an increasingly challenging endeavour. This fact was fully acknowledged in the final International Technology Roadmap for Semiconductors[1] (ITRS), in 2015, which predicted that transistors will reach their minimal limit soon after 2021.

Although 7-nm FinFET devices are expected to ship sometime in 2018, the foundries face an uphill struggle to find cost-effective engineering solutions for the next 5-nm node as the existing transistor architecture is nearing the end of its scaling lifespan. The FinFET, featured in every modern microprocessor, was originally designed to mitigate leakage-current issues associated with a planar FET geometry. This device has 3D silicon structures that jut out from the substrate like a fin, hence the name. As the fins continue to get thinner, the technology is expected to hit another wall at a width of 5 nm due to channel size variations and potential mobility loss. Hence, to keep Moore's law going, new engineering strategies are urgently needed.

For chips to get denser, the manufacturers may still try to extend FinFET to 5 nm or, building upon the existing technology, switch to gate-all-around (GAA) FETs. In terms of its geometry, a GAA FET closely resembles a FinFET except that the gate surrounds the channel region on all sides. Owning to these similarities, the GAA FET is considered a likely candidate for the 5-nm node, which, according to some predictions, may be extended further down to 3 nm. This scenario looks very plausible judging by the recent IBM demonstration[2] of a test silicon chip containing 30 billion horizontal GAA FETs. This technological marvel has a 40% performance edge over commercial 10-nm chips and offers 75% lower power consumption at the same level of performance. Besides, as opposed to 7-nm technology the newly presented chip accommodates a whopping 10 billion additional transistors. Each device contains a stack of three silicon nanosheets between the source and drain electrodes wrapped in the gate. Analogous to 7-nm IBM transistors, the fabrication process of a GAA FET with its tiny features requires an extra step that involves extreme ultraviolet (EUV) lithography. Despite the remarkable resolution limit of less than 4 nm, the deployment of EUV for volume manufacturing has been postponed for years due to its extreme complexity, high implementation cost and multiple reliability issues. Therefore it is no secret that the 5-nm node will cost manufacturers dearly, making the future of transistor downscaling economically irrelevant and potentially putting the technology out of reach for a large number of consumer applications. Economic arguments aside, vertical transistors with nanowire channels could provide another way of cramming more transistors onto a chip similar to the Samsung 3D V-NAND memory[3]. But then again, opting for vertical transistors won't offer any long-term relief for the chip makers, as according to the same ITRS the 3D technology will run out of steam by 2024[1]. The reason is that existing chip-cooling solutions will no longer be sufficient to tackle ever-increasing power dissipation densities. Another critical issue that urgently needs an effective engineering solution is the so-called interconnect bottleneck that comes as a result of tighter packing of the components on a microprocessor and could severely impair the speed of computing. Finally, looking for new channel materials instead of changing a transistor design is also under consideration. To that end, semiconductors such as III–V and germanium are being considered as the most promising silicon substitutes in terms of mobility.

With all these challenges in mind, the manufacturers are clearly not in a rush to introduce another node or switch to an alternative transistor type. Clinging on to the purely economic yet short-lived strategy of further FinFET downscaling would help chip makers squeeze every last drop out of the existing technology and justify billions of dollars of investment. Yet, the future of the 5-nm node and beyond is far from certain, especially in the absence of one clear transistor contender and other much-needed cost-effective technological innovations. After decades of the semiconductor industry faithfully living by the golden rule — smaller, faster, cheaper — the time has come to re-evaluate its capacity for fabricating ever-smaller features at ever-increasing densities. After all, it doesn't really matter whether Moore's law lives or dies as long as consumer needs are satisfied at a reasonable cost. ❐

References

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