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# Graphene radio frequency receiver integrated circuit

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Graphene has attracted much interest as a future channel material in radio frequency electronics because of its superior electrical properties. Fabrication of a graphene integrated circuit without significantly degrading transistor performance has proven to be challenging, posing one of the major bottlenecks to compete with existing technologies. Here we present a fabrication method fully preserving graphene transistor quality, demonstrated with the implementation of a high-performance three-stage graphene integrated circuit. The circuit operates as a radio frequency receiver performing signal amplification, filtering and down-conversion mixing. All circuit components are integrated into 0.6 mm<sup>2</sup> area and fabricated on 200 mm silicon wafers, showing the unprecedented graphene circuit complexity and silicon complementary metal-oxide-semiconductor process compatibility. The demonstrated circuit performance allow us to use graphene integrated circuit to perform practical wireless communication functions, receiving and restoring digital text transmitted on a 4.3-GHz carrier signal.

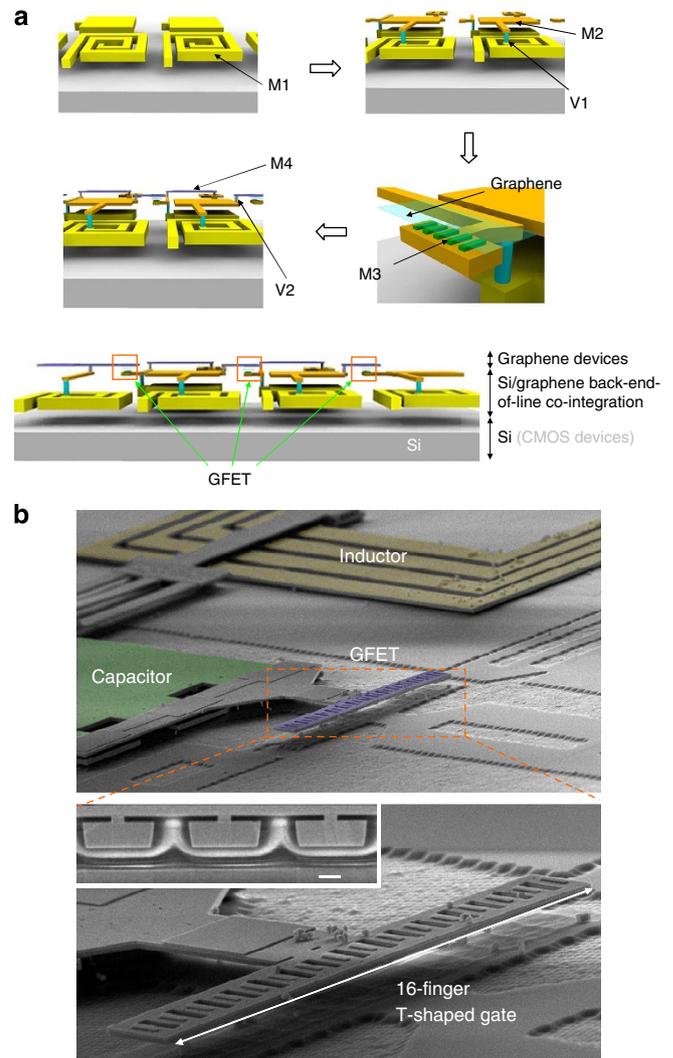
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With recent developments in graphene field-effect transistors (GFETs) showing intrinsic unity current gain frequencies ( $f_T$ ) higher than 400 GHz (ref. 1), along with theoretical work projecting operation exceeding 500 GHz (ref. 2), graphene shows great promise in radio frequency (RF) applications. The rapid advances in graphene transistor performances,  $f_T$  and maximum oscillation frequency ( $f_{MAX}$ ), came from all aspects of the device, including improved starting graphene materials<sup>3</sup>, better gate dielectrics<sup>4–6</sup>, improved contact resistance<sup>7</sup>, new device architectures<sup>8,9</sup> and aggressive channel length scaling<sup>1,10</sup>. On the other hand, the pace of the development of graphene RF circuits seems significantly slower, and raises the question about the true feasibility of using graphene in modern communication systems. Most graphene circuits demonstrated today are arguably the extension of the study of a transistor itself. High-performance discrete passive components have been connected to GFET externally at the equipment level, and these circuits are limited to single-transistor designs. Demonstrations using this approach have shown several promising GHz functions such as voltage amplification<sup>11</sup>, frequency multiplication<sup>12,13</sup> and signal mixing<sup>7,14</sup>. However, to compete with existing technologies, particularly silicon, requires that all active and passive components be monolithically integrated onto single chip for not only the small circuit footprint and low cost but also high circuit complexity and advanced system functionality. A millimetre-wave mixer integrating exfoliated graphene and microstrip technology has recently been demonstrated<sup>15</sup>. The circuit fabrication, however, requires more exotic processes such as substrate thinning and through-substrate via etching. For the large-scale synthesized graphene, perhaps the best attempt displayed to date is a single-stage mixer integrated circuit (IC) built by small-piece, offline-type processes<sup>16</sup>. This proof-of-concept IC consists of only one transistor, fabricated by a conventional process flow, that is, the active device was first constructed, followed by a series of back-end-of-line (BEOL) processes to complete the circuit interconnect and passive components. Because of the delicacy of graphene, resulting from its single atomic layer nature and weak adhesion between graphene and other materials, these BEOL processes inevitably deteriorate GFET quality, which is evident from much worse device performance in the IC compared with stand-alone GFETs using similar substrates<sup>3,4,10,17</sup>. This fundamental process compatibility issue apparently hinders the progress of graphene RF research.

Here, we present the first multi-stage graphene RF IC fabricated in a standard silicon fab. The device integrity is fully preserved and the circuit performance is confirmed by the demonstration of successful receiving and recovering of digital text carried on a GHz signal. The device degradation issue is overcome by completely reversing the conventional fabrication flow, where all passive components together with device gates are first built on 8-inch silicon wafers before the graphene films, grown by chemical vapour deposition (CVD) methods<sup>18</sup>, are transferred. The demonstrated conversion gain at the same local oscillator (LO) input power is  $\sim 10,000\times$  better than previously reported graphene IC<sup>16</sup>. This novel integration scheme can also be applied to any channel materials that can be transferred, such as carbon nanotubes<sup>19</sup> or other two-dimensional nanomaterials<sup>20,21</sup>.

## Results

**Passive-first active-last fabrication flow.** Figure 1a shows schematics of the simplified fabrication flow, which depicts the establishment of the passive-first active-last integration scheme. Inductors and bottom plate of capacitors were first fabricated at M1 metal level using single Cu damascene process. To get



**Figure 1 | Fabrication and architecture of graphene receiver IC.**

(a) Schematic of the passive-first active-last process flow showing how the IC fabrication can be integrated into standard Si BEOL process. Four metal levels (M1–M4) are required to complete the circuit. (b) Tilted view scanning electron microscopic (SEM) image revealing the integration of key components in IC with enlarged view showing the advanced gate structure of the graphene field-effect transistors (GFET). Inset image shows cross-sectional SEM of embedded T-shaped gate. Scale bar, 500 nm.

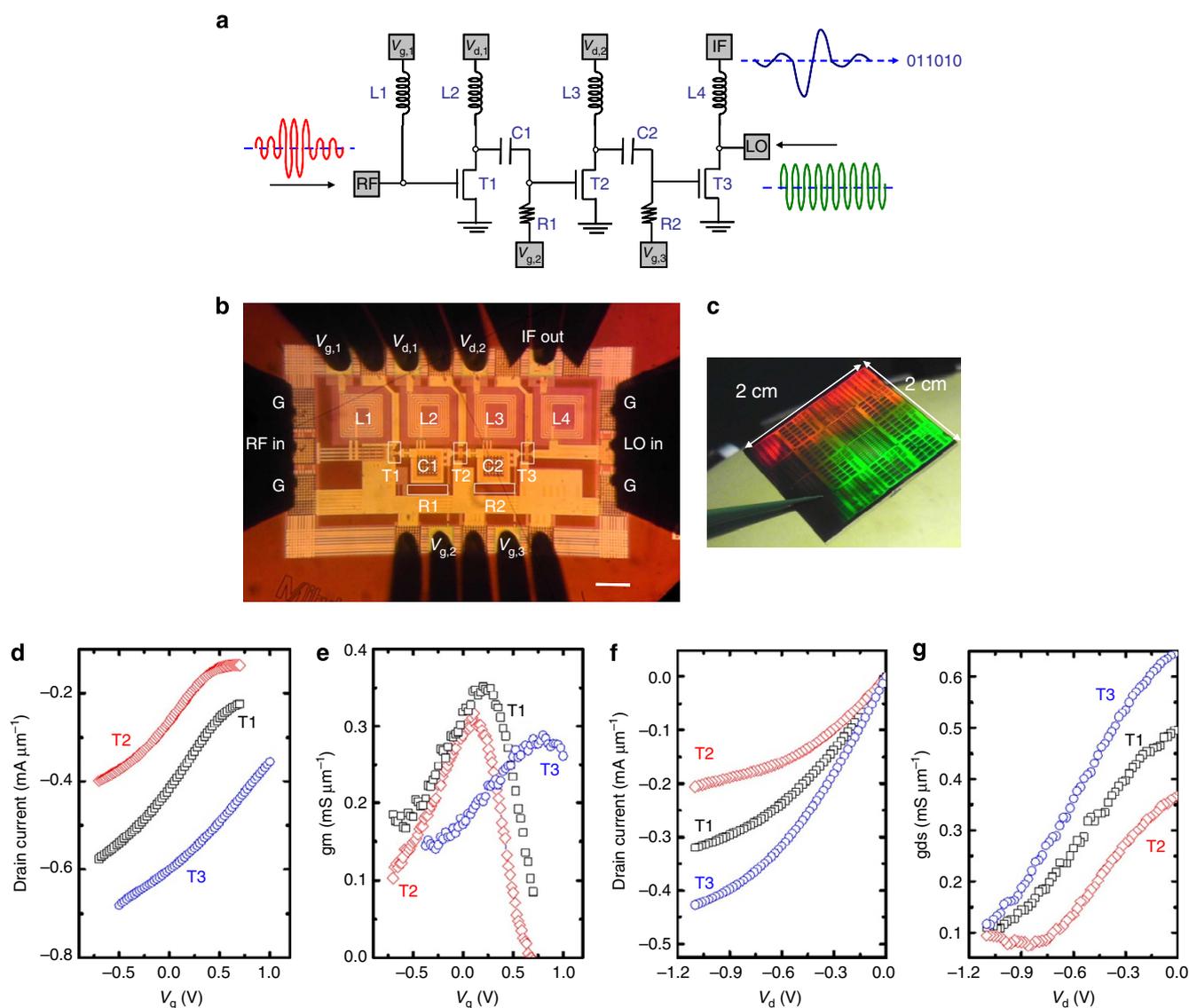
high-quality factor ( $Q$ ) of the inductors, M1 was thicker than  $1\ \mu\text{m}$ , and can be the same top metal level in standard Si complementary metal–oxide–semiconductor (CMOS) chips for global power distribution. The fabricated inductors showed inductances matching the designed values (Supplementary Table 1) with  $Q > 8$  (Supplementary Fig. 1). The M2 metal level formed by the similar Cu damascene process served as the top plate of capacitors as well as the bottom (wide) part of the embedded T-shaped gate. The M3 metal lines were then patterned to form the top part of the T-shaped gate, where the width of M3 lines defined the transistor's channel length. After the T-gate formation, atomic layer deposition (ALD) was used to deposit gate dielectric of 10 nm  $\text{Al}_2\text{O}_3$  followed by CVD graphene transfer and patterning. The mobility of the CVD graphene is around  $2,000\text{--}2,500\ \text{cm}^2\ (\text{Vs})^{-1}$  at the carrier density of  $2 \times 10^{12}\ \text{cm}^{-2}$  (Supplementary Fig. 2). No seed layers that are typically needed for promoting the nucleation of gate dielectric on graphene were required, resulting in high gate dielectric quality and the potential for future scaling.

As the last step, the M4 metal level comprising Pd/Au stack was deposited to form resistors and also device source/drain contacts.

To illustrate the integration architecture, a tilted view scanning electron microscopic image capturing key circuit components from the wafer completing the gate fabrication, before graphene transfer, is shown in Fig. 1b. All the inter-metal dielectrics as well as gate dielectric were stripped off to reveal the underlying structure. The unique embedded T-shaped gate structure in Fig. 1b, together with the multiple-finger design, provides very low gate resistance while maintaining a short channel length, leading to notably improved  $f_{MAX}$  verified from stand-alone RF transistors built on the same chip (Supplementary Fig. 3)<sup>22</sup>.

The IC consists of 11 components including 3 GFETs, 4 inductors, 2 capacitors and 2 resistors (Fig. 2a,b). The circuit is designed as an RF receiver front-end comprising three stages. Each stage is connected to the next through capacitive coupling; thus, the gate bias ( $V_g$ ) of each stage can be individually adjusted to optimize circuit performance. The first two stages are designed

as band-pass amplifiers, providing amplification and filtering of received RF signal. The third stage performs mixing with LO signal that down-converts the GHz RF signal to much lower intermediate frequency (IF) in the MHz range. Although the ambipolar nature of graphene enables several new circuit designs<sup>12,23</sup>, including subharmonic mixer operation<sup>14</sup>, these mixers require the Dirac point close to zero gate bias with highly symmetric electron and hole transfer curves for the best performance, and relatively high levels of LO power. In our design, a fundamental drain-pumped mixer is employed since it leads to better performance based on the characteristics of our graphene transistors (shown in Fig. 2d–g), and results in low LO power requirements (<0 dBm). Inductor L4, connected at the drain of mixing FET, serves a double purpose: it resonates the drain capacitance of transistor T3 to provide a large LO voltage swing at the drain terminal, and it attenuates the LO signal leakage towards the IF port. The photo of a fabricated chip in Fig. 2c exhibits arrays of graphene ICs, transistors for



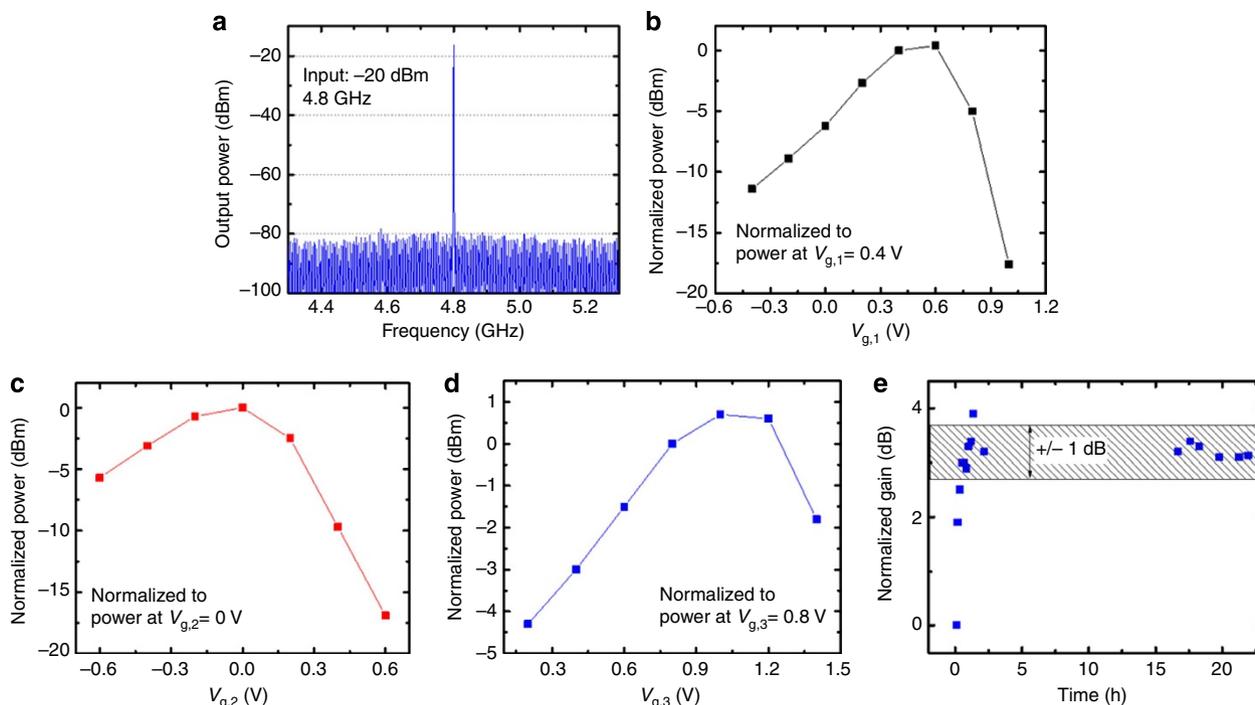
**Figure 2 | Circuit diagram and device DC performance.** (a) Circuit schematic of three-stage graphene receiver IC comprising 11 active and passive components. (b) Optical micrograph of an IC under testing. The circuit has the dimension of  $1,020 \times 600 \mu\text{m}^2$ . Scale bar,  $100 \mu\text{m}$ . (c) Photo of a fully processed graphene IC chip. (d) Drain currents as a function of gate biases for three transistors in one circuit and (e) their width normalized transconductances. The drain biases were  $-1\text{V}$ . (f) Drain currents as a function of drain biases and (g) width normalized output conductances from the same devices. The gate biases were  $0.25\text{V}$  for both devices T1 and T2, and  $0.75\text{V}$  for device T3.

S-parameter characterization and process monitor structures (Supplementary Fig. 4).

One key feature of this process flow is to fabricate GFET as the last step, which prevents possible graphene damage during harsh BEOL processes (for example, chemical mechanical polishing and Cu electroplating). This advantage can be clearly seen from direct current performance of three GFETs of gate lengths of 900 nm and device widths of 12  $\mu\text{m}$  in one circuit measured after the full circuit has been built, as shown in Fig. 2, where Fig. 2d,e and Fig. 2f,g present transfer and output characteristics, respectively. At  $-1\text{ V}$  drain bias ( $V_d$ ), these devices exhibit peak transconductance ( $g_m$ ) larger than  $0.3\text{ mS}\mu\text{m}^{-1}$ , on par with state-of-the-art GFETs with similar device dimensions and about 450% better than the device in the previous graphene IC report despite a higher  $V_d$  (1.6 V) was used<sup>16</sup>. More importantly, the devices show clear drain current saturation (verified by low output conductance ( $g_{ds}$ ) in Fig. 2g), leading to high intrinsic gain ( $g_m g_{ds}^{-1}$ ) of about 2–4.5. We would like to point out that the gapless band structure in graphene typically causes the weaker saturation of the drain current in GFET compared with other semiconductor devices with a bandgap<sup>24</sup>. We have previously shown that by employing a very thin gate dielectric (equivalent oxide thickness less than 2 nm), full drain current saturation ( $g_{ds}=0$ ) can be achieved in GFETs<sup>25</sup>. Therefore, a higher gain performance can be expected by continuously improving the gate dielectric quality in our IC fabrication process. At 1 V drain bias,  $f_T$  and  $f_{MAX}$  ranging from 8 to 10 GHz and from 8.5 to 13.5 GHz, respectively, were measured from stand-alone RF transistors with the same gate length. It is noteworthy that the current chips have not gone through the last passivation step. Several reports have shown that various dielectric films can be directly deposited on graphene, such as  $\text{Si}_3\text{N}_4$  deposited by plasma-enhanced CVD<sup>26</sup> or a  $\text{NO}_2$  and  $\text{HfO}_2$  stack deposited by ALD<sup>27</sup>, which can provide sufficient chip protection.

**IC performance.** Before testing the IC as an RF receiver, the successful circuit integration was verified by measuring it as an RF amplifier driving a 50- $\Omega$  load, a standard impedance in RF systems. A small-signal power gain of 10 dB at 1 GHz has been previously demonstrated with a discrete graphene transistor<sup>28</sup>. This circuit function in our IC can be achieved by simply adjusting gate biases of transistors to their highest  $g_m$  points, and replacing the IF output in Fig. 2a with the third-stage drain bias. Figure 3a shows that the IC exhibits +4 dB power gain, which is the first graphene IC able to perform amplification when loaded with 50  $\Omega$  impedance. This performance is in good agreement with circuit simulations performed using the measured values of individual components (Supplementary Fig. 5, Supplementary Note 1). To demonstrate that each of the three active stages is operational, Fig. 3b–d shows the normalized gain as a function of  $V_g$  in one stage while keeping  $V_g$  of other two stages constant. The gain of each stage can be independently controlled, confirming the correct functions from all active and passive components in each stage. In addition, the stability of the graphene IC was tested by applying high drain current stress and monitoring the gain variation continuously (Fig. 3e). The initial performance improvement is attributed to the current-induced annealing effect that removes contamination of graphene<sup>29</sup>. Once transistors become stabilized, the circuit exhibits less than  $\pm 1\text{ dB}$  variation during  $>20\text{ h}$  testing period, suggesting excellent stability and reliability.

The circuit was measured in receiver mode, with an LO signal applied at the drain of T3 and IF output measured after L4. The measured output spectrum is shown in Fig. 4a. The conversion gain of the circuit with 4.3 GHz RF input signal is  $-10\text{ dB}$  with a low LO input power ( $P_{LO}$ ) of  $-2\text{ dBm}$ , presenting 50 times higher conversion gain with 200 times smaller LO power compared with previously reported graphene IC (Supplementary Table 2)<sup>16</sup>. Such low  $P_{LO}$  is important to effectively prevent LO



**Figure 3 | Graphene IC measured as RF amplifier.** (a) Output spectrum of the IC with 900 nm gate length under  $-1.6\text{ V}$   $V_d$  with input power of  $-20\text{ dBm}$  at 4.8 GHz. (b) Normalized amplifier output power as a function of the first-stage gate bias ( $V_{g,1}$ ). The second-stage gate bias ( $V_{g,2}$ ) was kept at  $-0.13\text{ V}$  and the third-stage gate bias ( $V_{g,3}$ ) was kept at  $0.99\text{ V}$ . (c) Normalized amplifier output power as a function of  $V_{g,2}$ .  $V_{g,1} = 0.45\text{ V}$  and  $V_{g,3} = 0.99\text{ V}$ . (d) Normalized amplifier output power as a function of  $V_{g,3}$ .  $V_{g,1} = 0.45\text{ V}$  and  $V_{g,2} = -0.13\text{ V}$ . (e) Variation of amplifier gain during bias stress test for over 22 h. The circuit was measured in air.

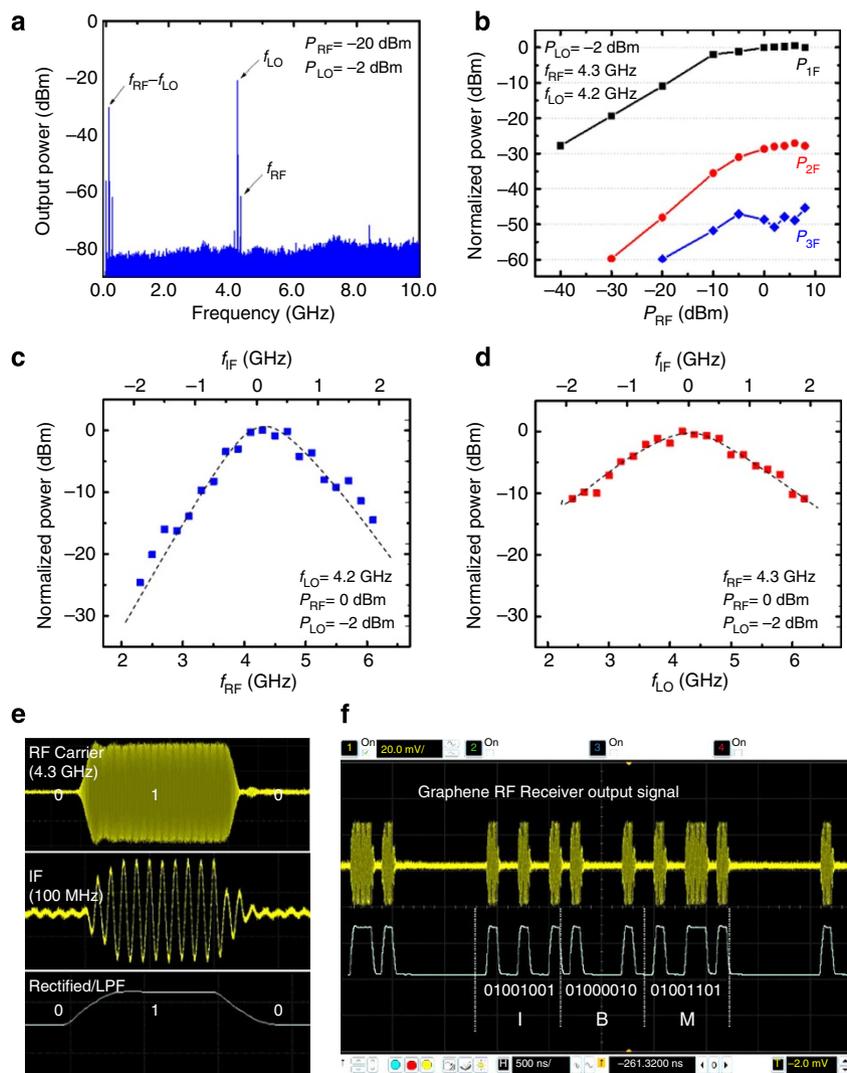
from leaking into the final IF output. The measured conversion gain as a function of  $P_{LO}$  is also shown in Supplementary Fig. 6. With drain biases of  $-1.5$  V, the whole three-stage IC consumes less than 20 mW power, 600% lower than single-stage graphene IC in ref. 16. Figure 4b shows the measured receiver output tones ( $P_{1F}$ ,  $P_{2F}$ ,  $P_{3F}$ ) as a function of input RF power ( $P_{RF}$ ); low RF harmonic distortion ( $P_{1F}-P_{2F} \sim 30$  dB for  $P_{RF} = 0$  dBm) indicates good circuit linearity. The circuit is designed to band-pass filter the RF input signal before entering the mixer to improve the data quality by rejecting unwanted signals outside the carrier frequency band. The effective RF input filtering can be seen from the sharp frequency response in Fig. 4c ( $\sim 1$  GHz of 3-dB bandwidth). The receiver conversion gain is also measured as a function of the LO frequency (Fig. 4d).

To best demonstrate the true functionality of the graphene IC, an RF carrier of 4.3 GHz was amplitude modulated with a bit stream and sent into the receiver to mimic the typical digital data transmitted via wireless carrier. Measured single bit waveforms in Fig. 4e show undistorted IF output signal from the receiver

without the aid of any additional signal amplification, suggesting that a high-quality receiver function has been achieved. The original binary code can then be easily recovered by rectification and low-pass filtering. Figure 4f further shows that bit stream comprising ASCII code of 'IBM' modulated at  $20$  Mb s $^{-1}$  is successfully received and demodulated. The modulation rate is limited by the test equipment, and not by the receiver IC.

**Discussion**

The demonstration of multifunctional RF ICs built with the graphene-last flow in Si fab clearly paves the way for seamless heterogenous three-dimensional (3D) system integration, where graphene IC's BEOL can be co-integrated with standard Si CMOS BEOL as illustrated in Fig. 1a. On the other hand, stacking conventional semiconductor layers such as Si or III-V into 3D system is rather complicated and costly, where challenges arise from high-temperature annealing processes (typically  $> 1,000$  °C) required for each active layer device formation that are not



**Figure 4 | Graphene IC measured as RF receiver.** (a) Output spectrum of graphene receiver with 900 nm gate length. RF input signal was  $-20$  dBm at 4.3 GHz and LO input signal was  $-2$  dBm at 4.2 GHz. Down converted IF output signal at 100 MHz ( $f_{IF} = f_{RF} - f_{LO}$ ) was  $-30$  dBm. (b) Normalized output power of the fundamental tone ( $P_{1F}$ ), the second harmonic ( $P_{2F}$ ) and the third harmonic ( $P_{3F}$ ) as a function of RF power ( $P_{RF}$ ), showing no gain compression up to  $-10$  dBm  $P_{RF}$ . (c) Normalized output power as a function of LO frequency. (d) Normalized output power as a function of RF. (e) Measured waveforms of RF input signal amplitude modulated at a rate of  $20$  Mb s $^{-1}$ , IF output signal and restored binary code after rectifying and low-pass filtering IF signal. (f) A screenshot of receiver output waveforms taken from the oscilloscope, with LO power of  $-2$  dBm at 4.2 GHz. The original bit stream comprising three letters (24 bits) was recovered by graphene receiver with very low distortion. The circuit was measured in air.

compatible to Cu BEOL technology<sup>30</sup>. Our entire IC fabrication flow does not require any process steps higher than 400 °C, making it an ideal candidate for monolithic 3D integration with Si CMOS backbone. Such integration concept fully utilizes the transfer property of graphene, and one can envision that high-performance graphene RF circuits will be directly built on top of high-density Si CMOS logic circuits to form an extremely low-cost, ultra-compact communication system.

## Methods

**CVD graphene growth and transfer.** The graphene growth was carried out in a 4-inch furnace, which can support up to 12 × 12 inch<sup>2</sup> graphene size. A Cu foil (99.99% from Kamis) was annealed at 1,050 °C for 5 min in 5 mTorr CH<sub>4</sub> for initial graphene island growth, and then annealed for 20 min in 75 mTorr CH<sub>4</sub> for graphene growth<sup>18</sup>. The graphene was transferred to a target substrate with typical wet transfer process. First, 150 nm thick PMMA was spin coated on the graphene/Cu foil sample (3,000 r.p.m. for 1 min). The polymethyl methacrylate (PMMA)/graphene/Cu foil sample was then floated on 1 M FeCl<sub>3</sub> to dissolve the Cu foil, followed by moving the remaining PMMA/graphene sample on 1 M HCl for rinsing away the residue of Cu etchant. Finally, the PMMA/graphene sample was scooped by a target substrate and then blown dry by pure nitrogen.

**Passive-first active-last process flow.** A total of nine lithography masks are required to complete the IC fabrication. In a 200-mm silicon fab, beginning with low-doped Si wafers with 2 μm thick silane oxide deposition at 400 °C, the wafer was then spin coated with photoresist and patterned using an ASML Deep ultra-violet stepper. High-power reactive ion etching (RIE) with a mixture of C<sub>4</sub>F<sub>8</sub> and Ar for 135 s was used to remove ≈ 1 μm SiO<sub>2</sub>, and the photoresist was stripped off in oxygen plasma. Physical vapour deposited liner consisting of TaN/Ta was adapted before the deposition of a thin Cu seed layer, which was followed by Cu electroplating and chemical mechanical polishing. After inspection of post-CMP patterns, low-stress CVD nitride (100 nm) and silane oxide (800 nm) were deposited. The measured capacitance of plate capacitors is 6.1 × 10<sup>3</sup> pF cm<sup>-2</sup>. Cu vias and following metal levels were fabricated using similar process steps with different dielectric thickness and etch time. Al<sub>2</sub>O<sub>3</sub> gate dielectric (100 Å) was then deposited at 250 °C using TMA and H<sub>2</sub>O in a Fiji ALD system to cover the whole wafer and an HBr-based RIE process was used to etch open the contact pad to the gate. After CVD-grown graphene was transferred, photoresist was again patterned in a DUV system and the exposed graphene area was etched away in a Unaxis RIE system with a 50-W plasma maintained by 30 s.c.c.m. O<sub>2</sub>. Photolithographic patterning was used to define source/drain electrodes and electron beam evaporation was used to sequentially deposit 0.2 nm Ti, 20 nm Pd and 30 nm Au followed by a lift-off process in resist stripper.

**IC measurement.** The LO signal was provided by a Wiltron 69047A signal generator, and the input RF signal was provided by a Rohde & Schwarz SMIQ06B signal generator, which could be 100% amplitude modulated to about 20 MHz by an external signal. The mixer and amplifier outputs were measured with an Agilent E4448A spectrum analyser. Losses due to bias tees, cables and probe resistance were calibrated using an on-wafer 'through' wire structure. Modulation of the input RF signal was performed by driving the RF signal generator amplitude modulation input with a data pattern stored on an Agilent 81133 pulse generator. The demodulated signal was observed on an Agilent DSA91204A real-time oscilloscope, which also performed the rectification and low-pass filtering to convert it to digital format.

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## Author contributions

S.-J.H. conceived and designed the experiments; A.V.G. and S.-J.H. designed the circuit; S.-J.H. developed the integration process and fabricated the circuit; S.O. synthesized CVD graphene; S.-J.H., A.V.G. and K.A.J. performed the device and circuit measurement and analysed the data; S.-J.H. wrote the manuscript. All authors discussed the results and commented on the manuscript.

## Additional information

**Supplementary Information** accompanies this paper at <http://www.nature.com/naturecommunications>

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