

ARTICLE

Fabrication of 3D air-core MEMS inductors for very-high-frequency power conversions

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We report a fabrication technology for 3D air-core inductors for small footprint and very-high-frequency power conversions. Our process is scalable and highly generic for fabricating inductors with a wide range of geometries and core shapes. We demonstrate spiral, solenoid, and toroidal inductors, a toroidal transformer and inductor with advanced geometries that cannot be produced by wire winding technology. The inductors are embedded in a silicon substrate and consist of through-silicon vias and suspended windings. The inductors fabricated with 20 and 25 turns and 280–350 μm heights on 4–16 mm^2 footprints have an inductance from 34.2 to 44.6 nH and a quality factor from 10 to 13 at frequencies ranging from 30 to 72 MHz. The air-core inductors show threefold lower parasitic capacitance and up to a 140% higher-quality factor and a 230% higher-operation frequency than silicon-core inductors. A 33 MHz boost converter mounted with an air-core toroidal inductor achieves an efficiency of 68.2%, which is better than converters mounted with a Si-core inductor (64.1%). Our inductors show good thermal cycling stability, and they are mechanically stable after vibration and 2-m-drop tests.

Keywords: MEMS inductor; PwrSoC; TSVs; very high frequency; 3D

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INTRODUCTION

Inductors and transformers are the fundamental building blocks of electronics, and they are found in every electronic device. Micro-inductors and transformers (now referred to as inductors) are used in, for example, radio frequency microelectromechanical systems (RF MEMS)^{1–4}, microactuators^{5,6}, and biosensors⁷. Micro-inductors for power electronics is an emerging application in which inductors are used as energy storage elements for switched mode power supplies (SMPS). Miniaturization of SMPS has become the main focus for developing future generation power supplies, that is, power supply in package (PwrSiP) and power supply on chip (PwrSoC)^{8–10}. The PwrSoC vision is to integrate all power electronics components on one chip. Higher integration lowers the cost and increases both efficiency and power density. Therefore, one of the most important inductor requirements for PwrSoC technology is the CMOS compatibility for on-chip integration. Other requirements are compact physical dimensions, a high-current capacity, and a high-quality factor for high efficiency¹⁰. Switching at very high frequencies (VHF, 30–300 MHz) is one route toward PwrSiP and PwrSoC^{11,12}. In the VHF range, inductors with an air core or non-magnetic core are preferred, as suitable magnetic materials working at these frequencies are limited and the core implementation is very challenging¹³. For example, at 50 MHz, NiZn and CoNiZn have low magnetic saturation fluxes and cause detrimental core heating in high-flux power electronics applications¹⁴. In addition, VHF converters require inductance values of 10 s of nH, which is in the inductance range of air-core inductors, thereby lending themselves to a promising solution¹⁵.

The reported MEMS inductor fabrication technologies can be classified into two main categories: on-substrate inductors and substrate-embedded inductors. To fabricate on-substrate planar inductors, surface micromachining technology has been widely used, particularly for low-aspect-ratio inductors. These methods are based on sacrificial layers¹⁶, molding¹⁷, or a combination of the two¹⁸. One method to fabricate on-substrate high-aspect-ratio 3D inductors is to use UV-LIGA lithography with SU-8 negative resist. The resist structures serve as electroplating molds and sacrificial layer^{19–21} or supporting pillars^{22,23} for the electrodeposition of conducting metals. The second category is embedded inductors, in which the inductors are embedded inside the Si substrate and utilize the unused substrate volume. Consequently, the inductor height above the substrate surface can be lowered, which is an advantage for integrated circuit implementation¹⁴. Si-embedded inductors are also an attractive solution for the advanced packaging of ultra-compact power supplies with the passive interposer²⁴. There are prior-art studies of etched Si cavities for embedded inductors (wet-etched²⁵ and dry-etched²⁶) or through-silicon vias (TSV)^{24,26–28}. Yu *et al.*²⁶ reported a Si-embedded inductor using a fabrication process using 3D shadow masks and multiple lithographical exposures with SU-8. The interconnections are not through wafer. By contrast, TSV inductors²⁷ have the advantage of integrated circuit (IC) integration, that is, co-packaged or stacked systems in a package^{29,30}. MEMS TSVs are known to be a promising technology for miniaturized RF MEMS and advanced system packaging and integration^{31,32}. With the necessity of high-aspect-ratio TSVs for compact 3D inductors, fabrication technology for Si-embedded inductors is still a challenge.

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The near-ideal design of an air-core MEMS inductor involves free-standing windings where the remaining silicon is far from the windings because the silicon negatively affects the operation frequency and energy conversion efficiency due to parasitic capacitance (C_p) and eddy-current losses that ultimately causes undesired heating. The parasitic capacitances between the Cu windings and the Si substrate deteriorates the quality factor and decreases the operation frequency^{26,33}. In addition, there is also an eddy-current loss in the Si core³⁴.

In this paper, we implement a fabrication process of Si-embedded 3D air-core inductors for VHF power conversion applications. The inductors are embedded in the silicon substrate, and the suspended Cu windings are secured by Si fixtures (Figure 1). Our process has three main advantages. First, the process is CMOS-compatible with a maximum processing temperature lower than 200 °C. This allows MEMS processing of CMOS electronics wafers without harming the CMOS electronics. Second, the process is highly generic and enables the fabrication of a large diversity of inductor geometries. We demonstrate the diversity by fabricating spiral, solenoid, toroid, transformer, and the 'DTU' inductor, which cannot be fabricated using wire-winding technology. The toroid geometry is especially well matched for PwrSoC applications because the magnetic field is confined in the

windings to reduce EMI and minimize the cross-talk effects on other proximity electronic components³⁵. Third, the TSV-based inductor technology enables the fabrication of a passive interposer with embedded 3D inductors for PwrSiP.

The paper is presented as follows: The materials and fabrication method are described with a process overview emphasizing the critical steps. Then, the fabrication and characterization results are presented. The inductors were tested with a small-signal measurement, reliability tests with thermal and mechanical shocks, and large-signal testing in VHF converters. The last section concludes the paper.

MATERIALS AND METHODS

Fabrication process overview

The fabrication process includes three main stages, 12 steps and 4 UV lithography masks (Figure 2). A 3D animation of the process is in Supplementary Video S1. We used 100-mm diameter, double-side polished, [100] crystal orientation, Si wafers. Stage 1 focuses on deep reactive ion etching (DRIE) TSV etching and begins with depositing 50-nm-thick aluminum oxide (Al_2O_3) on both wafer sides by atomic layer deposition (ALD). On the wafer front side, an Al_2O_3 hard mask is patterned by buffered hydrofluoric acid (BHF)

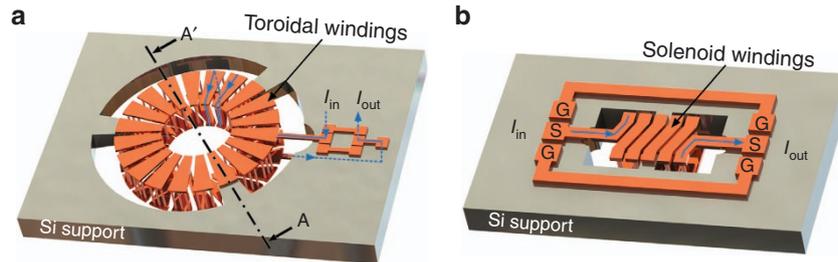


Figure 1 3D illustrations of the air-core toroidal inductor (a), and solenoid inductor (b). The input current (I_{in}) and output current (I_{out}) are indicated by the arrows. Ground-signal-ground (GSG) pads were designed for RF measurements. For the fabrication process of the cross section A'-A, see Figure 2.

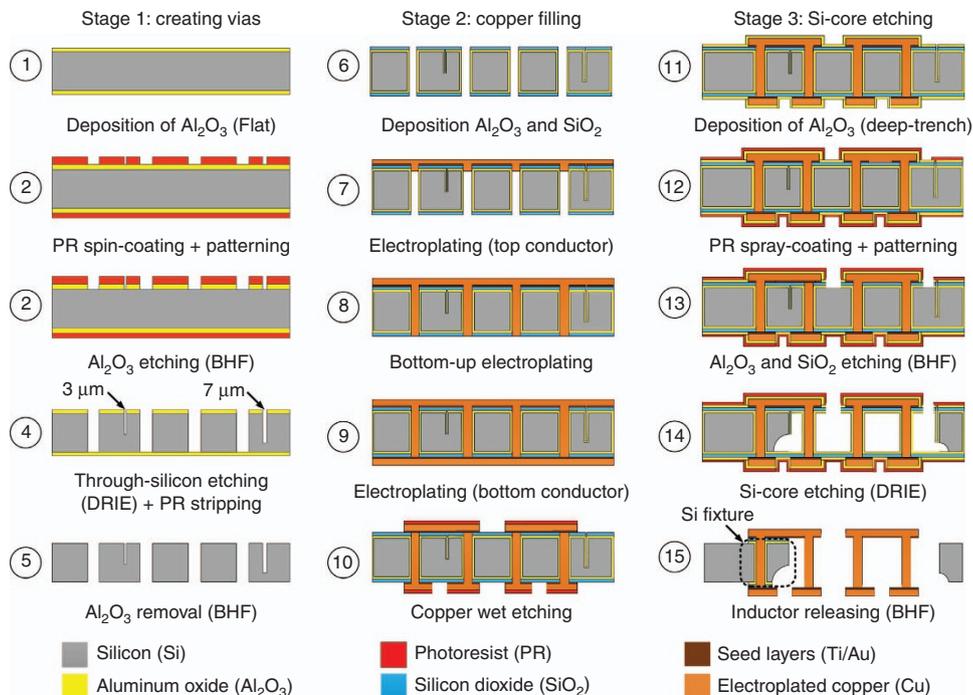


Figure 2 Cross-sectional illustration of the fabrication process flow (section A-A' in Figure 1a). BHF, buffered hydrofluoric acid; DRIE, deep reactive ion etching.

etch using a photoresist mask (AZ Mir 701). Next, TSVs are created by DRIE. The aspect ratio is from 9 to 12. The core shape is also defined in this step by the fixture trenches, which are between 3 μm and 7 μm wide. Finally, the remaining resist and Al_2O_3 are removed with an oxygen plasma and BHF. Stage 1 is finalized by an RCA cleaning step, which is an important preparation for stage 2.

Stage 2 focuses on creating Cu TSVs and windings. First, Al_2O_3 is deposited because it is crucial to cover and protect the deep fixture trenches ($\text{AR} > 30$) during the Si core removal (stage 3). Because of the high etching selectivity of Si over Al_2O_3 in an SF_6 plasma (100 000:1)³⁶ only 50 nm of Al_2O_3 thin film is sufficient to protect the Si support and fixtures (Figure 1b) while removing the Si core. Step 6 also includes the deposition of 1.5 μm SiO_2 by plasma-enhanced chemical deposition. It partly seals the 3- μm -wide fixture trenches to avoid defects on the top windings. Subsequently, three electroplating steps are performed to form Cu windings. We first plate a 30- μm -thick top layer and seal of the TSVs (step 7), followed by a bottom-up plating step to fill the TSVs (step 8); finally, a 30- μm -thick bottom layer (step 9) is plated. For the electroplating seed layer, we use an electron beam evaporated 10 nm Cr and 100 nm Au thin-film stack. The inductor windings are patterned by Cu wet etching using a resist mask, thus obtaining the Si-core inductor (step 10).

In stage 3, the Si core is selectively removed by inductively coupled plasma (ICP) etching. During the ICP etch, Cu is protected by a 50-nm-thick Al_2O_3 layer from the plasma environment as an additional precaution (step 11). A spray-coated photoresist uniformly covers the 30- μm -tall Cu windings and, more importantly, seals the fixture trench (step 12). The spray-coating recipe was carefully developed. Photolithography is then performed on the wafer front side, followed by BHF etching of Al_2O_3 and SiO_2 to expose the silicon (step 13) for isotropic silicon ICP etching (step 14). The Al_2O_3 layers on the fixture trenches and at the wafer backside act as an ICP etch stop, allowing complete removal of the Si core. The windings are anchored by several Si fixtures and suspended on the $\text{Al}_2\text{O}_3/\text{SiO}_2$ membrane. The final air-core inductor is obtained by removing the oxides in BHF.

Critical processes and process parameters

In this section, we describe the critical equipment, materials, and process parameters optimized for our process flow. We focus on the ALD of Al_2O_3 (steps 1, 6, and 11), DRIE for TSV etching (step 4), Cu electroplating for TSVs and inductor windings (steps 7–9), photoresist spray coating for BHF etching of Al_2O_3 and SiO_2 (step 12), and isotropic ICP etching of the Si core (step 14).

For steps 1, 6, and 11, a thermal ALD instrument (Picosun R200, Espoo, Finland) deposits Al_2O_3 , which serves as both the DRIE etch mask and the stopping barrier. Here a 50-nm-thick Al_2O_3 film is ALD-deposited at 200 °C using alternating exposures of trimethylaluminum (TMA) (Strem Chemical, MA, USA) and H_2O . The reactor pressure was below 2 kPa during deposition. We developed two recipes for flat surface (step 1) and deep trenches ($\text{AR} = 32$) (steps 6 and 11), respectively. For flat wafers, one ALD reaction cycle consists of one pulse and purge step for each precursor. Together with the carrier gas (N_2), the precursor gasses are pulse injected into the reactor, and the reactor is subsequently purged with the carrier gas. The pulse time is 0.1 s, and the purge time for TMA and H_2O are 3 and 4 s, respectively. For deep trenches, the second recipe has two pulse and purge steps for each precursor. For both precursors, the first pulse is 0.1 s followed by 0.5 s of purging, whereas the second pulse is 0.1 s followed by 20 s of purging³⁷. The carrier gas flow is 150 sccm and 200 sccm for the TMA and H_2O precursor, respectively. The deposition rates of both recipes are 1 Å per cycle. The thin-film thickness is measured using spectroscopic ellipsometry (M-2000V, HAWoollam, Inc., Lincoln, Nebraska, USA).

For step 4, a DRIE tool (Pegasus, SPTS, UK) etches TSVs and the fixture trenches. The etch mask stack includes 2- μm -thick Mir 701 photoresist (Microchem, Inc., USA) and a 50-nm-thick Al_2O_3 layer. The Al_2O_3 layer on the wafer back side acts as a stopping layer when etching through the Si wafer. For etching silicon TSVs and fixtures, we developed a two-segment recipe including a fast etching segment (segment A) and a notching-compensation etching segment (segment B) for the final part of the TSV. For both segments, coil powers are 2800 W and 2000 W in the etch and passivation steps, respectively. The process temperature is 20 °C for segment A and 10 °C for segment B. Segment A is used to etch 95% of Si in the wafer thickness, whereas the remainder is etched with segment B. The plasma chamber is pre-conditioned by 10 min of an oxygen plasma before DRIE of silicon. Segment A is optimized for high-speed etching with an etch rate of 11 $\mu\text{m min}^{-1}$ with a 5% etch load. This recipe is based on the Bosch process with three alternating steps, including sidewall passivation (4 s, 200 sccm C_4F_8 , 25 mTorr), boost (1.5 s, 350 sccm SF_6 , 25 mTorr, platen power 140 W), and Si etch (5 s, 550 sccm SF_6 , 150 mTorr). Segment B uses a low-frequency platen generator (380 KHz) to minimize notching³⁸ at the Al_2O_3 stop layer. The two main steps are Si etching (3 s, 400 sccm SF_6 and 40 sccm O_2) and passivation (2 s, 250 sccm C_4F_8).

For steps 7–9, electroplating is used to deposit Cu as the conductor material. It is done in a custom-designed chemical bath and setup³⁹. Briefly, the electroplating bath consists of two titanium bars holding a Cu anode and a cathode, which is connected to the sample. The electrolyte contains 140 g L^{-1} CuSO_4 , 140 g L^{-1} H_2SO_4 , and 66 mg L^{-1} NaCl. Air bubbling is used for electrolyte agitation. Electroplating is performed at room temperature. Two processes are developed for, respectively, plating a 30- μm -thick Cu layer on a planar surface (steps 7 and 9) and bottom-up filling into TSVs (step 8). Dedicated wafer holders for each processes have been designed. One key feature of the holder for the first process is the stainless steel ‘current thief’ for excellent plating-thickness uniformity across a 100-mm wafer (< 5% peak to peak). The holder for the second process has a stainless steel plate connected to a pin to achieve electric contact from the bottom of the wafer and a plastic cover to fix the wafer and avoid plating at the edge. First, for the planar plating step, it is important to seal the TSVs to provide an electrical path for TSV filling. A pulsed current with an average current density of 2.57 A dm^{-2} is tested to be effective in closing the TSVs. Second, for TSV filling, a direct DC current at a density of 0.3 A dm^{-2} is used. A degassing step is required for both TSV closing and filling to achieve void-free Cu-filled TSVs. For degassing, the Si wafer is immersed in water and kept in vacuum (desiccator) for 10 min before abrupt venting. Trapped air bubbles expand in a vacuum and escape from cavities. This step is repeated several times until no bubbles appear, after which the wafer is mounted on the plating holder. Despite degassing, the plating process is not uniform, and some TSVs would be filled and over-plated before others. This problem is solved by removing over-plated Cu with a ‘shaving’ process using a stainless-steel blade. Because silicon dioxide and alumina are much harder than stainless steel, the shaving process does not scratch the sample mirror finish, which is required for subsequent processes. The filling process is then continued for the unfilled TSVs. This shaving-filling procedure is repeated several times until all TSVs are uniformly filled. More than 98% of TSVs are filled successfully with this process. Top and bottom Cu layers are then etched with a photoresist mask (AZ 4562, Microchem, Inc.) using a commercial wet etchant (APS 100, Transene, MA, USA). The etch rate is $\sim 0.5 \mu\text{m min}^{-1}$ at room temperature.

For step 12, a spray-coating instrument (ExactaCoat, Sono Tek Co.) is used for uniform resist-layer coating of the 30- μm -tall Cu windings and, more importantly, for sealing the fixture trenches. The spray-coated resist is then used (step 12) as a mask for etching

Al_2O_3 and SiO_2 using BHF (step 13). The photoresist, AZ4562, is diluted in methyl ethyl ketone and propylene glycol monomethyl ether acetate with an optimized mixing ratio of 10:2:1. A two-step spray coating recipe is developed to simultaneously cover the Cu windings and seal the fixture trenches, which are 3 and 7 μm wide. The resist is sprayed twice with a 1-min waiting time at 28 °C and the following parameters: The spray nozzle is 30 mm above the substrate, moving along a meandering path at a speed of 10 mm s^{-1} . The resist dispense rate is 2500 $\mu\text{l min}^{-1}$. The distance between two spraying lines is 5 mm. The substrate temperature is kept at 28 °C. To avoid air bubbles in the resist, the resist solvents trapped in the trenches are slowly evaporated by storing the samples for 5 h at room temperature. Then, the resist is pre-exposure baked in a convection oven at 90 °C for 30 min. The resist thickness on flat areas is 6 μm . Multiple exposures (4 exposures, 10 s waiting time between exposures, and a total dosage of 420 mJ cm^{-2}) are necessary to avoid resist overheating. The sample is then developed for 300 s using AZ 351B (Microchem, Inc.) diluted in deionized water with a volume ratio of 1:5. Hard-baking is done in a convection oven at 150 °C for 30 min.

For step 14, an ICP silicon-etching tool (STS MESC Multiplex ICP, SPTS, Newport, UK) removes the silicon core and realizes the final air-core inductors. We developed a fluorine-based isotropic ICP recipe utilizing the undercut effect to etch Si in the toroidal core. The etch gases are 230 sccm SF_6 and 23 sccm O_2 . The coil power is 2800 W, and a minimal platen power of 3 W is applied for maximal isotropic etching. The etch rate of the Si core is 10 $\mu\text{m min}^{-1}$. The spray-coated resist and a 50-nm-thick Al_2O_3 stack serve as the etch mask. The wafer backside is coated by 50-nm-thick Al_2O_3 and two layers of the spray-coated resist. The Al_2O_3 layer stops the etching and prevents leaking of helium for backside substrate cooling.

RESULTS AND DISCUSSION

Fabrication results

We successfully fabricated 3D air-core inductors. Scanning electron microscopy (SEM) micrographs show toroidal inductors, solenoids, spirals, and a 1:1 transformer (Figure 3). In addition, we can also create inductors with arbitrary shapes; this is demonstrated by the 'DTU' inductor. The process achieved a yield of 64–95% (Supplementary Figure S4).

In this study, we fabricated 15 different toroidal inductor designs with footprints from 4 mm^2 to 16 mm^2 , an outer radius (R_o) from 0.5 mm to 2 mm, and an inner radius (R_i) from 0.5 to 1 mm. The number of turns varies from 15 to 35 turns. Inductors with 30- μm -diameter TSVs were realized on 280- μm -thick and 350- μm -thick Si substrates. Thicker substrates can also be used with our process. We created inductors on a 500- μm -thick substrate with 50- μm TSVs. The inductors were designed with several TSVs in the outer ring to enhance volume coverage and minimize resistance. In addition, the identical diameter of TSVs achieves a uniform through-wafer etching and Cu TSV filling. As described before, the Si core has been removed to realize the desired air-core and suspended windings structure. The release process includes BHF dipping, deionized water rinsing, and gentle nitrogen gas drying. After the release, we did not observe any deformation of the windings. The inductors are suspended on the Si support and secured by symmetrically placed Si fixtures. Our inductors are made of only Si and Cu; no polymers (for example, PDMS or SU-8) are used. We expect the inductors to have good thermal stability, and low stresses are anticipated due to the lower thermal expansion coefficient (CTE) mismatch between Cu and Si ($\Delta_{\text{CTE Cu-Si}} = 14.1$ ppm per °C), compared with Cu and SU-8 ($\Delta_{\text{CTE Cu-SU-8}} = 35.3$ ppm per °C). The inductor windings are free hanging and only secured in the Si fixtures. Only at the fixtures, there may be higher stress due to the direct Si-Cu contact. To

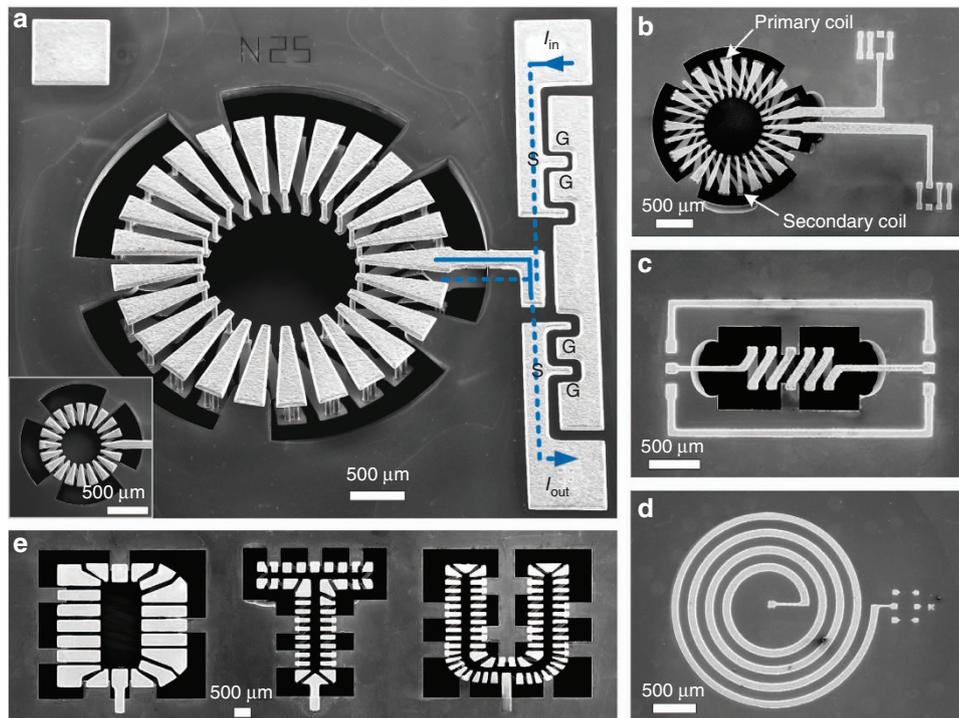


Figure 3 SEM micrographs of the fabricated 3D air-core MEMS inductors, (a) toroidal inductors with 16 mm^2 (1.5 mm outer radius, 0.75 mm inner radius, and 25 turns) and 4 mm^2 footprint (inset). Presented by the lines and arrows, the current flows from the top wire bonding pad, through the TSV interconnects, then passes through the windings and exits at the lower pad. The measurement pads are designed in a ground-signal-ground configuration at both terminals for wafer-level probing. Four 800 μm by 800 μm pads at the corners are for flip-chip bonding. (b) 1:1 toroidal transformer. The primary coil has larger conductors than that of the secondary coil. (c) Solenoid inductor, (d) spiral inductor, (e) 'DTU' inductor. SEM, scanning electron microscopy; MEMS, microelectromechanical systems; TSV, through-silicon vias.

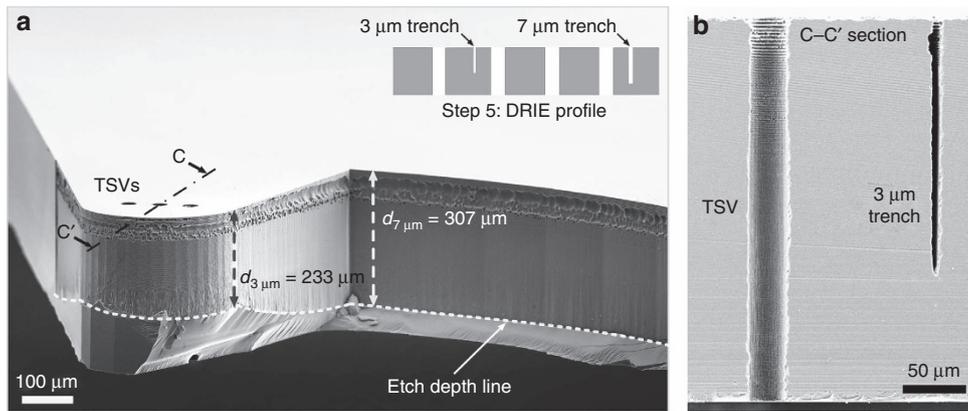


Figure 4 Etching profile after DRIE (step 5). **(a)** An SEM micrograph of a cleaved Si wafer showing the etching profile at the Si fixture. Enclosed in the fixture are three TSVs that have been etched through. As depicted in the inset taken from the process flow, the fixture trenches are etched with shallower depths of 233 and 307 μm for the 3- and 7- μm -wide fixture trenches, respectively. **(b)** A cross-sectional SEM micrograph (C-C' direction) of the TSV and 3- μm -wide trench. This sample was cut with a diamond blade. DRIE, deep reactive ion etching; SEM, scanning electron microscopy; TSV, through-silicon vias.

enable post processing of CMOS wafers, we kept all process temperatures below 200 $^{\circ}\text{C}$.

In the following, the fabrication results of each step are presented and discussed. Design considerations and technology challenges are described.

DRIE etching

We created the TSVs and fixture trench by DRIE (step 4). The Si fixture is designed taking advantage of the loading effects and the aspect ratio dependent etch (ARDE) effect⁴⁰, which means that wider patterns are etched with deeper than narrower patterns as presented in the inset of Figure 4a. Figure 4a shows a tilted view of the Si fixture trench after through-wafer etching. Figure 4b shows that the TSVs have been etched through while the narrow fixture trench is not. The fixture trench has 3- and 7- μm -wide sections. The 7- μm -wide trench defines the core shape, and the 3- μm -wide trench defines the shape of the Si fixture. The semicircle trench must be 3- μm wide to avoid defects that are transferred to the top inductor windings during copper plating. Illustrated by the dashed line in Figure 4a, the ARDE leads to an etch depth of 307 μm for the 7- μm -wide section and a 233- μm etch depth for the 3- μm -wide section.

Copper electroplating and wet etching

After the first plating step of a 32- μm -thick top Cu layer (step 7), the 30- μm -diameter TSVs were completely closed (Figure 5a). Approximately 35 μm of copper was deposited into the TSVs (Figure 5a, inset). Without any voids or trapped air, the TSVs were filled in the second plating process (step 8, Figure 5b). While we completely filled the TSVs directly in the second plating step, another fabrication method is to make hollow TSVs with seed layers covered uniformly on the TSVs sidewalls followed by electroplating. ALD is a suitable technique to uniformly deposit seed layers on high-aspect-ratio TSVs^{41,42}. However, hollow TSVs are limited in current handling capability and are less suitable for power electronic applications. We patterned the inductor windings by Cu wet etching with a photoresist mask. Due to undercutting of the isotropic Cu wet etching, we must consider etch compensations on the mask design, meaning that, for example, a winding gap (G_w) of 94 μm requires a mask design width of 40 μm (Figure 5c). Because of the isotropic etching profile, the pitch between nearby turns is limited. To reduce the winding pitch, alternative methods are mould-based electroplating^{19,20,43} and anisotropic plasma etching of Cu^{44–46}.

Both approaches can easily be integrated into our process with minor adaptations at steps 8 and 10.

Spray coating and Si-core isotropic dry etching

This section presents the last stage of Si-core removal to create the final air-core inductors (Figure 6). To expose the Si core to the isotropic ICP etch, photolithography is performed using a spray-coated resist. Figure 6a shows BHF etching of SiO_2 and Al_2O_3 using a spray-coated resist mask (step 13). Conformal coating of the resist is preferred, but this is impossible for the deep fixture trenches; hence, we sealed the trenches. Sprayed resist flowed into the trenches and resulted in a very thin resist layer (150 nm) on the fixture edge. This was not enough to sustain the 20-min BHF etch to remove the 50-nm-thick Al_2O_3 and 1.5- μm -thick SiO_2 because HF diffusion depends on the resist thickness. According to Fick's law of diffusion, doubling the resist thickness allows a four-times-longer etching time in BHF. Therefore, we doubled the resist thickness by developing a two-step spraying recipe, whereby the resist covers the 30- μm -tall Cu windings and seals the trenches simultaneously. After the first spraying step, the resist was optimized so that the solvents quickly evaporated (60 s) before the second spray coating, which gives a resist laying on top of the first layer and seals the trenches. The same resist thickness could be achieved with a one-step spraying recipe; however, all the resist will flow into the trenches and result in bad sealing and thin resist on the trench edges. Figure 6b shows good and poor resist trench filling and the corresponding results after Si-core etching. With poor sealing, Al_2O_3 deposited on the fixture trench sidewalls is not protected in BHF etching (step 13), resulting in an eroded fixture during the ICP Si-core etch (step 14). After Si-core etching with good trench sealing, a hollow Al_2O_3 stopping barrier remained as shown in Figure 6c.

After the inductor releasing step with BHF etching, the final air-core toroidal inductors were obtained as shown in Figure 3a. The Si core was completely removed, leaving the suspended windings secured by the symmetrically placed Si fixtures. After the ICP etch, the windings were not deformed, indicating that the residual stresses were extremely low due to the low processing temperature. We did not observe winding deformations after the release steps, indicating that the structures can withstand wet processes and that no vapor or critical-point drying steps were required. The two inductor terminals are placed on the front side for advanced packaging and characterization. We show outstanding inductor core design flexibility, and our process uniqueness is demonstrated by the 'DTU' core inductor. The

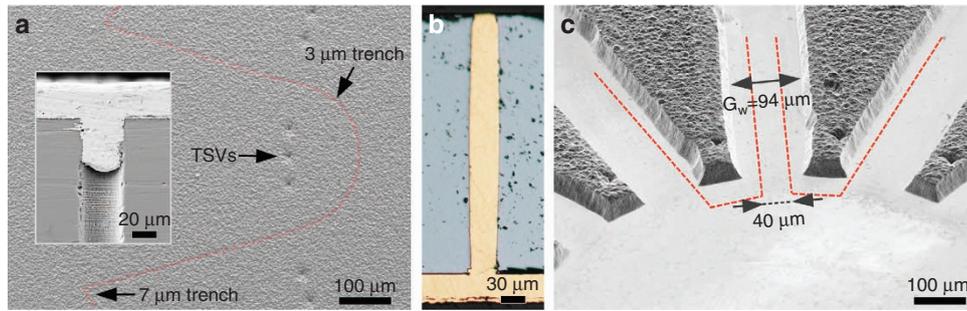


Figure 5 Cu electroplating and wet-etching results. (a) A top-view SEM micrograph after the first plating of the 30- μm -thick Cu layer (step 7). All TSVs and the fixture trench are closed, which provides the electrical path for bottom-up TSV filling. The transparent red line illustrates the fixture trenches that have been closed. Copper is filled 35 μm into the TSVs, as shown in the subfigure. (b) A void-free Cu-filled TSV after 13.5 h of plating at 0.5 A dm^{-2} (step 8). (c) Wet-etched toroidal Cu windings (step 9). The red lines are isotropic wet-etch compensations on the photolithography mask design. The winding pitch (G_w) is increased from the designed 40 to 94.3 μm due to the lateral undercut. SEM, scanning electron microscopy; TSV, through-silicon vias.

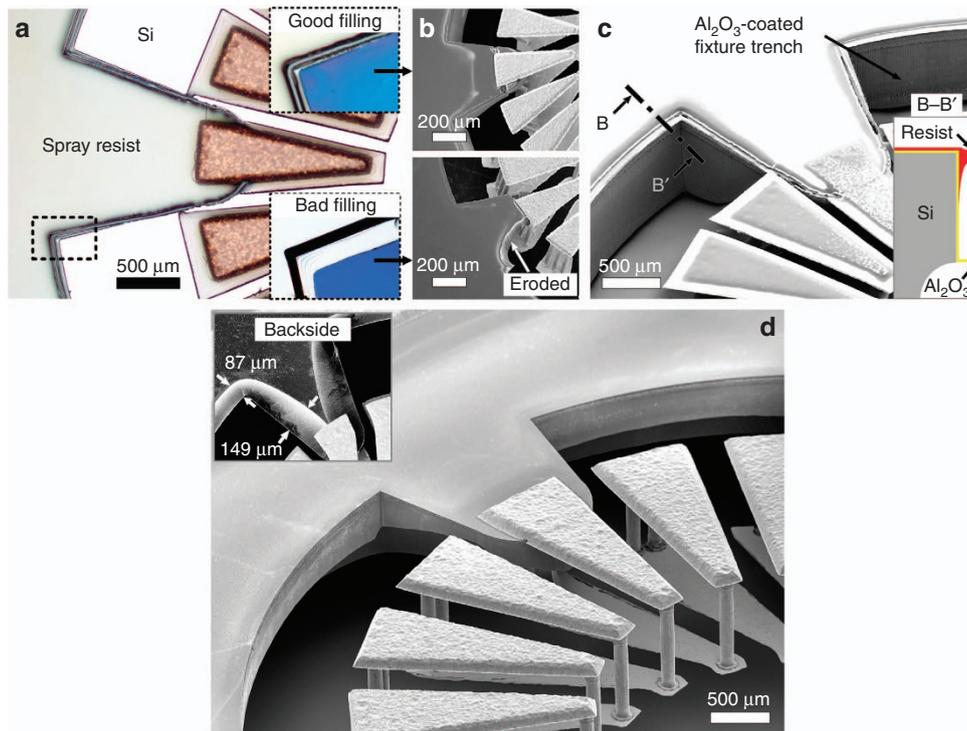


Figure 6 (a) Optical top-view micrograph of the patterned spray-coated resist at the Si fixture (step 12). Good and bad fixture trench resist sealing are shown in the top and bottom insets. (b) Si-core etching results corresponding to good and bad sealing. (c) A hollow Al_2O_3 stopping barrier on the fixture trench (cross section is depicted in the inset) and an $\text{Al}_2\text{O}_3/\text{SiO}_2$ membrane at the bottom remained after isotropic ICP Si etching. (d) A well-defined Si fixture was on the final inductor after the BHF releasing step, and the fixture backside is shown in the inset. BHF, buffered hydrofluoric acid; ICP, inductively coupled plasma.

other approach to remove the Si core is potassium hydroxide (KOH) Si wet etching, but the core geometries are heavily restricted, that is, square rectangular cores are possible. The KOH is, however, a cheaper batch process.

Small signal measurement

Our MEMS inductors were electrically characterized in the frequency range from 1 to 110 MHz using a precision impedance analyzer (Agilent 4294A, Agilent Technologies Inc., Santa Clara, CA, USA). The measurements were done for four toroidal inductor designs: (i) 280- μm -tall and 25-turn air-core inductors, (ii) 280- μm -tall and 20-turn air-core inductors, (iii) 350- μm -tall and 20-turn air-core inductors, and (iv) 280- μm -tall and 20-turn Si-core inductors. The inductors have a 0.75-mm inner radius, a 1.5-mm outer radius, and a TSV

diameter of 30 μm . For each design, we measured three inductors, and for Figure 7, 12 inductors in total were measured. More details on the inductor design, modeling, and measurement will be presented in our upcoming paper.

Figure 7a shows the measurement results for three inductors of design (i). The measured inductance and resistance values are 20% larger than simplified analytical calculations of ideal toroid inductors. At the peak quality factor (Q) frequency (41.2 MHz), the inductance is $34.3 \text{ nH} \pm 0.12 \text{ nH}$, and Q is 12.9 ± 0.17 . The resistance is $180 \pm 7 \text{ m}\Omega$ at 1 MHz. The inductors were from the same wafer. For all measurement points, the average peak-to-peak variations are 0.56% (inductance), 2.67% (quality factor), and 2.56% (resistance), respectively. We have also compared the inductors from two different process runs. Ten toroidal inductors with 280 μm tall and 20 turns were measured. The standard

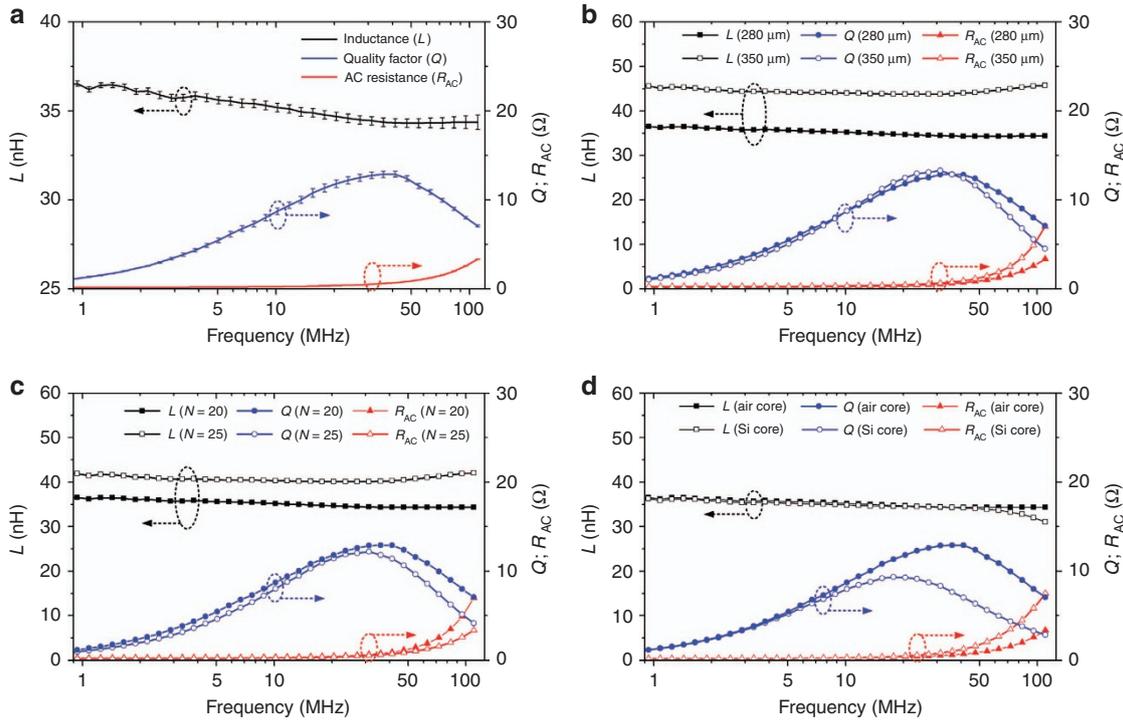


Figure 7 Comparison of the frequency-dependent inductance (L), quality factor (Q), and AC resistance (R_{AC}) of selected toroidal inductor designs. (a) Measurement of three inductors with the same design (280- μm tall, 20-turn air-core toroidal inductor). The mean values and error bars are plotted. (b) Comparing 20-turn air-core inductors fabricated using 280- and 350- μm -thick substrates. (c) Comparing air-core inductors with 20 and 25 turns. (d) Comparing air-core and Si-core inductors.

Table 1 Comparison of the electrical performance of embedded air-core toroidal inductors

Inductor from	R_{DC} (m Ω)	L_{density} (nH mm $^{-3}$)	$Q_{\text{peak@frequency}}$ (MHz)
This work (toroid)	180–263	13.6–17.3	10–12.9@31.8–72.6 MHz
Yu <i>et al.</i> ²⁶ (toroid)	400	3.12–4.16	16–17.5@40–70
Li <i>et al.</i> ²⁸ (toroid)	265	2.95	10.5@14

deviations are less than 1.9% for inductance, 8.4% for resistance, and 9.2% for quality factor. The inductance tolerance of our inductor is lower than that of the wire-wound inductors (5–10%). The relatively small variations indicate that the fabrication process is reproducible. This is an essential advantage for SMPS and electronic design.

For PwrSoC inductors, a high inductance and a high Q factor are desired. For a toroidal inductor, this could be done by increasing the inductor height or number of turns. We compared 350 to 280- μm -tall inductors and 25 to 20-turn inductors. The results are shown in Figures 7b and c. Our data show that there are tradeoffs between the inductance density, Q-factor, and optimal operation frequency. By increasing the number of turns, a higher inductance density (17.3 nH mm $^{-3}$) is achieved, however at the same time causing a lower peak Q-factor (10) at a lower frequency (31.8 MHz). Taller inductors show a higher Q-factor at higher frequencies, whereas the inductance density is lower (14.2 nH mm $^{-3}$).

Figure 7d compares air-core and Si-core toroidal inductors fabricated with 20 turns on a 280- μm -thick wafer. Air-core inductors showed a 140% higher-quality factor and a 230% higher-operation frequency than did the Si-core inductors (Q of 9.3 at 17.8 MHz). At high frequencies (> 50 MHz), the inductance decreases and the resistance increases due to the increased parasitic capacitances (C_p) and the eddy-current losses in the Si

core. C_p was measured to 3.71 pF and 11.5 pF for the air core and the Si core, respectively. A higher C_p increases the effective resistance with increasing frequency. Therefore, without removing the Si-core, $R_{AC\text{-eff}}$ is 108 and 140% higher than that of the air-core inductor at 50 and 100 MHz, respectively. We also fabricated inductors that can operate at a higher frequency of 72.6 MHz with a Q of 11.5 and an L of 42.5 nH. This inductor (350- μm -tall, 5 mm 2) has a lower parasitic capacitance due to 20 times smaller pads (Figure 1a), compared with that of the inductor in Figure 3a.

Table 1 compares the electrical performance of our MEMS toroidal inductors and prior art on embedded inductors. Our inductors have four-times-higher inductance compared to other Si-embedded toroidal inductors with typical densities of 3–4 nH mm $^{-3}$. This is because our high-aspect-ratio TSVs enable compact inductors to be embedded in a Si wafer for a decreased total volume and higher inductance density. Our inductor DC resistance is lower while the Q-factor is similar to the previous work.

Thermal and mechanical reliability

Our 3D MEMS toroidal inductors were tested with thermal shock and drop testing experiments. First, the thermal shock test was performed in a temperature shock test chamber VT 7010 S2 (Vötsch, Weiss Technik UK Loughborough, Leicestershire, UK). The temperature was rapidly cycled from –40 to 150 °C under vacuum

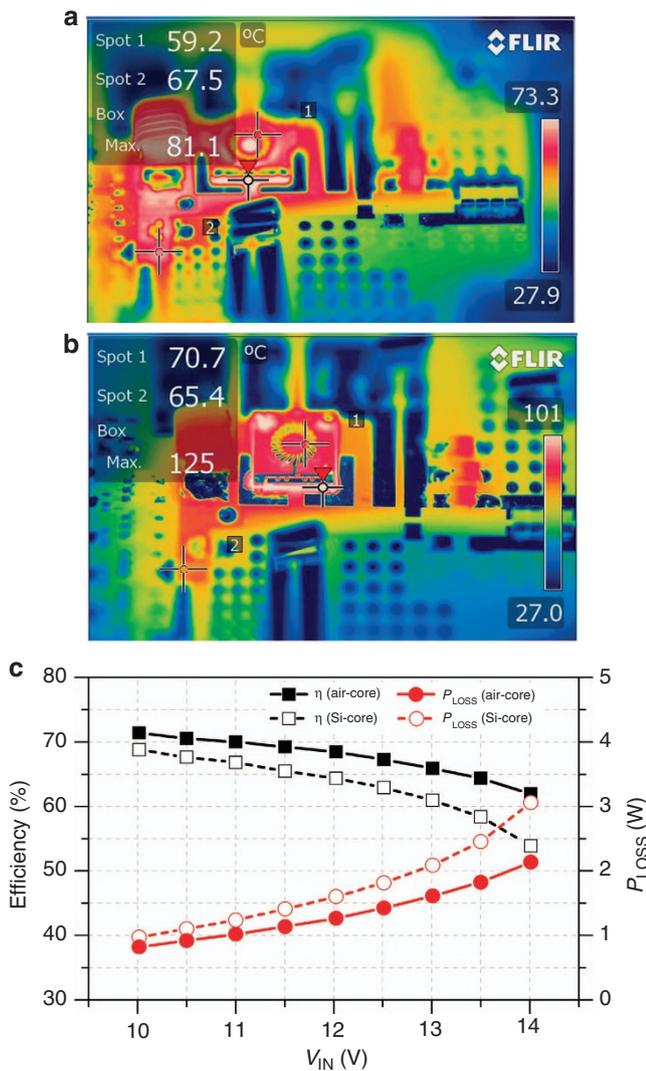


Figure 8 Thermal images of the converter ($V_{IN} = 12\text{ V}$) with (a) the air-core inductor and (b) the Si-core inductor. The images were captured by FLIR camera T600 (FLIR, USA) using a standard lens. (c) The efficiency and the converter power loss are presented as a function of the input voltage (V_{IN}) for the air-core inductor and the Si-core inductor.

for 250 cycles. The heating rate was 3 °C min^{-1} , and the cooling rate was 3.5 °C min^{-1} . We tested eight inductors: four air-core inductors (TSV diameters of 30 and 50 μm) and four Si-core inductors (TSV diameters of 30 and 50 μm). After 250 cycles, the inductors were optically inspected and electrically characterized. All inductors were electrically functional, and no deformation or cracks were observed. More details of the testing results can be found in Supplementary Figures S1 and S2.

Second, drop testing experiments were conducted to probe the mechanical stability of the suspended windings. The inductors were mounted on a PCB test board, which then was dropped on an aluminum plate from a height of 0.5, 1, and 2 m. Up to the height of 2 m, no winding deformation was observed, and the electrical properties were unchanged. Our results suggest that the fabricated inductors are stable for practical use in electronic circuits. The optical images of tested inductors are shown in Supplementary Figure S3. For applications that require more robust windings, we suggest filling the air core with epoxy or silicon rubber. We anticipate a slight decrease in performance.

Large signal testing in VHF converters

The large signal performances of our air-core toroidal inductors and Si-core toroidal inductors were compared in a 33 MHz class E resonant DC-DC boost converter (Figure 8). More details about the converter design are in Ref. Le HT, Nour Y, Han A, et al. Microfabricated air-core toroidal inductor in very high frequency power converters, unpublished observations. The input voltage ranges from 10.0 to 14.0 V_{DC} , the output voltage ranges from 25.5 to 35.4 V_{DC} , and the output power ranges from 1.6 to 3.2 W. Figures 8a and b show thermal images of the converter with an input voltage of 12.0 V and an output voltage of 30.0 V. Our Si-core inductor shows a maximum temperature of 125 °C, a power converter efficiency (η) of 64.1%, and a converter power loss (P_{LOSS}) of 1.6 W. In contrast with the Si-core inductor, our air-core inductor shows a significantly lower peak temperature of 85 °C, a higher converter efficiency (68.2%), and a lower converter power loss (1.26 W). As the inductor geometries are identical, our results imply that the Si core causes a power loss of 0.34 W for the converter, which results in an additional 40 °C temperature increase. This is consistent with our small signal resistance measurements; at 33 MHz, the Si-core inductor has a higher resistance (1 Ω) than the air-core inductor (0.6 Ω). The increased resistance is due to the capacitive and the eddy-current loss in the Si core.

CONCLUSION

We successfully realized 3D air-core MEMS inductors for VHF power electronic applications. Compared with prior art on toroid inductors, we demonstrated a fourfold larger inductance density while keeping a good-quality factor and operation frequency. We have demonstrated that the proposed process is CMOS-compatible for the post integration of 3D inductors and highly generic for fabricating a large diversity of inductor geometries, for example, a spiral, solenoid, and toroidal inductor; a toroidal transformer; and a 'DTU' inductor. Our small-signal and large-signal measurements show that the air-core inductors outperform the silicon core inductors in the MHz regime. Our technology of integrated 3D inductors with high-aspect-ratio TSVs has a great potential for PwrSiP as an advanced passive interposer with the embedded 3D inductors. In the next step, we will focus on integrating magnetic materials as the core material, to expand the frequency range in which the inductor can be used. While our technology has been developed for power systems on chip (PwrSoC) applications, we believe that our generic technology will find other applications, for example, integrated high-Q LC filters may be used in RF MEMS for transmitters and receivers.

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COMPETING INTERESTS

The authors declare no conflict of interest.

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