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REVIEW ARTICLE

Development of massively parallel electron beam direct write lithography using active-matrix nanocrystalline-silicon electron emitter arrays

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Nanoscale lithographic technologies have been intensively studied for the development of the next generation of semiconductor manufacturing practices. While mask-less/direct-write electron beam (EB) lithography methods serve as a candidate for the upcoming 10-nm node approaches and beyond, it remains difficult to achieve an appropriate level of throughput. Several innovative features of the multiple EB system that involve the use of a thermionic source have been proposed. However, a blanking array mechanism is required for the individual control of multiple beamlets whereby each beamlet is deflected onto a blanking object or passed through an array. This paper reviews the recent developments of our application studies on the development of a high-speed massively parallel electron beam direct write (MPEBDW) lithography. The emitter array used in our study includes nanocrystalline-Si (nc-Si) ballistic electron emitters. Electrons are drifted via multiple tunnelling cascade transport and are emitted as hot electrons. The transport mechanism allows one to quickly turn electron beamlets on or off. The emitter array is a micro-electro-mechanical system (MEMS) that is hetero-integrated with a separately fabricated active-matrix-driving complementary metal-oxide semiconductor (CMOS) large-scale integration (LSI) system that controls each emitter individually. The basic function of the LSI was confirmed to receive external writing bitmap data and generate driving signals for turning beamlets on or off. Each emitted beamlet ($10 \times 10\ \mu m^2$) is converged to $10 \times 10\ nm^2$ on a target via the reduction electron optic system under development. This paper presents an overview of the system and characteristic evaluations of the nc-Si emitter array. We examine beamlets and their electron emission characteristics via a 1:1 exposure test.

Keywords: direct write lithography; electron beam lithography; electron emitter array; multiple electron beams; nanocrystalline; Si

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INTRODUCTION

High-throughput nanoscale lithographic technologies have been intensively studied and developed in relation to the upcoming 10-nm node and beyond for the improvement of semiconductor manufacturing practices. Electron beam (EB) direct-write lithography, immersion lithography combined with multiple patterning, extreme ultra-violet lithography and nano-imprinting methods serve as candidates of the next generation of lithography practices. Only the EB direct-write approach serves as a mask-less lithography method.

While conventional single-EB direct-write systems have been used to fabricate photomasks and semiconductor devices with fine patterns, they are not suitable for mass production due to their slow writing speed capacities. For a high-speed lithography to be performed, more than three orders of throughput increase are required. A massive parallelism approach has been proposed to address this roadblock[1], and several approaches to parallel EB lithography involving the use of conventional thermionic sources have also been presented[2–8]. Multiple aperture pixel by pixel enhancement of resolution (MAPPER)[5] uses a single thermionic source. Emitted electrons are split into parallel 5-keV electron beamlets that are collimated when passing through a fabricated micro-electro-mechanical system (MEMS) aperture array. A blanker array is signal-delivered by laser beams and switches each beamlet on or off. Projection mask less lithography (PML2)[4] also involves utilizing the blanking array mechanism to generate multiple 50-keV electron beamlets for the realization of high throughput levels. These technologies require a blanking array mechanism for the individual control of beamlets, whereby each beamlet is deflected onto a blanking object or passed through the array. In turn, beam-switching speeds may be restricted. In contrast, reflected electron beam lithography (REBL)[2,3] methods involve the use of a complementary metal-oxide semiconductor (CMOS) digital pattern generator (DPG) chip that includes over one million electrostatic reflectors. Electrons generated from a thermionic source are accelerated via an electron gun module and are decelerated to illuminate a DPG chip. The DPG modulates the illuminated electrons and either reflects them back or not by switching them on or off via pixel-by-pixel CMOS voltage levels. The reflected beamlets are then reaccelerated at 50 keV–100 keV and demagnified (1/80 to 1/100) onto a wafer.

We propose a massively parallel electron beam direct write (MPEBDW) system[9–11] with a nanocrystalline-Silicon (nc-Si) electron emitter array. An array of microminiaturized nc-Si electron emitters is integrated with an active-matrix-driving large-scale integration (LSI) mechanism. In the nc-Si, electrons are drifted via multiple tunneling cascade transport and are emitted as hot

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electrons. The transport mechanism allows for the high-speed direct switching of electron beamlets on or off by CMOS-compatible voltage levels without the use of a blanking mechanism. Furthermore, aberrations generated in the electron optics are compensated for by the emitter array itself.

This approach allows for mask-less LSI digital fabrication via production that not only limits increasing photomask costs, but that also shortens the development turnaround period of cutting-edge LSIs. Our blank-less active matrix nc-Si electron emitter driven by CMOS LSI is suitable for use in massive parallel EB lithography practices[9,12].

The EB emitter, which consists of nc-Si dots surrounded by thin tunnelled oxides, is fabricated on a silicon substrate[13–16]. When a sufficient electric field is applied to the emitter, electrons are accelerated and emitted via multiple tunnelling cascade transport[17–19]. The mean kinetic energy of the emitted electrons reaches 5 eV–7 eV through the application of a driving voltage level of roughly 15 V.

1:1 EB exposure lithography approaches have been employed for the improvement of throughput level. The technique has been used for over 40 years[20–23]. Its resolution is determined by $w + 2\varepsilon/E$, where w is the electron emission area, ε is the initial electron energy dispersion level, and E is a uniform electric field strength level that is generated through the application of acceleration voltage between an electron emitter and target wafer[20]. The resolution level can be improved by reducing the electron emission area size, by reducing the initial energy spread or by increasing the electric field intensity level. Prior to the MPEBDW system's development, we experimentally evaluated the resolution capacities of the nc-Si electron emitter using the 1:1 EB exposure test bench. We found a small chromatic aberration owing to a small dispersion of kinetic energy and a small emission angle of the ballistic electron[24,25]. High-resolution pattern transfer ability (<30 nm) levels were also found for the test bench[26,27].

This paper reviews recent progress in our development of MPEBDW lithography methods that use the active-matrix nc-Si emitter array. An overview of the system is provided in the "Configuration of the MPEBDW" section. A fabrication process, performance evaluations of a prototyped nc-Si electron emitter array and a prototyped active-matrix-driving LSI are described in the section "PROTOTYPE NC-SI EMITTER ARRAY AND EMISSION CHARACTERISTICS" and the section "AN ACTIVE-MATRIX-DRIVING LSI FOR THE MPEBDW", respectively.

CONFIGURATION OF THE MPEBDW

Target commercial system specifications

We aim to develop a commercial massive parallel EB lithography system that can write with high resolution and high throughput. Target specifications for the EB writing system include the followings: 10 nm or less in resolution and a throughput level of more than 100 12-inch wafers per hour (>100 wph). To achieve these specifications, we specified (1) a multi-beam column: a single electron optic column that generates 1000 × 1000 electron beamlets of 2.5 × 2.5 nm^2 in beam size and 38 pA in beam current and (2) a multi-column system: a system that projects multiple 1000 × 1000 electron beamlets onto a target wafer. Specifications of the target commercial system are presented in this section.

Our system uses an nc-Si electron emitter rather than a thermionic source and involves beam switching without the use of a blanking array mechanism. The system thus differs from earlier technologies[2–8], as noted in the previous section. We use an electron emitter array as an electron source, and each emitter is turned on or off by an active-matrix-driving LSI. The system can adjust to various electron doses by dynamically controlling electron emitter-driving periods. The emitter array includes 1000 × 1000 electron emitters with a 2.5 × 2.5 μm^2 emission area and 10 μm pitch. A condenser lens array is installed 100 μm above the surface of the electron emitter array. The condenser lens array consists of 1000 × 1000 electron condenser lenses with electrostatic lenses of 8 μm in diameter with a 10 μm pitch. Each electron beamlet size generated by the emitter is converged to 1/10 (0.25 × 0.25 μm^2) by the condenser lens. The 1000 × 1000 electron beamlets that pass through the 1000 × 1000 condenser lens array are accelerated to 5 keV towards an anode. The accelerating voltage is kept relatively low to increase exposure sensitivity levels and downsize the electron optic column. In each electron optic column, 1000 × 1000 electron beamlets of 0.25 × 0.25 μm^2 with a 10 μm pitch are simultaneously reduced by 1/100 using the objective lens (electrostatic Einzel lens). As a result, 1000 × 1000 electron beamlets of 2.5 × 2.5 nm^2 with a 100 nm pitch are projected onto the target wafer. The electron beamlet positioned far away from the optical axis of the objective lens is defocused on the target wafer due to an aberration of field curvature (FC). This aberration is corrected using a method discussed in the section "Aberration correction function".

The system throughput level is estimated using the following equations. Equation (1) calculates the exposure time for a beamlet. Equation (2) calculates the exposure time for each wafer.

$$T_{\text{shot}} = D/J_e \tag{1}$$

$$T_{\text{wafer}} = T_{\text{shot}} \times (L_{\text{EBpitch}}/L_{\text{EBsize}})^2 \times (S_{\text{wafer}}/S_{\text{array}})/N \tag{2}$$

where,
D: Appropriate dosage level (μC cm^{-2}),
J_e: Current emission density (μC cm^{-2}),
T_{shot}: Exposure time per shot (s),
L_{EBpitch}: Beamlet pitch on wafer (μm),
L_{EBsize}: Beamlet size on wafer (μm),
T_{array}: Exposure time required to fill array area (s),
S_{wafer}: Wafer area (mm^2),
S_{array}: Array area on wafer (mm^2),
N: Number of electron optic columns,
T_{wafer}: Exposure time per wafer (s)

We developed a prototype system to establish basic technologies for the target 12-inch-wafer commercial system as shown in Table 1.

Main differences found in these specifications pertain to the current emission density, to the number of beamlets, and to the number of electron optic columns. Here, we focus on improving electron emitter characteristics. Each component of the prototype system under development is described in the following section.

Prototype system configuration

We developed a prototype MPEBDW system to examine the active-matrix nc-Si emitter array and to expose 10 000 pixels of 10 × 10 nm^2 sized beamlet onto the wafer. A column shown in a photograph (Figure 1a) is used in the reduction electron optic system[9]. When the column is modified, it can be used for the 1:1 exposure system. The modified column was used to evaluate EB exposure levels of the nc-Si emitter array via a 1:1 exposure test system as shown in the section "Electron emission characteristics".

The prototype system consists of a 100 × 100 emitter array that is hetero-integrated with an active matrix LSI as a unit, a condenser lens array, an anode, a three-stage deflector (two-stage for beamlet alignment and another for beamlet scanning),

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Table 1 Specifications of the prototype and target commercial system

System		Prototype	Target (commercial)
Current emission density	J_e	10 μA cm^{-2}	600 μA cm^{-2}
Emitter size		10 × 10 μm^2	2.5 × 2.5 μm^2
Emitter array size		10 mm	10 mm
Emitter pitch		100 μm	10 μm
Number of beamlets		10 000	1 000 000
Reduction factor (Condenser lens)		10	10
Reduction factor (Objective lens)		100	100
EB array area on wafer	S_{array}	100 × 100 μm^2	100 × 100 μm^2
EB pitch on wafer	$L_{EBpitch}$	1 μm	0.1 μm
EB size on wafer	L_{EBsize}	0.01 × 0.01 μm^2	0.0025 × 0.0025 μm^2
Accelerating voltage		5 kV or more	5 kV or more
Number of electron optic columns	N	1	12
Exposure time / shot	T_{shot}	2.0 μs	0.033 μs
Exposure time (100×100μm^2)		20 ms	53 μs
Exposure time / wafer	T_{wafer}	141 300 s	31 s
Throughput		0.025 wph	115 wph
Writing bitmap data amount		90 TB wafer^{-1}	1440 TB wafer^{-1}
Appropriate dose	D	20 μC cm^{-2}	20 μC cm^{-2}
Target wafer size	S_{wafer}	12 inch wafer area ($\pi \times 150^2$ mm^2)	

a stigmator, an objective lens as a reduction lens, and a moving stage for wafer positioning.

These 10 × 10 μm^2-sized, 100 μm-pitch, 10 × 10 mm^2-arrayed beamlets generated by the electron emitters are individually converged by a condenser lens array to 1/10 for the generation of 1 × 1 μm^2 beamlets. The beamlets are accelerated to 5 keV by the anode and are aligned with the optical axis using a two-stage deflector. They are reduced by 1/100 (10 × 10 nm^2-sized, 1 μm-pitch, 100 × 100 μm^2-arrayed beamlets) using the objective lens in the system shown in Figure 1b. The size of each beamlet generated by the emitter array is reduced by 1/1000 from the original size.

As shown in Figure 1b, the beamlets cross at the focal area. However, the cross points are dispersive in this area, resulting in a relaxation of Coulomb repulsion effects. This dispersive crossover electron optic system allows for low acceleration voltage and higher exposure sensitivity leading to the generation of higher throughput levels.

Aberration correction function

Aberration of electron optics in the multi-EB system

In an ideal electron lens without aberrations, all incident electron beamlets are converged to a focal point. However, in a real lens with axis symmetry, refraction angles of incident beamlets positioned far from the optical axis grow larger than those of an optimized electron lens. Such excessive refraction angles result in the generation of geometric aberrations.

Various methods that involve the use of electron lenses that are not axis symmetrical or non-spherical in the EB optic system have been presented for the correction of aberrations. While some systems use a magnetic/electrostatic objective lens[28–30], others use multipole compensation lenses[31–33]. In the former, a retarding electric field produced by an electrostatic lens and

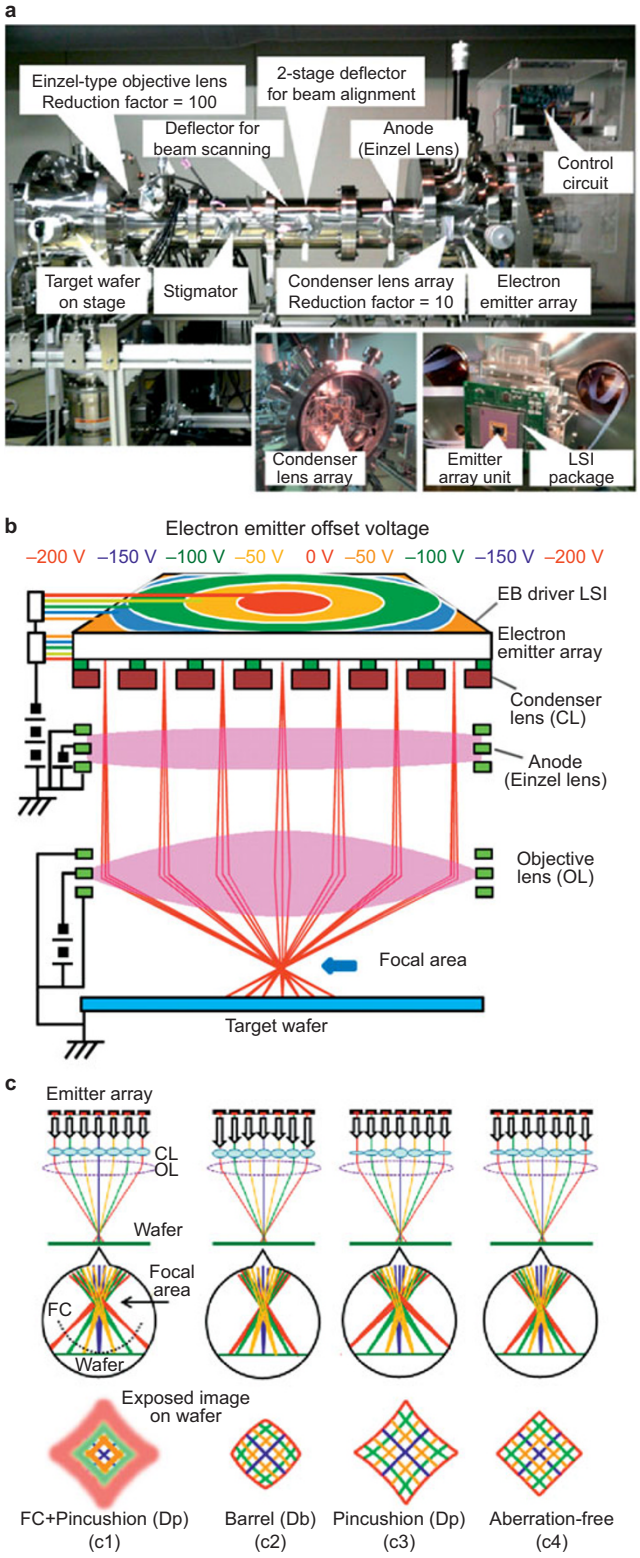

Figure 1 (**a**) Photograph of the MPEBDW system. (**b**) Electron reduction optic system. (**c1**) Electron beamlet trajectories without aberration corrections. (CL, condenser lens; OL, objective lens). (**c2**) Aberration correction through the control of electron beamlet accelerations in conjunction with the emitter array. (**c3**) Aberration correction by adjusting electron beamlet focal lengths in conjunction with the condenser lens array. (**c4**) Aberration correction through a combination of Figure 1c2 and c3.

magnetic objective lens corrects the refraction angle by repelling beamlets with a negative electric field. In the latter, the electromagnetic field of a pseudo-concave lens produced by combined multi-poles corrects aberrations of the objective lens. These complex lens systems increase column sizes and thus cannot be used in our system.

In our system, the objective lens was set to 70 mm (diameter) to install 12 electron optic columns in the target commercial system. The diameter of the electron optic column is 70 mm, which is same as that of the objective lens. This is only five, i.e., 70 mm/($\sqrt{2}\times$10 mm), times larger than the diagonal length of the electron emitter array. As the size of the objective lens is relatively small compared to that of the electron emitter array, the aberration increases considerably (mainly as a result of the objective lens) when a conventional electron optic column is applied.

Via experimental evaluation, the largest refraction angle of the 5-keV electron beamlet positioned far from the optical axis, i.e., $\sqrt{2} \times 5$ mm from the optical axis, was measured by projecting the beamlet onto a fluorescent screen placed in the target wafer position. The resulting angle was 7% larger than the refraction angle of an ideal aberration-free lens. The aberration was eliminated by applying 140 eV of electrostatic energy onto the emitted electron. The largest refraction angle of the beamlet was also simulated using the finite element method, and similar results were found.

We propose an aberration correction method that involves the use of electron optics, such as a non-spherical Fresnel lens, to enable the use of a 70 mm (diameter) objective lens in a multi-column system. The electron optics include an Einzel-type objective lens, an electron emitter array and a condenser lens array. Both the electron emitter array and condenser lens array are divided into concentric rings. Aberrations in the refraction angle were corrected for by applying voltages to each ring. A power supply circuit was designed to produce appropriate voltages for each ring shown in the upper section of Figure 1b. The circuit covers experimentally derived 140 eV electrostatic potential energy to correct the aberration. Because aberration magnitude increases with cubed distance from the optical axis, the ring widths grow narrower with increasing their radius.

Aberration correction by an electron emitter array integrated with an active-matrix-driving LSI

As noted in the previous section, an electron emitter array and condenser lens array are used to correct aberrations. In the prototype system, they were separated into five concentric rings as shown in Figure 1b[9–11,34,35].

Figure 1c1 shows the FC and a pincushion-type distortion (Dp) without any aberration correction. We recommend employing two methods to correct these aberrations: (1) compensate for objective lens refraction angles by controlling electron acceleration levels, and (2) compensate for beamlet focal lengths by adjusting the effective thickness of condenser lenses.

Reducing the FC by adjusting electron acceleration levels (method (1)) results in barrel-type distortion (Db) as shown in Figure 1c2.

In contrast, adjusting the effective thickness of condenser lenses (method (2)) retains the Dp as shown in Figurer 1c3.

When methods (1) and (2) are applied together, the FC and Dp are corrected as shown in Figure 1c4.

PROTOTYPE NC-SI EMITTER ARRAY AND EMISSION CHARACTERISTICS

Structure and function

Figure 2a[9,12] shows the structure of the prototyped nc-Si emitter array unit. The emitter array is fabricated on an Si substrate,

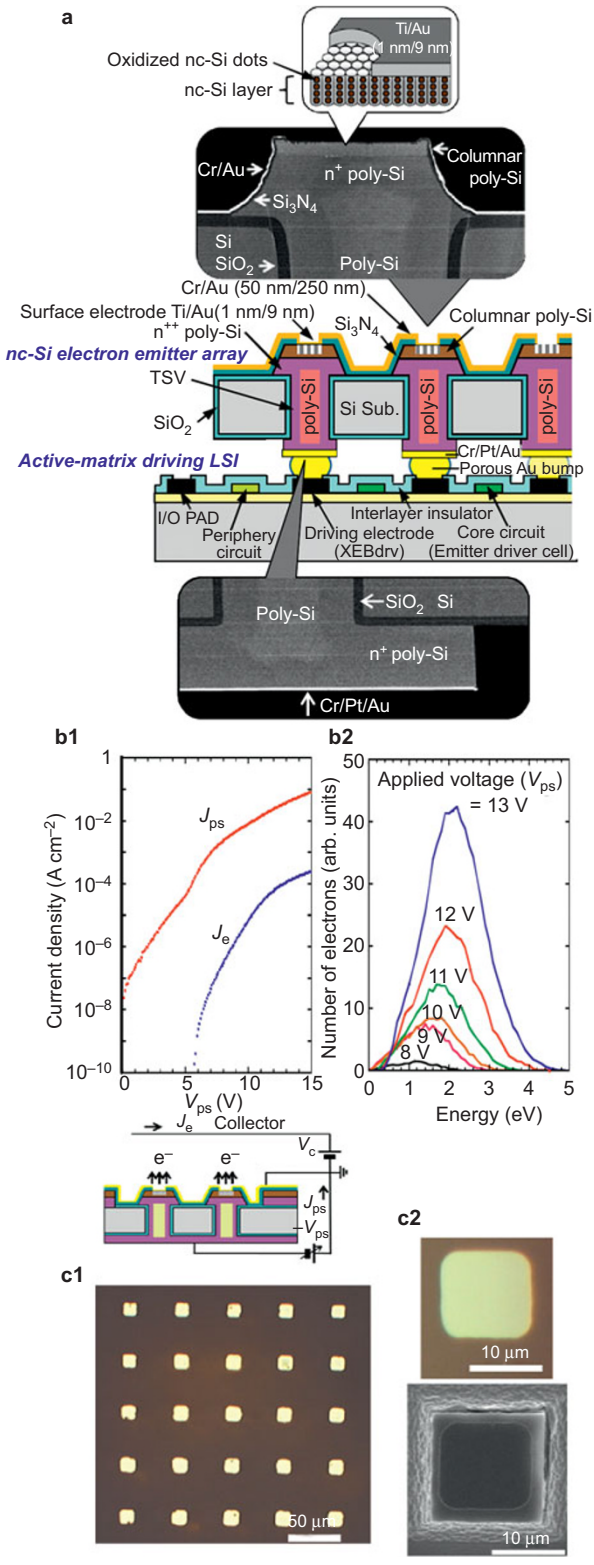

Figure 2 (**a**) Nc-Si electron emitter array integrated with an active-matrix-driving LSI. (**b1**) Features of diode current density *Jps* and corresponding emission current density *Je* vs. applied voltage *Vps*[9]. (**b2**) Bias voltage dependence of the energy distribution of electrons emitted onto a vacuum from the nc-Si emitter array at room temperature[9]. (**c1**) Pattern image exposed by an arbitrarily selected 5 × 5 subset from the 200 × 200 electron emitter array, each with a 12 × 12 μm^2 emission area[9]. (**c2**) Magnified exposed pattern image selected from the 5 × 5 subset and SEM image of the corresponding emitter, juxtaposed for comparison[9].

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and each emitter is connected to an electron emitter driver cell on an active-matrix-driving LSI through a through-silicon-via (TSV) and porous Au bump. Each emitter has an active area of 10 × 10 μm^2 for electron emission at Si_3N_4 passivation film openings.

A Pierce electron gun nc-Si emitter array is also being prototyped. Each emitter covers a larger emission area to accommodate higher beamlet currents and is concave in shape to independently converge electron beamlets without the use of a condenser lens[36,37].

Fabrication process

Fabrication process flows of the electron emitter array and the unit integration methods are explained as follows[9,12].

(1) The TSV array is generated by via-first-process. A 100 × 100 array of holes is created on a Si substrate via deep-reactive-ion-etching (deep-RIE), and this substrate is oxidized to form a SiO_2 layer for electric isolation. Two phases of low pressure chemical vapour deposition (LPCVD) are realized for poly-Si deposition for the generation of a TSV conducting plug. By the first phase of LPCVD, the poly-Si is deposited on a wall in holes and is then doped by diffusion to form n^{++}-poly-Si for reducing plug resistivity levels. A second LPCVD phase is realized for hole filling and depositing top and base of the plug. Then doping is conducted again to reduce resistivity levels at the top and base of the plug.

(2) Columnar poly-Si is deposited by plasma-enhanced chemical vapour deposition, and columnar poly-Si and n^{++}-poly-Si are then etched to form tapered emitters via selective RIE.

(3) A Si_3N_4 layer is deposited via LPCVD, and a Cr/Au layer is sputtered for interconnection with the surface electrode formed at a following stage (9). The Si_3N_4 layer isolates the TSV from the Cr/Au interconnection layer.

(4) Cr/Pt/Au electrodes are sputtered onto the back of the TSV.

(5) The electron emission portion of the Cr/Au and Si_3N_4 layers are removed by wet etching and RIE with CHF_3/CF_4 mixture gas, respectively, for electron emission window opening.

(6) Nc-Si dots are created in the columnar poly-Si via photo-anodization in an ethanolic hydrogen fluoride solution by galvanostatically applying an anodic pulse current on the Cr/Pt/Au rear electrode as an anode.

(7) Surfaces of the nc-Si dots are electrochemically oxidized in a mixture of aqueous ethylene glycol electrolyte and KNO_3 solution. The surface is then treated via high pressure water vapor annealing and super-critical rinsing/drying[38].

(8) The emitter array and LSI are bonded together with porous-Au bumps at 100 MPa and 150 °C for 20 min. The porous-Au bumps are made of submicron Au particles[39,40]. They absorb process-induced height differences via bump deformation[41].

(9) A thin Ti (1 nm)/Au (9 nm) layer is sputtered as a surface electrode to connect it to the Cr/Au interconnection layer for the application of surface voltage to the emitter.

Electron emission characteristics discussed in the following section are most sensitive to processes (6) and (7), which involve the development of a roughly 1-nm-thick homogeneous tunnel oxide layer that surrounds the nc-Si dots. The uniformity of tunnel oxide is affected by the previous process (6) focused on nc-Si dot development, and this results in increased oxide thickness variation levels. As a result, emission currents fluctuate. In this regard, we aim to optimize process (7) and subsequent thermal treatment processes to obtain a uniform tunnel oxide. This process-induced fluctuation in emission currents is also corrected for by the control LSI as discussed in the section "Electron emitter driver cell".

Electron emission characteristics

Figure 2b1[9] shows diode current density J_{ps} and corresponding emission current density J_e features vs. applied voltage V_{ps} levels obtained from a test structure of the nc-Si emitter array. The illustration shown under Figure 2b1 depicts the test structure and measurement circuit. The J_e plot presents electron emissions when $V_{ps} > 6$ V, that reach ~0.3 mA cm^{-2} at 15 V. The plot shows that electrons were effectively injected into the nc-Si layer from the rear n^{++}-poly-Si through the TSV plugs, drifted towards the surface, and were then ejected through the thin-surface Ti/Au electrode. A Fowler-Nordheim (F-N) plot obtained from the J_e–V_{ps} curve results shown in Figure 2b1 presents linear behaviors that cover the full range of applied voltage[9]. The J_e /J_{ps} ratio at 15 V was still <1% (see Figure 2b1), which was promising for the existence of intrinsic energy loss pathways during electron transport. However, derived linearity in the F-N plot of J_e suggests that the emissions included electrons that were quasi-ballistically transported via cascade tunnelling through interconnected nano-dots in the silicon nanowires. Figure 2b2 shows electron energy distribution curves obtained from the nc-Si emitter array at different V_{ps} levels using a hemispherical energy analyser. As was the case for typical planar surface nc-Si diode emitters, the results show distribution peaks along the high-energy side in contrast with thermalized Maxwellian distributions, thus supporting the ballistic transport model[16].

Pattern transfer characteristics

A pattern transfer experiment involving the use of a test sample with the same fabrication process discussed in the previous section was performed as an initial assessment using a test bench[9]. The sample structure was a 200 × 200 emitter array with a pitch size of 50 μm, representing the largest array size we have ever prototyped. The experiment was performed via a 1:1 exposure test bench. Emitter shapes were directly transferred onto a 50-nm-thick ZEP520 EB resist on a target wafer. The emitted electrons were accelerated at 5 keV and were then directed onto a target wafer placed 3 mm away. The nc-Si electron emitter was driven by 14 V pulses, was 250 ms in width, and had a 25% duty ratio relation to the grounded surface electrode. The target wafer was exposed to the emitted electrons until it reached a total electron dose 30 μC cm^{-2}. To suppress angle dispersion in the emitted electrons, a magnetic field of 0.56 T in parallel with the electric field was applied using two permanent magnets, causing the emitted electrons to spiral around the magnetic field lines and to focus on the target.

Figure 2c1 shows a pattern image exposed by an arbitrarily selected 5 × 5 subset of the 200 × 200 electron emitter array, each with a 12 × 12 μm^2 emission area. Square patterns from the subset were reproduced on the EB resist, though there were variations in the exposed patterns associated with the incomplete uniformity of the electron emission current. Figure 2c2 shows a magnified exposed pattern image selected from the subset (shown above) and a scanning electron microscope image of the corresponding emitter (shown below), juxtaposed for purposes of comparison. The profile shape of the emitter was

precisely transferred without any distortion or fluctuation, denoting that energy dispersion levels were minor.

Furthermore, to make a preliminary evaluation as to whether the emitter array can be selectively switched, the array was externally driven as a 600 μm-pitch 17 × 17 active matrix using commercially available display driver LSIs. The array was assembled with a low temperature co-fired ceramic[41] multilayer wiring board under the same bonding conditions described in the section "Fabrication process" (process (8)). As a result, 1:1 transferred patterns were observed.

AN ACTIVE-MATRIX-DRIVING LSI FOR THE MPEBDW

Outline of the LSI

The LSI of the MPEBDW system consists of two regions: a core and periphery region, as shown in Figure 3a. It was fabricated through a 0.18-μm CMOS high-voltage process that involved integrating 1.8 V/5 V/32 V transistors onto a single chip[34].

The LSI inputs 128 bit-wide writing bitmap data from outside into 128 shift registers of approximately 80 bit long. After all 100 × 100 bitmap data are shifted inward, they are transferred to temporal memory in each electron emitter driver cell. They then guide electron emitter activity according to the bitmap data. While driving emitters based on existing data, bitmap data are inputted in a pipe-line manner for speed operation. The LSI can compensate for electron emission variations between emitters for accurate electron dose control over the array by adjusting each driver's exposure time.

The LSI shifts in the bitmap data by 100 MHz and can update 100 × 100 bitmap data within 1 μs to meet the 2-μs exposure-time/shot (T_{shot}) level required for the prototype system shown in Table 1.

The core region (10 × 10 mm^2) consists of 10 000 electron emitter driver cells that are laid out with a 100-μm pitch as a 100 × 100 array to match the electron emitters as shown in Figure 2a. The driver cells are separated into five concentric rings so that different offset voltages can be applied onto each ring for aberration correction as discussed above. Approximately 80 driver cells are connected as a shift register to shift the bitmap data serially into the driver cells, and 128 shift registers are positioned on the LSI. In turn, the number of input pins required to transfer bitmap data onto the LSI was greatly reduced for assembly into a smaller package.

The periphery region consists of 430 pins for input/output signals and power supplies, level shifters for converting 5 V input signals into 1.8 V and 15 V signals required for the core region, and a sensor for measuring LSI temperatures.

The LSI of the prototype system has following functions:

(1) Drive the electron emitter while inputting writing bitmap data in a pipeline manner for higher throughput.
(2) Operate the electron emitter at up to 17 V, with each driver capable of selecting one of the four electron emission periods to compensate for electron emitter variation. From this function, emitter electron emission current variations can be equalized, and appropriate dose exposure to the target wafer is realized.
(3) Output electron emitter-driving signals to monitor and test LSI functioning.
(4) Provide vacant spaces for isolation between rings for the application of different offset voltages for aberration correction on each ring. Driver cells are grouped into five aberration correction rings with dedicated signals and powers.

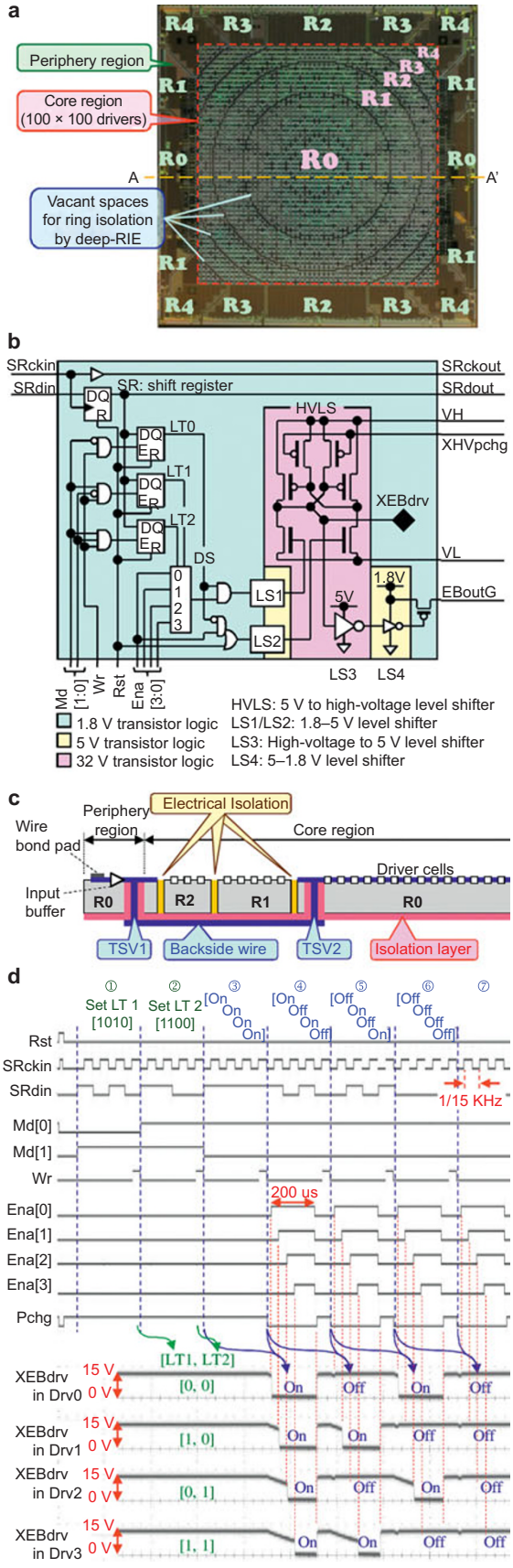

Figure 3 (**a**) Photograph of the active-matrix-driving LSI. (**b**) Electron emitter driver cell. (**c**) Cross section of the LSI after ring isolation and rewiring. (**d**) Functional operation of the LSI.

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Circuit operations of (1), (2), and (3) are described in the section "Electron emitter driver cell", aberration schemes are described in the section "Ring isolation for aberration correction", and the actual operation of the LSI is described in the section "LSI operation".

Electron emitter driver cell

This section presents structure of the LSI and the system initialization and electron emitter-driving circuit operation approach.

The driver cell is shown in Figure 3b. Approximately 80 driver cells are cascaded to form a shift register SR, and data from SRdin are shifted over the cells as a shift register SR. Each cell has a bonding pad XEBdrv for bonding with each electron emitter on the emitter chip, and the surface electrode of the electron emitter is connected to the VH. The electron emitter is turned on for emission by XEBdrv = VL or is turned off by XEBdrv = VH. As the XEBdrv is driven by a high voltage level shifter (HVLS) using 32 V transistors, the emitter is driven at up to 17 V. Transistor sizes for electron emitter operation were determined by measuring I/V characteristics and stray capacities of the electron emitters. $\Delta V/\Delta I$ and stray capacitance levels were set to 150 MΩ and 0.2 pF, respectively, at the emitter-driving voltage stage. The electron emitter driver cell was set up based on values that fit the transistors within a 100 × 100 μm^2 driver cell area.

When initializing the MPEBDW system, emission currents of each electron emitter are measured by activating only one driver cell in the array. An external controller then determines a 2-bit code for each emitter based on measured emission variation levels. The code is shifted into the shift register SR and is transferred to LT1 and LT2 in each cell by setting mode signals Md[1:0] as "10" and "11", respectively. The two-bit code in the LT1 and LT2 selects one of the four rising edge timings of Ena[3:0] to compensate for emitter emission current variations.

Following initialization, Md[1:0] is set to "00" for lithography. Writing bitmap data are shifted into the shift register SR and are transferred to LT0. When LT0 = "1", electron emissions are triggered by a rising edge Ena[3:0] selected via LT1/LT2 and shutoff by XHVpchg = VL. When LT0 = "0", emissions are blocked by Ena[0] = "1".

The electron emitter-driving signal at XEBdrv is level shifted by level shifters (LS3 and LS4), is wired-OR with other cells following a transistor, and is then outputted from the LSI. An electron emitter-driving signal can be monitored by activating only one cell in the LSI.

Ring isolation for aberration correction

This section presents a way to isolate electron emitters between aberration correction rings on the LSI.

The LSI must be fabricated by a sufficiently fine process to integrate 10 000 driver cell circuits within 10 × 10 mm . For aberration correction purposes, concentric rings in the core must be electrically isolated in order for different ring offset voltage levels to be applied. The maximum offset level is roughly 200 V. However, an LSI that allows for both a sufficiently fine process and appropriate withstand voltage levels have not been developed. We thus designed the LSI using a sufficiently fine process, and we planned to isolate the concentric rings using a post-process[34,35] based on deep-RIE. Peripheries related to the rings were also isolated. As a result, rings R0 and R1 in the core and periphery were electrically isolated. Figure 3c shows the left-hand portion of cross section A-A' in Figure 3a. To electrically connect R0 (and R1) circuits between the core and periphery, TSV1 and TSV2 are placed in the periphery and core regions, respectively, and electrical interconnections are created on a back of the LSI.

LSI operation

This section presents the experiment results of an actual LSI operation.

Figure 3d shows a case of LSI operation. LSI operations were successfully confirmed by observing XEBdrv outputs with an oscilloscope. Such observations were carried out by introducing required input signals and power supplies to the LSI, and VL and VH were connected to ground and DC 15 V power supplies, respectively. As the input capacitance of the oscilloscope probe (10 pF) was larger than the actual electron emitter capacitance (0.2 pF), a test was performed at a low rate: 200 μs pulse width (actual target exposure time of 2 μs) and 15 kHz SRckin frequency (actual target of 100 MHz). Only the first four driver cells (Drv0 through Drv3) on the shift register were driven.

First, series of data for LT1/LT2 were shifted serially at ①/②, and LT1/LT2 were initialized on the Drv0 through Drv3 at ②/③. Writing bitmap data were then introduced serially during ③ through ⑥ , and 15 V amplitude pulses with different pulse widths based on the selected Ena[3:0] were observed on XEVdrv bond pads in Drv0 through Drv3 at ④. Furthermore, 15 V amplitude pulses that were switched on/off according to the writing bitmap data were observed at ⑤ ⑥ ⑦. Active matrix operations and high-voltage amplitudes with variable pulse widths for the delivery of appropriate electron doses to compensate for emission current variations were confirmed for the LSI.

SUMMARY

This paper reviews the current status of MPEBDW lithography system development. The system is unique in its utilization of an electron emitter array that is controlled by a CMOS LSI as an active matrix operation.

Specifications of the MPEBDW as a target commercial system for the next generation of lithography were proposed and compared with a prototype system under development. The nc-Si electron emitter array employed as an electron source serves as a key feature for the realization of such specifications. Current emission density level increases via the optimization of tunnel oxide fabrication processes and issues of electron emitter array densification are critical to the realization of higher throughput levels.

The current development status of each component of the prototype system was described. Electron optics were examined for aberration corrections conducted by adjusting acceleration levels and focal lengths of the electron beamlet.

An nc-Si electron emitter array with TSV was fabricated and is planned to be hetero integrated with the LSI. From the preliminary exposure experiment, a uniform 1:1 exposure level for the emitter array was confirmed. Based on these results, we extend our work on the prototype system using an emitter array that is hetero-integrated with the LSI. The system can compensate for electron emission variations and can correct aberrations electronically.

Core MPEBDW system technologies were created. We will create the system by synergistically combining the core technologies developed. Multi-column MPEBDW system development through the miniaturization of an electron optic column is also being planned. This system supports mask-less lithography that achieves a practical level of throughput for future mass production and commercial semiconductor manufacturing. This approach reduces recently increasing photomask costs associated with cutting-edge LSI use while enabling high-mix, low-volume production and reducing development turnaround periods, and costs.

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COMPETING INTERESTS

The authors declare no conflict of interest.

REFERENCES

1 Chang THP, Kern DP, Muray LP. Arrayed miniature electron beam columns for high throughput sub-100 nm lithography. *Journal of Vacuum Science & Technology B* 1992; **10**: 2743–2748.
2 McCord MA, Petric P, Ummethala U *et al.* REBL: Design progress toward 16 nm half-pitch maskless projection electron beam lithography. *Proceedings of the SPIE* 2012; **8323**: doi: 10.1117/12.919744.
3 Freed R, Gubiotti T, Sun J *et al.* Reflective electron-beam lithography: Progress toward high-throughput production capability. *Proceedings of the SPIE* 2012; **8323**: doi: 10.1117/12.916090.
4 Klein C, Loeschner H, Platzgummer E. 50 keV electron multibeam mask writer for the 11 nm HP node: First results of the proof of concept tool (eMET POC). *Proceedings of the SPIE* 2012; **8323**: doi: 10.1117/12.916613.
5 Hakkennes EA, Wiersma AD, Hoving M *et al.* Demonstration of real-time pattern correction for high-throughput maskless lithography. *Proceedings of the SPIE* 2011; **7970**: doi: 10.1117/12.881482.
6 Doering HJ, Elster T, Klein M *et al.* Optimization of MSB for future technology nodes. *Proceedings of the SPIE* 2012; **8323**: doi: 10.1117/12.916394.
7 Liu ED, Tran C, Prescop T *et al.* Multiple columns for high-throughput complementary e-beam lithography (CEBL). *Proceedings of the SPIE* 2012; **8323**: doi: 10.1117/12.916118.
8 Kojima Y, Takahashi Y, Takakuwa M *et al.* Study of device mass production capability of the character projection based electron beam direct writing process technology toward 14 nm node and beyond. *Journal of Micro/Nanolithography, MEMS, and MOEMS* 2012; **11**: doi: 10.1117/1.JMM.11.3.031403.
9 Ikegami N, Yoshida T, Kojima A *et al.* Active-matrix nanocrystalline Si electron emitter array with a function of electronic aberration correction for massively parallel electron beam direct-write lithography: Electron emission and pattern transfer characteristics. *Journal of Vacuum Science & Technology B* 2013; **31**: 06F703.
10 Kojima A, Ikegami N, Yoshida T *et al.* Development of maskless electron-beam lithography using nc-Si electron-emitter array. *Proceedings of the SPIE* 2013; **8680**: doi: 10.1117/12.2011553.
11 Kojima A, Ikegami N, Yoshida T *et al.* Massively parallel electron beam direct writing (MPEBDW) system based on micro-electro-mechanical system (MEMS)/nanocrystaline Si emitter array. *Proceedings of the SPIE* 2014; **9049**: doi: 10.1117/12.2046584.
12 Ikegami N, Yoshida T, Kojima A *et al.* Active-matrix nanocrystalline Si electron emitter array for massively parallel direct-write electron-beam system: First results of the performance evaluation. *Journal of Micro/Nanolithography, MEMS, and MOEMS* 2012; **11**: doi: 10.1117/1.JMM.11.3.031406.
13 Koshida N, Ozaki T, Koyama H. Cold electron emission from electroluminescent porous silicon diodes. *Japanese Journal of Applied Physics* 1995; **34**: L705–707.
14 Koshida N, Sheng X, Komoda T. Quasiballistic electron emission from Porous Silicon diodes. *Applied Surface Science* 1999; **146**: 371–376.
15 Komoda T, Sheng X, Koshida N. Mechanism of efficient and stable surface-emitting cold cathode based on porous polycrystalline silicon films. *Journal of Vacuum Science & Technology B* 1999; **17**: 1076–1079.
16 Nakajima Y, Kojima A, Koshida N. Generation of ballistic electrons in nanocrystalline porous silicon layers and its application to a solid-state planar luminescent device. *Applied Physics Letters* 2002; **81**: 2472–2474.
17 Uno S, Mori N, Nakazato K *et al.* Theoretical investigation of electron-phonon interaction in one-dimensional silicon quantum dot array interconnected with silicon oxide layers. *Physial Review B* 2005; **72**: 035337–035347.
18 Uno S, Mori N, Nakazato K *et al.* Reduction of acoustic-phonon deformation potential in one-dimensional array of Si quantum dot interconnected with tunnel oxides. *Journal of Applied Physics* 2005; **97**: 113506–113511.
19 Mori N, Minari H, Uno S *et al.* Theory of quasiballistic transport through nanocrystalline silicon dots. *Applied Physics Letters* 2011; **98**: 062104.
20 O'Keeffe TW, Vine J, Handy RM. An electron imaging system for the fabrication of integrated circuits. *Solid-State Electronics* 1969; **12**: 841–848.
21 Delong A, Kolarik V. A 1:1 MIM cathode electron-projection stepper. *Microelectronic Engineering* 1990; **11**: 359–362.
22 Poppeller M, Cartier E, Tromp RM. Hot electron emission lithography. *Applied Physics Letters* 1998; **73**: 2835–2837.
23 Hongo H, Ochiai Y, Kawaura H. Resolution of 1:1 electron stepper with patterned cold cathode. *Japanese Journal of Applied Physics* 2002; **41**: 4132–4135.
24 Kojima A, Ohta T, Ohyi H *et al.* Surface electron emission lithography system based on a planar type Si nanowire array ballistic electron source. *Proceedings of the SPIE* 2010; **7637**: doi: 10.1117/12.846343.
25 Kojima A, Ohta T, Ohyi H *et al.* Fast and large-field electron-beam exposure by CSEL. *Proceedings of the SPIE* 2011; **7970**: doi: 10.1117/12.879279.
26 Kojima A, Ohyi H, Koshida N. Sub-50 nm resolution surface electron emission lithography using nano-Si ballistic electron emitter. *Journal of Vacuum Science & Technology B* 2008; **26**: 2064–2068.
27 Kojima A, Ohyi H, Koshida N. Sub-30-nm resolution parallel EB lithography based on a planar type Si nanowire array ballistic electron source. *Proceedings of the SPIE* 2009; **7271**: doi: 10.1117/12.812933.
28 Yau YW, Pease RF, Iranmanesh AA *et al.* Generation and applications of finely focused beams of low-energy electrons. *Journal of Vacuum Science & Technology* 1981; **19**: 1048–1052.
29 Frosien J, Plies E, Anger K. Compound magnetic and electrostatic lenses for low-voltage applications. *Journal of Vacuum Science & Technology* 1989; **B7**: 1874–1877.
30 Al-Khashab MA, Hujazie NS. The electron optical performance of the Gemini lens design for low voltage scanning electron microscope. *Pure Sciences* 2011; **38**: 52–59.
31 Rose H. Outline of a spherically corrected semi-aplanatic medium-voltage transmission electron microscope. *Optik* 1990; **85**: 19–24.
32 Haider M, Uhlemann S, Schwan E *et al.* Electron microscopy image enhanced. *Nature* 1998; **392**: 768–769.
33 Zach J, Haider M. Aberration correction in a low voltage SEM by a multipole corrector. *Nuclear Instruments and Methods in Physics Research* 1995; **A363**: 316–325.
34 Miyaguchi H, Muroyama M, Yoshida S *et al.* An LSI for massive parallel electron beam lithography: Its design and evaluation. Proceedings of the 31th Sensor Symposium on Sensors, Micromachines and Applied Systems 2014; Oct 20–22; Matsue, Japan; 2014: 22pm1-A2. Japanese.
35 Kaneko R, Yoshida S, Muroyama M *et al.* Development of LSI isolating and rewiring process for providing different offset voltage to each isolated region. IEEJ Technical Meeting on Sensor and Micromachines 2014; May 27–28; Tokyo, Japan; 2014: 9–14. Japanese.
36 Nishino H, Yoshida S, Kojima A *et al.* Development of MEMS pierce-type nanocrystalline Si electron-emitter array for massively parallel electron beam direct writing. Proceedings of the IEEE International Conference on Micro Electro Mechanical Systems (MEMS) 2014; Jan 26–30; San Fransisco, CA, USA; 2014: 467–470.
37 Nishino H, Yoshida S, Kojima A *et al.* Fabrication of pierce-type nanocrystalline Si electron-emitter array for massively parallel electron beam lithography. *IEEJ Transactions on Sensors and Micromachines* 2014; **134**: 146–153. Japanese.
38 Gelloz B, Kojima A, Koshida N. Highly efficient and stable luminescence of nanocrystalline porous silicon treated by high-pressure water vapor annealing. *Applied Physics Letters* 2005; **87**: 031107.
39 Ogashiwa T, Shibutani T, Miyairi M *et al.* Low temperature bonding technique using sub-micron Au particles. *Journal of the Japan Institute of Electronics Packaging* 2007; **10**: 560–566. Japanese.
40 Ishida H, Ogashiwa T, Yazaki T *et al.* Low-temperature wafer bonding for MEMS hermetic packaging using submicron Au particles. *Transactions of the Japan Institute of Electronics Packaging* 2010; **3**: 62–67.
41 Tanaka S, Mohri M, Ogashiwa T. Electrical interconnection in anodic bonding of silicon wafer to LTCC wafer using highly compliant porous bumps made from submicron gold particles. *Sensors and Actuators A* 2012; **188**: 198–203.