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ORIGINAL ARTICLE

Using binary resistors to achieve multilevel resistive switching in multilayer NiO/Pt nanowire arrays

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Reliable multilevel resistive switching in nanoscale cells is desirable for the wide adoption of resistive random access memory as the next-generation nonvolatile memory. We designed NiO-based cells in arrays of multilayered NiO/Pt nanowires to explore multilevel memory effects. Nonpolar resistive switching reproducibly occurs with significantly reduced switching voltages, narrow switching voltage distributions and a robust multilevel memory effect. A high resistance ratio ($\sim 10^5$) between the high- and low-resistance states in nanoscale cells enables stable multilevels that can be induced easily by a series of pulsed voltage. The existence of intermediate resistance states in NiO/Pt nanowire arrays can be well explained by the binary-resistor model combined with energy perturbations induced by the pulse voltage. We also verified that the conduction mechanism in multilayered NiO/Pt nanowires is dominated by the hopping of holes. Our bottom-up approach and proposed mechanism explain the controllable multilevel memory effect and facilitate sound device design to encourage their universal adoption.
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Keywords: binary-resistor; multilayered nanowires; multilevel memory effect; NiO; nonpolar resistive switching

INTRODUCTION

Resistive random access memory has attracted considerable attention as a promising candidate for the next-generation nonvolatile memory because of its excellent memory characteristics, which are superior to existing memory technologies.[1–3] Utilizing resistive switching between a low-resistance state (LRS) and high-resistance state (HRS), resistive random access memory serves as a potential alternative to the current flash memory for ultrahigh-density storage. Although resistive switching has been observed in various transition metal oxides,[4–13] the microscopic mechanism is not yet fully understood, which may limit its use in the integrated circuit industry. The primitive filament model[1] provided the first sketch for the conduction mechanism and stimulated later theoretical investigations[5,11,14,15] meant to elucidate various switching phenomena. Among these models, it is widely accepted that resistive switching correlates with the formation and rupture of conducting paths due to voltage-driven migration of ion or oxygen vacancies.[16] Such an oxygen-ion-transport model is quite applicable to *n*-type metal oxide systems with either bipolar or unipolar switching.[17]

Furthermore, the recent observation of multilevel resistive random access memory[10,18–20] at the sublithographic scale in a single resistive switching cell provides a pathway to achieving ultrahigh-density memory. The multilevel memory effects occur through the formation and rupture of conducting paths with different widths and/or quantities. However, it is quite challenging to quantitatively control the width and/or number of conducting paths in oxides, especially when the cell size is large. Note that further scaling down beyond the lithographic limit is challenging when using the conventional top-down approach.[21–23] Here, via an alternative bottom-up approach, we demonstrate nonpolar multilevel resistive switching using multilayered NiO/Pt nanowire arrays. Robust and repeatable multilevel memory effects are achieved by voltage-pulse manipulations. Resistance switching between different states is well captured by a simple binary-resistor model based on the hopping conduction of holes via defects. Our self-assembled approach provides a clear understanding of multilevel resistive switching in a large number of nanoscale cells.

The bottom-up method for constructing nanowires based on a self-assembly mechanism provides a promising platform to fabricate nanoscale devices.[6,20,24] However, most nanowire-based devices exhibit large switching voltages and distributions,[24] which may partly result from the large distance between two electrodes.[12] To overcome these shortcomings, we previously developed multilayered NiO/Pt nanowire arrays with controllable and reproducible resistive transitions.[25] The random conducting paths[7] can be suppressed in multilayered NiO/Pt nanowire arrays because of the reduced lateral

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dimension in nanowires and the shortened effective electrode distance caused by the Pt insertion. The multilayered NiO/Pt nanowire arrays can be treated as a large number of conducting units connected in series (within each nanowire) and in parallel (nanowire arrays). In consequence, uniform nonpolar resistance switching is realized with a narrow distribution of the switching voltages, and robust multilevel memory effects are achieved by repeatable voltage-pulse manipulations that tune the binary resistors in each NiO segment.

EXPERIMENTAL PROCEDURES

Schematic illustrations of the fabricated multilayered NiO/Pt nanowire-based devices are shown in Figure 1a. First, the anodic aluminum oxide (AAO) templates were prepared by two-step anodization of Al sheets.[26] The multilayered Ni/Pt nanowires were then prepared within the AAO templates by cyclic alternate electrodeposition in a sulfate bath containing $NiSO_4 \cdot 6H_2O$ (2 M), H_2PtCl_6 (0.002 M) and H_3BO_3 (0.5 M). The detailed experimental procedures were reported in Huang *et al.*[25] After electroplating, 10 wt% H_3PO_4 was used to enlarge the pore size of AAO, which can increase the empty space between nanowires and AAO so that oxygen can react with the nanowires during the subsequent annealing process. Nanowires were subsequently annealed in air for 6 h at 800 °C to obtain multilayered NiO/Pt nanowires.

The Pt top electrode with a thickness of 60 nm and a diameter of 200 μm was deposited by sputtering using a shadow mask for the resistive switching measurements of nanowire arrays. The aluminum sheet below the AAO template was used as the grounded bottom electrode. To construct single nanowire devices, the nanowires were liberated by dissolving AAO with 5 wt% NaOH. Next, the nanowires were collected by centrifugation and redispersed into isopropanol. The nanowire suspension was then transferred onto a heavily doped *n*-type Si substrate with a thermally grown 500-nm-thick SiO_2 layer.

We used electron beam lithography and the lift-off process to define the electrode patterns on the substrate, followed by a deposition of Pt/Ti (50 nm/150 nm) using evaporation. The resistive switching measurements were performed by using a Keithley 4200 semiconductor characterization system. This single nanowire device was also studied in the configuration of a planar nanowire back-gate field-effect transistor device with metal contacts functioning as source and drain electrodes, and a thermally grown 500-nm-thick SiO_2 layer as the back gate. The field-effect characteristics were measured and evaluated.

RESULTS AND DISCUSSION

A pore diameter of 70 nm and interpore distances of 90 nm were obtained with as-made well-ordered AAO templates that defined the diameter of nanowires and the number of nanowires connected in parallel under a single Pt electrode. X-ray diffraction patterns of the annealed samples show that multilayered Ni/Pt nanowires completely transform to multilayered NiO/Pt nanowires.[25] The image of a single multilayered NiO/Pt nanowire obtained with a high-angle annular dark-field transmission electron microscope is shown in Figure 1b. The multilayered NiO/Pt NWs are polycrystalline with thicknesses of each NiO and Pt segment of ~50 and 10 nm, respectively. When alternating electrodeposition is repeated for 100 cycles, a single multilayered nanowire can be considered as 100 NiO cells connected in series.

We measured the resistance-switching characteristics in multilayered NiO/Pt nanowire arrays containing $\sim 10^6$ nanowires in a parallel arrangement estimated by the areal density of AAO and the diameter of the top electrode (200 μm). As each nanowire contains ~100 NiO cells in series, the total number of resistive switching cells is estimated to be 10^8. Before conducting regular measurements, a relatively large voltage of ~15 V is used to initialize the device[27] for the subsequent resistive switching. Figure 2a shows typical current–voltage (*I–V*) curves of the multilayered NiO/Pt nanowire arrays in either unipolar or bipolar operations with a compliance current of 0.1 mA.

Switching from the low-resistance 'ON' state to the high-resistance 'OFF' state (RESET process) occurs at the reset voltages $V_{RESET} = 1.15$ V and $V_{RESET} = -1.20$ V in the unipolar ($1 \rightarrow 2$) and the bipolar ($1 \rightarrow 3$) operations, respectively, whereas the resistance transition from the HRS to LRS (SET process) occurs at a higher voltage $V_{SET} = 3.25$ V. The resistive switching characteristics indicate that nonpolar switching between the HRS and LRS is achievable regardless of voltage polarity. Similar behaviors have been observed in some thin-film systems,[9,28] suggesting the conducting behavior of nanowire arrays may be related to the energy-assisted rupture of conducting paths.

This voltage-induced resistance change is not observed in the blank AAO matrix with voltage sweeping to 18 V (see Supplementary Information S1). Therefore, we confirm that this reversible resistive switching behavior is contributed only by the multilayered NiO/Pt nanowires. This resistive switching behavior is highly reproducible in either unipolar or bipolar operations with a resistance ratio (HRS/LRS) as high as 10^5. Such an extraordinary HRS/LRS ratio can be sustained without significant degradation at a reading voltage of 0.5 V for at least 60 cycles. A retention of $\sim 10^4$ s was observed, similar to the reported value for NiO cells[29] (see Supplementary Information S2).

The distribution of switching voltages for millions of nanoscale cells in the nanowire-array devices, shown in Figure 2b, is comparable to or even better than the reported values in NiO nanowire devices[24] and thin-film devices[30] in which distributions were obtained from a

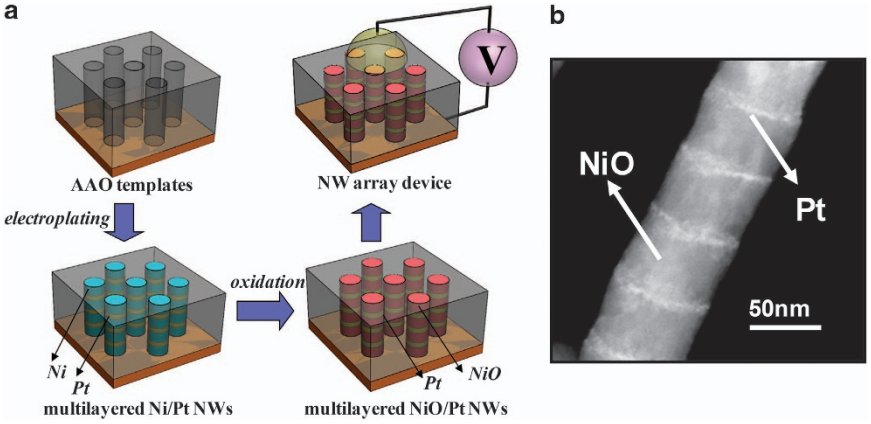

Figure 1 (**a**) The schematic illustrations for the fabrication of arrays of multilayered NiO/Pt nanowire devices; (**b**) the high-angle annular dark-field transmission electron microscope image of a single multilayered NiO/Pt nanowire. The bright and dark segments are Pt and NiO, respectively.

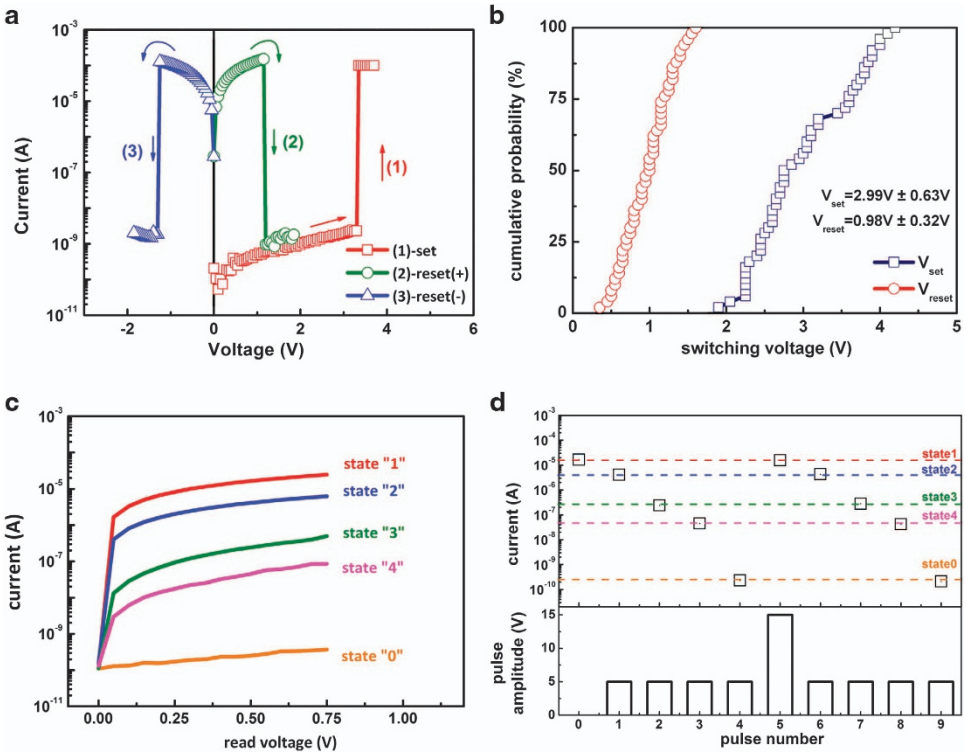

Figure 2 (**a**) *I–V* characteristics of the multilayered NiO/Pt nanowire array devices performed with DC voltage sweeping using a compliance current of 0.1 mA. (**b**) Cumulative probability of the switching voltages of multilayered NiO/Pt nanowire array devices. (**c**) *I–V* characteristics of multilayered NiO/Pt nanowire array devices after applying an increasing number of voltage pulses. The measurement starts from the LRS (state '1'), and voltage pulses with an amplitude and width of 5 V and 20 ns, respectively, are sequentially applied to change the states. State '0' represents the HRS. (**d**) The top panel shows multilevel states read at 0.5 V under different numbers of voltage pulses; the bottom panel shows the variations of the voltage-pulse amplitude with pulse number. The pulse width is fixed at 20 ns.

single cell. The conducting paths in nanowires are strongly confined due to the reduced lateral dimension. The inserted Pt layers serve as intermediate effective electrodes and allow the confined conducting paths to be reproducibly triggered by electric fields. In consequence, the switching voltages are substantially reduced with sharper distributions.[25]

Note that very few works have reported multilevel effects in nanoscale cells, especially in nanowire-based cells, mainly because the broadened distribution of the switching fields may mask the well-defined resistive states and result in irreproducible switching among them. With the narrow distribution of switching voltages, clear multilevel switching is observed in our multilayered NiO/Pt nanowire arrays, as shown in Figure 2c. Multilevel states are achieved by both unipolar and bipolar operations. The resistance state is set to the LRS (state '1') first, and then voltage pulses with an amplitude of 5 V and a duration of 20 ns are applied to the multilayered nanowire devices. It is remarkable that by applying sequential voltage pulses, we can produce a series of intermediate resistance states (labeled as state '2' to state '4') and the HRS (state '0') at the end. By applying a relatively large voltage pulse of 15 V, the device is brought from the HRS (state '0') to the LRS (state '1') again, and the cycle is completed. The pulse-induced multilevel memory effect is reproducible, as shown in Figure 2d. It is worth emphasizing that the five resistance states presented above are not the maximum limit but are given as an example. Because of the extremely large resistance ratio of 10^5, more resistance states can be deployed during design optimization.

In most reported multilevel memory effects generated by varying compliance currents or reset voltages, the multiple resistance states are believed to arise from the change in the number or sizes of the conduction filaments.[18–20] A gradual decrease in resistance is typically observed during the RESET process, consistent with the presence of multistable states explained by the filament model. It is important to stress that the operation required to reach these multiple resistance states always requires starting from either the HRS (varied compliance current) or the LRS (varied reset voltages). However, in our nanowire arrays (Figure 2), transitions between multiple resistance states can be achieved without going back to either the HRS or LRS—possibly indicating a rather different conduction mechanism.

We start with a simple 'binary-resistor' model to explain the multilevel transitions induced by voltage pulses. The device consists of N_w nanowires in parallel and N_l layers of conduction cells in series within each nanowire. When no conduction path is available, the resistance of a conducting cell (a NiO segment in our samples) is high, denoted by R. The voltage pulses help the formation of the conduction path in a cell, and its resistance drops to a much smaller value denoted by r. In real samples, one expects that the binary values R and r in each conducting cell should be different. However, if their variances are small, it is reasonable to approximate all cells with the same binary resistances. Within the binary-resistance model, the LRS of the nanowire arrays exhibits the maximum conductance $G_{max} = N_w/N_l r$, whereas the HRS shows the minimum conductance $G_{min} = N_w/N_l R$.

The transport measurement starts with the LRS. On application of one voltage pulse, it generates a finite probability p to flip the resistance of a cell from r to R. Suppose the binary-flip probability p generated by one voltage pulse is small (several percentiles in our

samples), the effect caused by n successive voltage pulses is additive and the resultant binary-flip probability is simply np. The finite binary-flip probability accounts for the inhomogeneous distribution of resistances in different cells and the total conductance G of the nanowire arrays can be computed by averaging overall possible configurations.

The resistor ratio R/r has a crucial role in generating multilevel resistive states and can be extracted from experimental data directly. For example, by using dV/dI at $V = 0.5$ V in the I–V curve shown in Figure 2a, we can obtain the resistance of the HRS and LRS. As the measured resistance of the HRS and LRS represents the resistance with the total number of R and r resistors connected in series and in parallel, respectively, the resistor ratio of R/r can be estimated rather accurately by taking the resistance ratio of the HRS to the LRS.

Voltage pulses cause conducting cells to be flipped to different resistive configurations and the total conductance of the nanowire arrays G is computed by averaging overall possible binary configurations (detailed derivations in Supplementary Information S3),

$$\frac{G}{G_{\max}} = \sum_{k=0}^{N_l} P_k g_k \approx (1-np)^{N_l} \approx e^{-N_l np} \quad (1)$$

Here, the dimensionless conductance (normalized to the maximum conductance) for a nanowire with k flipped conducting cells is $g_k = \frac{N_l}{(N_l - k) + k(R/r)}$, depending only on the resistor ratio R/r governed by the binomial probability distribution $P_k = C_k^{N_l}(np)^k(1-np)^{N_l - k}$. Because of the large resistance ratio R/r, the exact formula for the total conductance takes the simple exponential form $G/G_{\max} \approx e^{-N_l np}$, as explained next. For $k \neq 0$ terms, at least one conducting cell is flipped to high resistance R and the corresponding conductance is negligibly small. Thus, the total conductance is dominated by the $k = 0$ term in summation and the exponential form emerges, $G/G_{\max} \approx P_0 g_0 \approx (1-np)^{N_l} \approx e^{-N_l np}$. Now, we are ready to compare the theoretical prediction with the experimental data, as shown in Figure 3a. Impressive agreement is found with $p = 1.9\%$ for pulse numbers $n = 0,1,2,3$, giving rise to four robust multilevel resistive states. Note that the disagreement for the $n = 4$ case is expected, because the exponential form no longer holds and all conducting channels are flipped, bringing the nanowire arrays to the HRS with the highest resistance. The schematic diagram of the proposed binary-resistor model is shown in Figure 3b. Another set of experimental data obtained using voltage pulses with an amplitude of 12 V and a duration of 20 ns shows the same impressive agreement between experiment and theory (Supplementary Information S4).

The binary-resistor model certainly has its limitations. In our model, the transwire conduction from one wire to the other nearby wires is not included. If the transwire conduction is important, the exponential suppression of the total conductance will be gone, because the current cannot be easily blocked. Judging from the exponential decay of the total conductance observed in our samples, it is safe to say that the transwire conduction has a minor role here. In addition, because of the multilayer structure separated by metallic insertion (Pt), the conduction path formation in each conducting cell (NiO) is rather simple. Therefore, the resistance is R without a conduction path and r ($\ll R$) in the presence of a conduction path. Suppose we elongate the length of the conducting cell or enlarge the diameter of the nanowires, it is expected that the formation of conduction paths will be more complex and that the simple binary-resistor approximation will fail eventually. Therefore, the multilayer structure in nanowires has a crucial role in making the binary-resistor model a good approximation.

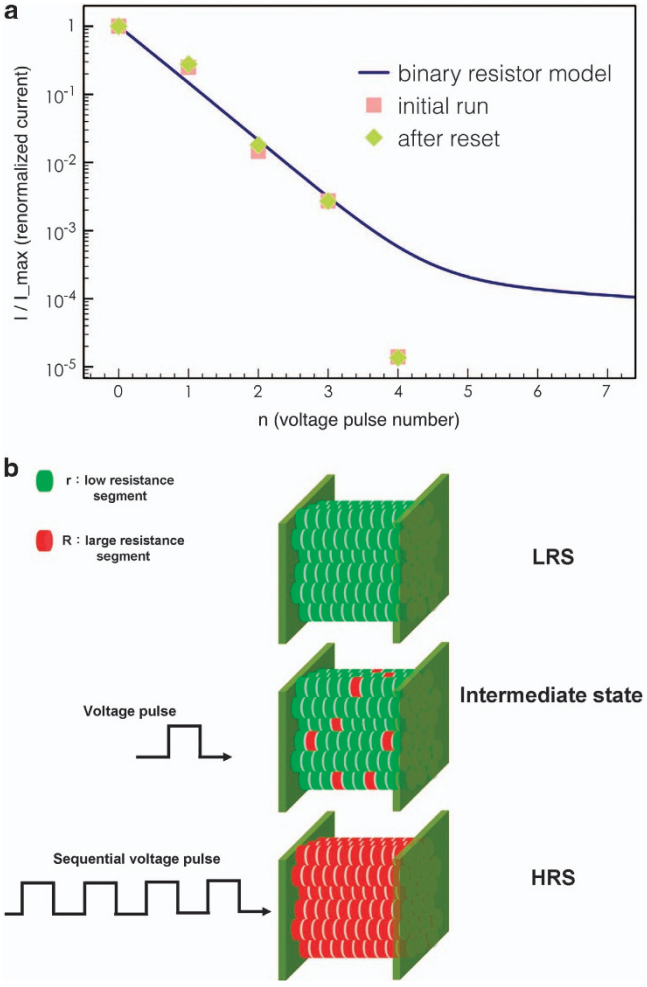

Figure 3 (**a**) Renormalized current $I/I_{max} = G/G_{max}$ versus the number of voltage pulses n. The experimental data for the initial run are shown in red squares and those for the second run after reset are shown in green diamonds. The blue curve is the theoretical prediction from the binary-resistor model. The resistor ratio $R/r = G_{max}/G_{min} = 72\,444$ is extracted from experimental data, and the estimated number of units in each wire is $N_l \approx 100$. The fitting parameter is the binary-flip probability p fitted to the value $p = 1.9\%$ here. (**b**) A schematic diagram of the multilevel memory effect induced by voltage pulses as described by the binary-resistor model.

To further verify the origin of the multilevels, we obtained I–V curves of the multilayered NiO/Pt single nanowire and single-layered NiO nanowire arrays. The resistive switching of the multilayered NiO/Pt single nanowire device under unipolar and bipolar operations (Supplementary Information S5) reveals similar results to those of nanowire-array devices, as shown in Figure 2a. This clearly indicates the good uniformity of nanowires. On the basis of I–V similarity, together with the narrow distributions of switching voltages observed in the nanowire arrays (Figure 2b), we can exclude the possibility that the multistable states observed in millions of cells originate from the variations of different nanowires. Furthermore, the resistive switching of single-layered NiO nanowire arrays revealed higher switching voltages and wider switching distributions than those of the multilayered NiO/Pt nanowire arrays, as we reported previously.[25] Notice that we do not observe the multilevel effect in either multilayered NiO/Pt single nanowire or single-layered NiO nanowire arrays, no matter how we adjust the amplitude or duration of voltage pulses.

As multilayered NiO/Pt single nanowire devices show similar *I–V* curves to those of NiO/Pt nanowire arrays but do not possess intermediate states, we can conclude that the multilevel does not exist in each NiO segment.

The binary-resistor model not only explains the observed multilevel effects in the multilayer NiO/Pt nanowire arrays but also provides the reasons why neither the NiO single-layered array nor the multilayered NiO/Pt single nanowire exhibits multiple resistance states. In the single-layered NiO nanowire array, the wire length is long, leading to the presence of the various conduction paths; therefore, they cannot simply be treated as a binary resistor. In the multilayered NiO/Pt single nanowire, just one unit flipping to high resistance will destroy the only conducting channel, and multiple resistance states are not possible. The model indicates that our multilevel memory effect reproducibly occurs in millions of cells, distinct from the reported work for single-cell devices. Our design of the multilayer nanowire arrays enables us to measure resistance switching between robust multiple resistance states controlled by voltage pulses and enjoys the flexibility of varying the number of nanowires and the layers within each nanowire. Furthermore, our synthesis method provides a versatile approach to achieve multilevels.

The multistate mechanism we report here is novel, and the key is to estimate the minimum number of wires needed to achieve the robust multilevel resistive states. By standard statistical analysis of the binary distribution (detailed derivations presented in Supplementary Information S6), the criterion for the minimum number of wires is

$$N_w \gg \frac{1}{P_0(1-P_0)}, \tag{2}$$

where $P_0 \approx e^{-N_l p}$. For the sample reported here, $p = 1.9\%$ and $N_l = 100$, giving rise to $P_0 \approx 15\%$. The criterion for the number of wires is $N_w \gg 8$. The criterion can be relaxed further if we shorten the length of the nanowires, for example, to $N_l = 50$, and the criterion becomes $N_w \gg 4$. On optimization, it is thus expected that $N_w \sim 10$ is large enough ($N_w \sim 10^6$ in our current sample) to achieve robust multilevel resistive states. The smallest AAO diameter reported in the literature is ~ 15 nm,[31] and thus a multilayered nanowire device with multilevel resistive switching can be achieved at the size of 150 nm.

Now, we would like to go beyond the phenomenological binary-resistor model and elaborate on the microscopic mechanism for resistance switching. To explain the valid conduction mechanism in nanowires, we first investigated the temperature dependence of resistance at the LRS on a single multilayered NiO/Pt nanowire in the temperature range of 85–325 K. An exponential decay of resistance versus temperature reveals typical carrier transport behavior in a semiconductor, as shown in Figure 4a, which can be fitted by a simple model as:[32]

$$R = A \exp(E_a / k_B T) \tag{3}$$

The activation energy of $E_a = 0.03$ eV is obtained from the ln(R) versus T^{-1} plot. The negative temperature coefficient and low E_a value, close to that of the high-defect NiO thin films (0.01–0.7 eV), suggest that the conduction in LRS is associated with hopping via defects.[32] Compared with the temperature dependence of the LRS of the NiO nanowire array reported in Huang *et al.*,[25] the activation energy is similar, which indicates that the inserted Pt layers in NiO nanowires behave mainly as electrodes and that the NiO segments maintain the original conduction mechanism.

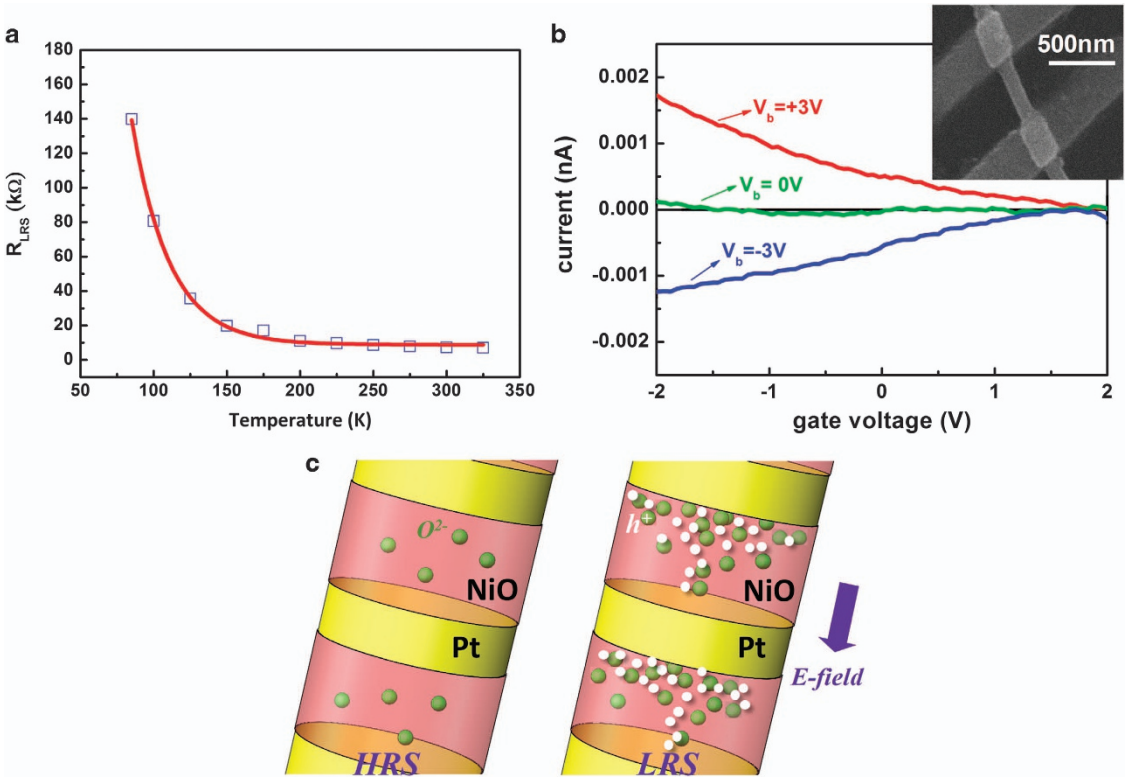

Figure 4 (**a**) Temperature dependence of the LRS resistance for a single multilayered NiO/Pt nanowire measured at 0.5 V; the solid line represents the exponential fitting. (**b**) I–V_g curves of the back-gated multilayer NiO/Pt nanowire device for bias voltage = +3 (red), 0 and −3 V (blue). Inset of **b** shows a scanning electron microscopic image of the measured device. (**c**) A schematic illustration of the conducting mechanism with migrating oxygen ions.

Bulk NiO is a well-known *p*-type semiconductor when it is nonstoichiometric and Ni deficient (or there is an oxygen excess).[33] To determine the conduction mechanism in nanowires, we use the planar field effect transistor structure to determine the carrier type.[34,35] Figure 4b shows the electrical current as a function of gate voltage (V_g) in the range from −2 to 2 V. The inset of Figure 4b shows an scanning electron microscopic image of the corresponding back-gate field-effect transistor structure of the multilayered NiO/Pt nanowires with a SiO_2 layer as the back gate oxide. Although the bias voltage is fixed, the current is modulated with varying V_g. The current amplitude with a negative V_g is larger than that with a positive V_g. This evidently indicates the *p*-type nature of multilayered NiO/Pt nanowires.

It was reported that the presence of oxygen vacancies is critical to the resistance switching of *n*-type metal oxides.[12,13] However, oxygen vacancies form the defect states at deep energy levels in NiO so that electrons in the presence of oxygen vacancies are highly localized.[36] In contrast, the energy level of Ni vacancies is near the valence band of NiO, so holes are the dominant carrier.[37–39] The field-effect transistor measurement also confirms that holes are the dominant carriers in our nanowires. Furthermore, it has been reported that oxygen ions are more mobile compared with Ni ions under electric fields.[40,41] Therefore, the movement of oxygen ions under an electric field may have a crucial role in resistance switching, even in *p*-type NiO.[37,38]

In our multilayered NiO/Pt nanowire arrays, the applied electrical field causes the oxygen ions to drift toward the anode during the SET process. The accumulated O^{2-} ions result in highly nonstoichiometric NiO (O/Ni ratio > 1) and increase the hole concentration locally near the anode side. When the applied field approaches V_{SET}, the conductive region may extend from the anode to the cathode. Thus, hopping conduction through percolated paths prevails, leading to the LRS (Figure 4c). For the bipolar RESET process, with the opposite applied electrical field, O^{2-} ions migrate back into the bulk oxide and then recombine with oxygen vacancies, leading to a reduced O/Ni ratio and hole concentration; thus, the HRS is achieved.

For the unipolar RESET process, the temperature is increased locally due to Joule heating, which accelerates the migration of O^{2-} ions to suppress the concentration gradient. No matter which operation (bipolar or unipolar) is performed, applied electric fields change the configuration of O^{2-} ions, which in turn modulate the local hole concentrations. When we apply a pulsed voltage to multilayered NiO/Pt nanowires, the resistance changes in each NiO segment are governed by the redistribution of oxygen ions and holes in NiO. By simply applying different numbers of pulsed voltages, the induced energy perturbation may reconfigure the oxygen ions and locally switch NiO segments from the LRS to the HRS. The intermediate state of resistance does not exist in each NiO segment. Instead, it results from averaging overall possible binary configurations for each NiO segment in the multilayered nanowire array, which is distinct from the reported multilevel in a single cell.

In summary, we demonstrate nonpolar resistance switching behavior in multilayered NiO/Pt nanowire arrays with low switching voltages and robust multilevel memory effects. Our bottom-up method provides a versatile approach to understand and design the resistance switching in a large number of nanoscale NiO/Pt cells and suits the study of a variety of material systems. In addition, we propose that resistance switching in these nanoscale cells correlates closely with the hopping conduction of holes. The multistable resistance states can be reliably achieved by simply applying different numbers of subsequent voltage pulses. The multilevel memory effects are well captured by a simple binary-resistor model. We anticipate that our finding may expedite the adoption of resistive memory by the memory industry.

ACKNOWLEDGEMENTS

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Supplementary Information accompanies the paper on the NPG Asia Materials website (http://www.nature.com/am)