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ORIGINAL ARTICLE

Electrically induced colossal capacitance enhancement in $LaAlO_3/SrTiO_3$ heterostructures

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The demonstration of a tunable conductivity for the $LaAlO_3/SrTiO_3$ interfaces by field effect drew significant attention to the development of oxide-based electronics. The increase in the gate capacitance of the $LaAlO_3/SrTiO_3$-based field-effect transistor is particularly important for conductivity modulation and the development of logic devices. Here, we demonstrate the annihilation of quantum capacitance and colossal capacitance enhancement (approximately 1000%) in $LaAlO_3/SrTiO_3$ heterostructures by DC gate voltage at room temperature, which we attribute to the motion of oxygen vacancies through the thickness of the $LaAlO_3$ layer. These capacitor devices will provide a platform for the further development and application of metal-oxide-semiconductor transistors.
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Keywords: capacitance enhancement; $LaAlO_3/SrTiO_3$ heterostructure; mobile oxygen vacancy; quantum capacitance; reversible capacitance switching; two-dimensional electron gas (2DEG)

INTRODUCTION

The discovery of high-mobility two-dimensional electron gas (2DEG) at the interface of two insulating oxides, $LaAlO_3$ (LAO) and TiO_2-terminated $SrTiO_3$ (STO),[1] has stimulated great interest in the development of oxide-based electronics.[2–7] In particular, LAO/STO-based field-effect devices have attracted considerable attention because the interface conductivity may be tuned using an electric field.[8–14] The tunability of the conductivity at the LAO/STO interface is closely related to the change in the capacitance of the field-effect devices.[15,16] Extensive efforts have been focused on the use of very thick $SrTiO_3$ substrates as gate dielectrics. However, extremely large turn-on voltages (hundreds of volts) are needed to switch these devices.[8,9] In another approach, a LAO thin film with a high dielectric constant ($\varepsilon_r = 18$)[17] was used in the field-effect devices, and much smaller gate biases (only a few volts) were found to be sufficient to modulate the conductivity at the interface.[3,18] The investigation of the gate capacitance of the LAO/STO-based field-effect devices using the LAO thin film as a dielectric layer is important for the quantitative understanding of the transport properties of 2DEG at the interface and the development of applications for the logic device. Recently, Li *et al.*[15] found a >40% enhancement of the gate capacitance of the field-effect transistor structure and suggested that the large quantum capacitance enhancement is related to the strong electronic correlation of 2DEG at the LAO/STO interface. Here, we present a colossal capacitance enhancement of approximately 1000% in LAO/STO-based capacitor devices at room temperature with a reversible transition between low capacitance state (LCS) and high capacitance state (HCS) under gate voltages with different polarities. We suggest one possible explanation for these behaviors in terms of the reversible modification of oxygen vacancy redistribution throughout the LAO thickness under the gate voltage.

MATERIALS AND METHODS

Growth of thin films

$LaAlO_3$ films with a thickness of 10 unit cells (u.c.) and 20 u.c. were grown on TiO_2-terminated (001) $SrTiO_3$ substrates by pulsed laser deposition using a KrF laser (Coherent, Göttingen, Germany) at 800 °C in an oxygen atmosphere of 2×10^{-3} mbar. The energy flux of the KrF excimer laser ($\lambda = 248$ nm) at the single crystal $LaAlO_3$ target was approximately 1 J cm^{-2}. During the film growth, the thickness and quality of the LAO films were monitored by *in situ* reflected high-energy electron diffraction. After the growth, the samples were cooled to room temperature at a rate of 5 °C min^{-1} under an oxygen pressure of 400 mbar to avoid oxygen vacancies.

Capacitor device fabrication and measurement

Pt electrodes with a typical area of 150×150 μm were deposited on the $LaAlO_3$ surface by sputtering through a shadow mask at room temperature, and Al electrodes were placed in direct contact with the electron gas. A Keithley 4200 SCS semiconductor characterization system (Solon, OH, USA) and an Agilent 4284 A LCR meter (Agilent, Kobe, Japan) were used to measure the capacitance, impedance spectroscopy and dielectric loss in the ambient atmosphere at room temperature.

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RESULTS

We prepared typical metal-insulator-metal capacitors in which the LAO thin films form a dielectric layer sandwiched between sputtered Pt gate electrodes and the 2DEG at the LAO/STO interface, as diagrammed in the inset of Figure 1a. The capacitance between a top gate and the interface was measured at frequencies in the range of 20 Hz to 10 MHz while varying a top gate DC voltage and reading out the capacitance with an AC voltage of 30 mV at room temperature. Figure 1a shows the capacitance versus gate voltage (C-V) curve of the capacitor device with a 10 u.c. LAO layer at a frequency of 5 kHz, which exhibits the typical characteristics of metal-insulator-semiconductor geometry. Near depletion, a sharp peak of capacitance was observed; this finding is consistent with the results reported by Li *et al.*,[15] who suggested that the capacitance upturn is associated with quantum capacitance, which is related to the strong interaction of 2DEG at the LAO/STO interface at low electron density. The effect of a strong electronic correlation of 2DEG at the GaAs/AlGaAs interface of a few percent beyond the expected geometric capacitance has also been observed.[19] In addition, a peak shift was found in the dual C-V curve, which would originate from the migration of residual oxygen vacancies near the LAO/STO interface. Oxygen vacancies, the most common defects in the LAO/STO system,[20–25] are mobile in perovskite oxides under an electric field.[26,27]

When the gate voltage amplitude was increased from 4 to 15 V, pronounced hysteretic C-V curves were observed, as shown in Figure 1b. These hysteretic C-V curves were extremely stable during the successive voltage sweeps. Here, we define the C-V branch from −15 to + 15 V with lower capacitance at zero gate voltage as the LCS and the C-V branch from + 15 to −15 V with higher capacitance as the HCS. The capacitance enhancement is defined as $100\% \times (C_H - C_L)/C_L$, where C_H and C_L are the high capacitance and low capacitance at zero gate voltage, respectively. The capacitance at zero gate voltage is enhanced by approximately 180% at 5 kHz, and the enhancement becomes more prominent with increasing gate voltage or decreasing frequency. The capacitance switching effect is dependent on the DC gate voltage polarity. There is almost no C-V hysteresis loop in the positive gate voltage region (Figure 1c) or in the negative voltage region (Figure 1d). However, the capacitance at zero gate voltage is much larger after the application of a positive gate voltage than after the application of a negative voltage. This result shows that a sufficient positive DC gate voltage enhances the capacitance or switches the capacitor device into HCS, whereas a sufficient negative gate voltage restores the capacitor to initial LCS.

To confirm that the sufficient positive and negative gate voltages switch the capacitor into HCS and LCS, respectively, we applied a train of periodic pulses of ± 15 V to the capacitor devices, as shown in the upper panel of Figure 2a. Between these voltage pulses, the LCS and HCS were read out with an AC voltage of 30 mV at frequency of 5 kHz. As expected, bistable capacitance states were achieved by applying the train of periodic pulses, as shown in the lower panel of Figure 2a. Subsequently, the stability and reproducibility of the stored capacitance states were studied in a cyclic operation. The HCS and LCS were found to be very stable, without detectable signs of degradation over 10^4 cycles, as shown in Figure 2b, demonstrating the nondestructive readout property of the capacitor with an AC voltage of 30 mV. The two states are nonvolatile, with retention of > 24 h, as shown in Figure 2c. The high capacitance switching ratio and good retention and endurance are highly significant for the design of nonvolatile devices in oxide electronics.

We further studied the thickness dependence of the quantum capacitance and capacitance switching behaviors. Supplementary Figure S2 in the Supplementary Information shows that in the small gate voltage region, a sharp peak of capacitance was also observed in the LAO/STO heterostructures with 20 u.c. LAO films. The geometric

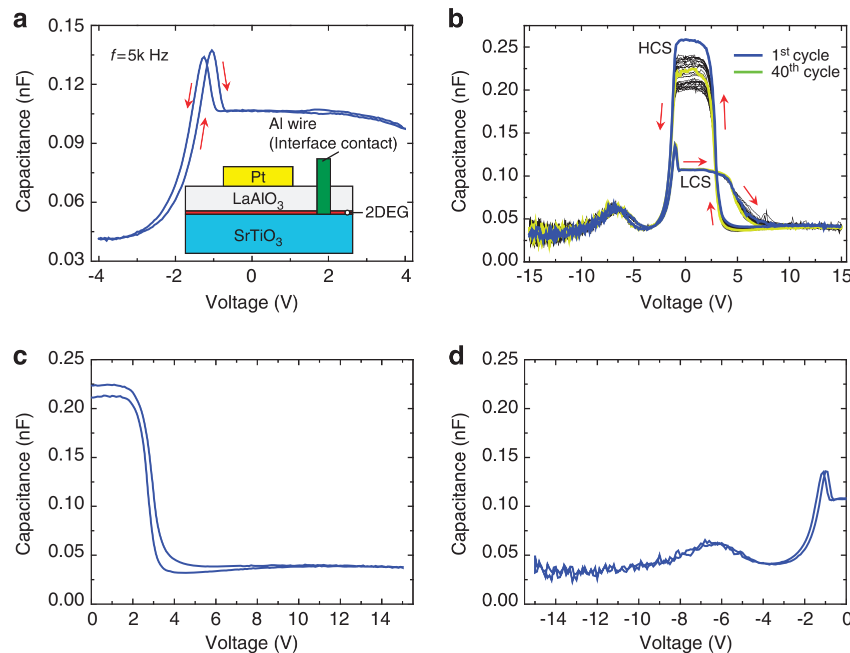

Figure 1 Colossal capacitance enhancement of $LaAlO_3$ (LAO)/ TiO_2-terminated $SrTiO_3$ (STO)-based capacitor devices with 10 unit cells (u.c.) LAO films at room temperature. (**a**) Near depletion, a sharp peak of capacitance was observed in small DC gate voltage region, which is related to electron–electron interactions at low electron density. The inset shows the capacitor device based on the LAO/STO heterostructure. (**b**) When the amplitude of the gate voltage is increased to 15 V, pronounced hysteretic C-V curves are observed. The capacitance switching effect is very stable during successive voltage sweeps. The polarity dependence of the switching effect (**c**) in the positive gate voltage region and (**d**) in the negative gate voltage region is shown.

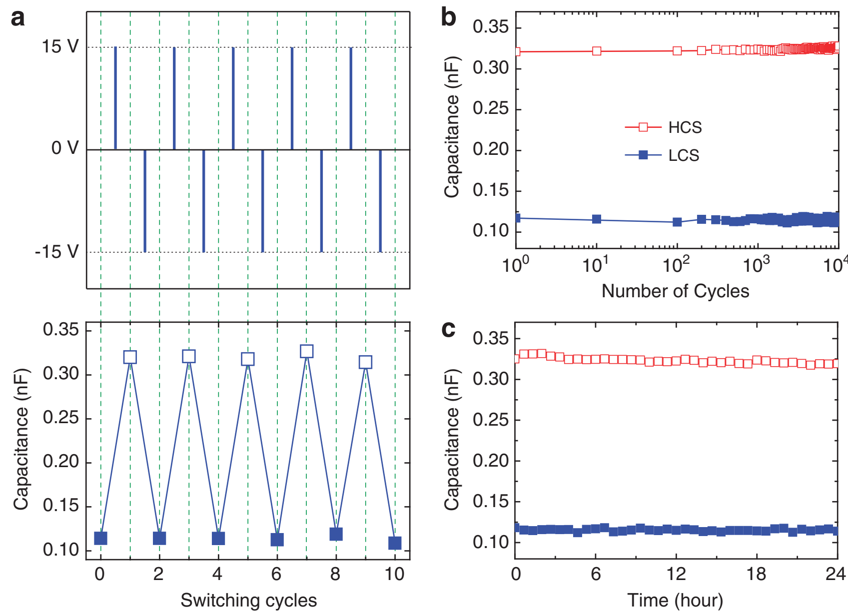

Figure 2 Nonvolatile capacitance switching characteristics. (**a**) Upper panel: a train of periodic pulses of ±15 V was used to switch the capacitor into different capacitance states. Between these voltage pulses, the LCS and HCS were read out with an AC voltage of 30 mV at a frequency of 5 kHz. Lower panel: positive gate voltage switches the device into HCS, whereas the negative voltage recovers the device to the initial LCS. (**b**) Reliable bistable capacitance states are very stable during the successive gate voltage sweeps, exhibiting a good endurance. (**c**) Both HCS and LCS are nonvolatile, with a good retention of >24 h.

capacitance $C_i = \varepsilon S/d$ of the capacitor device was reduced by approximately 50% in comparison with that of the 10 u.c. LAO film, where ε, S and d are the dielectric constant of the LAO film, the area of the cross sections of the capacitor devices, and the dielectric thickness of the LAO film, respectively. Similarly, in the large DC gate voltage region, prominent capacitance switching behavior and the annihilation of quantum capacitance were observed, as shown in Supplementary Figure S3. The capacitor devices with 20 u.c. LAO films also show good endurance and retention and even greater capacitance enhancement, of approximately 1000%, at 200 Hz compared with the devices with 10 u.c. LAO films.

DISCUSSION

The capacitance switching effect can be attributed to the redistribution of oxygen vacancies throughout the LAO film. Recent reports showed that the oxygen vacancies exist at the surface of the LAO layer in LAO/STO heterostructures,[2,3,28,29] as the LAO surface is expected to be a local energy minimum for oxygen vacancies. Bristowe *et al.*[28] presented a case for the surface redox reaction as the origin of the 2DEG with surface oxygen O^{2-} anions transforming into O_2 molecules, forming oxygen vacancies at the LAO surface and simultaneously releasing two electrons to the n-type LAO/STO interface. Cen *et al.*[2] observed the creation and erasure of nanoscale conducting regions at the LAO/STO interface using a conducting atomic force microscope probe as a gate, because of the generation and annihilation of the oxygen vacancies at the LAO surface. Recently, Bark *et al.*[29] found a switchable electromechanical response of the LAO overlayer, which they attributed to the redistribution of oxygen vacancies throughout the LAO layer thickness under an electric field. In our case, we suggest that the motion of oxygen vacancies inside the LAO layer is also responsible for the capacitance switching effect. Once the positively charged mobile oxygen vacancies are redistributed throughout the LAO film under application of the DC gate voltage, these mobile oxygen vacancies are in an unstable energy state and are mobile within the LAO under an electric field. Hence, the mobility increases the capacitance response to the AC voltage, resulting in capacitance enhancement. The negative gate voltage drives the oxygen vacancies back to the LAO surface. The oxygen vacancies could be trapped at the LAO surface, which is a local energy minimum for oxygen vacancies.[28] As the trapped oxygen vacancies fail to respond to the AC voltage, the capacitor devices should recover to the initial LCS after the application of a negative gate voltage. The mobile oxygen vacancies should show a stronger response to the AC voltage at the lower frequency because they have a longer time to be displaced. To test this hypothesis, we carried out C-V measurements of capacitor devices with 10 u.c. LAO films at different frequencies. Figure 3a shows C-V curves from 1 to 10 kHz, which demonstrate that the hysteresis became more pronounced with decreasing frequency. When the frequency increased beyond 10 kHz, no hysteretic C-V curve was observed. We also investigated the frequency dependence of capacitances in different states after applying a DC gate voltage of ±15 V, as shown in Figure 3b. Both HCS and LCS increase when the frequency decreases, while the HCS is more sensitive to the frequency than the LCS. Correspondingly, the capacitance enhancement of the capacitor devices with the 10 u.c. LAO film increases with the decrease in frequency, up to 500% at 200 Hz. The devices with the 20 u.c. LAO film show a greater enhancement, approximately 1000%, at the same frequency (Supplementary Figure S3).

To understand the mechanism of the colossal capacitance enhancement, impedance spectroscopy was carried out by applying a 30 mV AC small signal (20 Hz–10 MHz). Supplementary Figure S6a shows a semicircle in the Nyquist plot (–Im(Z) vs Re(Z)) for the LAO/STO interface, which suggests that the impedance of the interface can be represented by two circuit elements connected in parallel: one resistor, R, accounting for the conduction of the interface, and one capacitor, C, accounting for the dielectric character of the STO substrate.

The impedance spectrum of the LAO/STO interface can be fitted by the Cole–Cole function (see Supplementary Information).[30] In the Nyquist plot, the diameter of the semicircle is the resistance of the LAO/STO interface. From the fitted impedance curve, the resistance of the LAO/STO interface is extrapolated to be approximately 20 KΩ, in agreement with the sheet resistance measured in the Hall-bar configuration at room temperature (Supplementary Figure S1).

Subsequently, the impedance spectra in different capacitance states (HCS and LCS) after applying a sufficient positive/negative gate voltage were measured as shown in Supplementary Figure S6d. For both HCS and LCS, the impedance spectra exhibit two merged semicircles. The small semicircle was not altered by the application of sufficient gate voltage, and both spectra are dominated by a large semicircle, indicating that the total capacitance of the capacitor device in HCS and LCS should be determined by two contributions. The small contribution would be attributed to the interface portion, which is related to the dielectric property of STO near the LAO/STO interface, whereas the large contribution could be from the dielectric LAO layer, as diagrammed in Supplementary Figure S6c. The diameter of the semicircle in the LCS is larger than the diameter of the semicircle in the HCS because of the creation of mobile oxygen vacancies in the LAO thin film, resulting in extra capacitance because of the response of the mobile oxygen vacancies to the AC signal,[31] as shown in the equivalent circuit diagram of Supplementary Figure S6c.

The generation of mobile oxygen vacancies in the LAO thin film could also lead to increased leakage current. The increase in leakage current would affect the capacitance measurement. Here, C-V measurements were carried out with an AC signal, and the capacitance of the device was calculated with the following equation:

$$C = I/(2\pi f V_{AC}) \quad (1)$$

where V_{AC} and I are the applied AC voltage and the measured AC current (Supplementary Figure S7), respectively. Assuming that the leakage current of the capacitor increases after the application of a positive gate voltage, the measured capacitance value could also be larger than the real value. To exclude this possibility for capacitance enhancement, we investigated the dielectric loss in the different capacitance states, as shown in Figure 4. The dielectric loss tangent ($\tan\delta = 1/(2\pi fRC)$) reflects the energy loss because of the leakage current,[32] where R represents the resistance of the resistor in series with the capacitor. For the initial capacitance state (ICS) and LCS, the loss tangent is approximately 0.06 at 20 Hz, indicating that the leakage current is very low and therefore that the LAO thin films are sufficiently insulating. After switching to HCS, although the loss tangent increases because of the mobile oxygen vacancies in the LAO film, the loss tangent remains very small, approximately 0.13 at 20 Hz, indicating a low leakage current. Moreover, the loss tangents in LCS and HCS are the same, at approximately 5 kHz. Suppose that the capacitance remains constant after application of ±15 V, the leakage current does not change, and therefore no CV hysteresis could be observed. Obviously, this deduction contrasts with the capacitance switching measured at 5 kHz, as shown in Figure 2b. We also plotted the $1/(RC) \sim f$ curve in LCS and HCS to rule out the possibility of the variation of leakage current after the application of gate voltage, as shown in Supplementary Figure S7. As shown in Supplementary Figure S7, the amplitude of 1/(RC) increases greatly with frequency. The change of 1/(RC) is irrelevant to the frequency if the capacitance

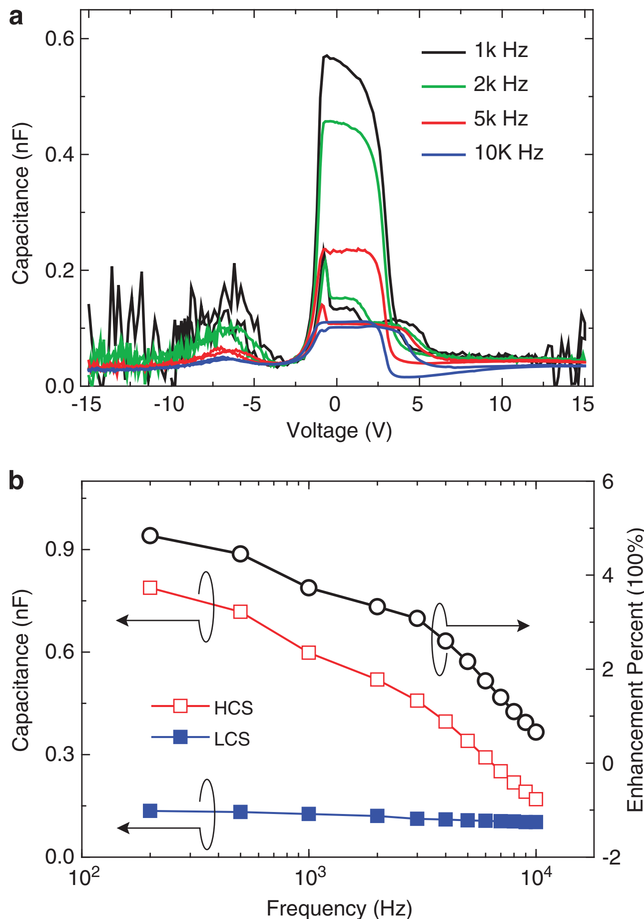

Figure 3 Frequency dependence of capacitance enhancement. (**a**) C-V curves measured at frequencies from 1 to 10 kHz demonstrate that the hysteresis becomes more pronounced with decreasing frequency. The hysteretic C-V curve almost disappears as the frequency increases beyond 10 kHz. (**b**) The HCS and LCS increases with decreasing frequency; the HCS is more sensitive to the frequency than the LCS. Correspondingly, the capacitance enhancement increases with decreasing frequency, up to 500% at a frequency of 200 Hz.

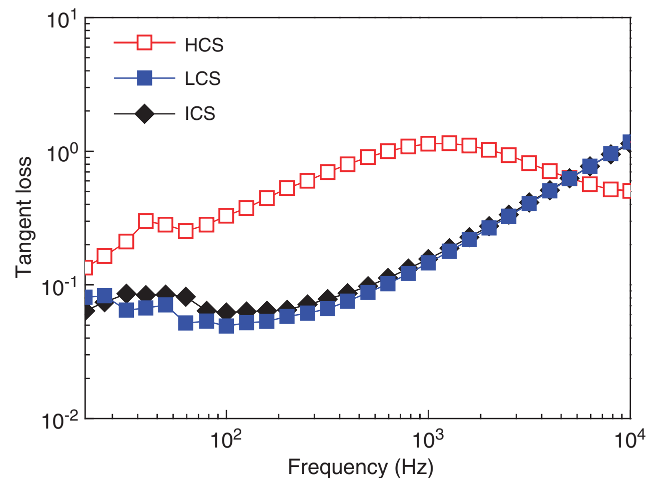

Figure 4 Dielectric losses in the different capacitance states. Regardless of whether the capacitor device is in ICS, LCS or HCS the loss tangent is very small, revealing a low leakage current. Moreover, the loss tangents in LCS and HCS are the same, at approximately 5 kHz. These results imply that the capacitance switching is intrinsic and not because of leakage current variation.

remains constant after the application of gate voltage, which is also inconsistent with the experimental results. We therefore conclude that the capacitance switching is intrinsic and not due to the variation of leakage current.

To shed light on the origin of the annihilation of quantum capacitance and the colossal capacitance enhancement, a schematic diagram of the migration of the oxygen vacancies in the LAO films after the application of gate voltages with different polarities and an equivalent circuit is illustrated in Figure 5. For the pristine capacitor devices, as shown in Figure 5a, it is reasonable to assume that positively charged oxygen vacancies are trapped at the LAO surface.[26] Under these circumstances, for the initial LCS, no extra capacitance is contributed by the response of mobile oxygen vacancies in the LAO film to the AC gate voltage. In addition to the capacitance contribution from the LAO film, we find a quite small capacitance at the LAO/STO interface because of the insulating STO layer underneath 2DEG, as shown in Supplementary Figure S4. The capacitance decreases with the increasing amplitude of the gate voltage, which could be related to the decrease in the dielectric constant of the STO substrate.[13,33] Thus, the total measured capacitance could be modeled as the in-series combination of the geometric capacitance C_i of the LAO film in parallel with the capacitance C_s of the STO substrate and the quantum capacitance C_q of 2DEG at the LAO/STO interface:

$$1/C = 1/(C_i + C_s) + 1/C_q. \quad (2)$$

For the initial LCS, the equivalent circuit of the LAO/STO heterostructures is simply modeled as a combination of capacitors in series, as shown in Figure 5b.

For the HCS, after applying a sufficient positive DC gate voltage to the capacitor device, a great number of positively charged oxygen vacancies trapped at the LAO surface migrate to the inside of the LAO thin film, as shown in Figure 5c. Accordingly, the capacitance in the LAO film could be expressed as the parallel combination of geometric capacitance C_i and capacitance C_m of mobile oxygen vacancies in the LAO film. The quantum capacitance is annihilated after the application of a positive gate voltage, as shown in Figures 1a and b. As the gate voltage is swept from negative voltage to positive voltage (-15 to $+15$ V), there is a peak related to quantum capacitance on the shoulder of the LCS branch because of the strong electronic correlation of 2DEG at the LAO/STO interface. However, when the gate voltage is swept from positive voltage to negative voltage ($+15$ to -15 V), the peak disappears from the shoulder of the HCS branch. The annihilation of quantum capacitance after applying a gate voltage of $+15$ V can be attributed to a Coulomb interaction between the positive oxygen vacancies in the LAO layer and the electrons at the LAO/STO interface; the interaction of the oxygen vacancy–electron pairs could suppress the strong electronic correlation of 2DEG at the LAO/STO interface. When a sufficient negative voltage is applied, the oxygen vacancies distributed throughout the LAO thickness would be driven back to the LAO surface. As the distance between oxygen vacancies at the LAO surface and electrons at the LAO/STO interface increases, the Coulomb interaction is reduced drastically or even disappears. The strong electronic correlation of 2DEG at the interface would recover to the initial state, and the peak on the shoulder of the LCS branch would appear again. Therefore, for the HCS, the measured capacitance at low frequency is given by:

$$C = C_i + C_m + C_s \quad (3)$$

The equivalent circuit of the capacitor devices on LAO/STO heterostructures is shown in Figure 5d. For the HCS, the oxygen vacancies redistributed throughout the LAO film have sufficient time to respond at low frequency, resulting in a colossal increase in capacitance. With increasing frequency, the mobile oxygen vacancies do not have sufficient time to respond to the high frequency, and the capacitance in the HCS decreases accordingly, as shown in Figure 3b. The capacitance enhancement increases with the amplitude or duration of the positive gate voltage because more oxygen vacancies would be driven into the inside of the LAO film. The electrically induced colossal capacitance enhancement in the LAO/STO heterostructure achieved by controlling the migration of oxygen vacancies in the LAO film under the gate voltage reveals a new approach for enhancing the capacitance of MOS structures, which allows the production of lower-power devices and represents a step forward in the development of high-k dielectrics.[15]

In summary, we have demonstrated reversible capacitance switching in LAO/STO-based capacitor devices after applying voltage pulses with opposite polarities, which we attribute to the redistribution of mobile oxygen vacancies through the thickness of the LAO layer. The colossal capacitance enhancement, up to approximately 1000% at low frequency, would be highly significant to the further development of currently fashioned transistors. The ability to reversibly switch the capacitance states of electron gas-based memory devices provides new ground for information storage and processing. The technological

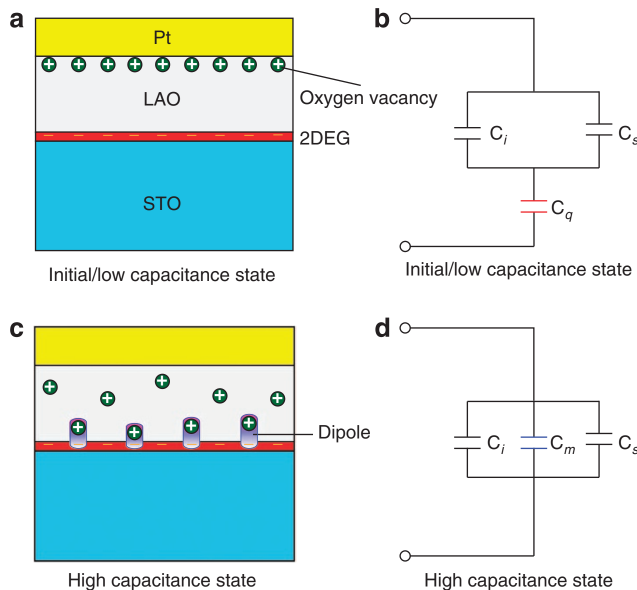

Figure 5 Mechanism of the colossal capacitance enhancement. (**a**) For pristine capacitor devices, it is reasonable to assume that the oxygen vacancies are trapped at the $LaAlO_3$ (LAO) surface. (**b**) For the ICS and LCS, the total measured capacitance could be modeled as the in-series combination of the geometric capacitance C_i of the LAO film in parallel with the capacitance C_s of the TiO_2-terminated $SrTiO_3$ (STO) substrate and quantum capacitance C_q of two-dimensional electron gas (2DEG) at the LAO/STO interface. (**c**) After the application of a sufficient positive DC gate voltage to the capacitor device, positively charged oxygen vacancies are distributed throughout the LAO film. These positively charged oxygen vacancies are responsible for the colossal capacitance enhancement. Coulomb interactions of oxygen vacancy-electron dipoles suppress the strong electronic correlation of 2DEG at the LAO/STO interface, leading to the annihilation of quantum capacitance. (**d**) For the circuit diagram of the HCS, the total capacitance could be modeled as the parallel combination C_i, C_s and C_m from mobile oxygen vacancies throughout the LAO film.

impact of new materials systems with functional properties of relevance to semiconductor devices relies on their successful integration with silicon. Recently, Park *et al.*[34] reported the integration of the LAO/STO interface on silicon, which opens the possibility of the integration with Si for the application of the capacitor devices based on the LAO/STO heterostructures. The interface-based capacitor devices will further pave the way toward the development of novel integrated oxide devices.

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