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ORIGINAL ARTICLE

Organic nonvolatile memory transistors with self-doped polymer energy well structures

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Developing organic nonvolatile memory devices with a writing/reading/erasing logic function in actual array structures is extremely important for realizing low-cost lightweight/flexible plastic electronic systems. Here, we demonstrate that organic field-effect transistors (OFETs) with a polymer energy well structure (PEW-OFET) exhibit excellent nonvolatile memory performances. The PEW structure is created by sandwiching a self-doped poly(*o*-anthranilic acid) (SD-PARA) nanolayer (high dielectric constant, $k = 14$) between two low-dielectric polymer layers ($k = 2$–4). The primary idea behind this concept is the rapid storage and retrieval of charge carriers in the PEW layer during operation due to the high *k* feature of the SD-PARA nanolayer, which aids the rapid transport of charge carriers inside, whereas the stored charges are safely trapped due to the two low *k* layers. The results indicate that the PEW-OFET memory devices exhibit outstanding retention characteristics upon continuous reading up to 2000 s after writing, whereas their excellent writing/reading/erasing/reading cyclability is demonstrated in a test with >3000 cycles. Therefore, the present simple yet cost-effective PEW-OFET concept is expected to significantly contribute to the development of low-cost plastic memory array devices because all processes can be inexpensively performed at low temperatures and additional logic transistors are unnecessary.
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Keywords: energy well; organic nonvolatile memory; self-doped poly(*o*-anthranilic acid); silver electrode; transistor

INTRODUCTION

Recently, organic memory devices have been extensively studied because of their potential in the low-temperature (low-cost) fabrication of flexible and lightweight plastic memory modules compared with conventional inorganic memory devices that intrinsically lack flexibility and should be processed at higher temperatures.[1–4] Among the various types of organic memory devices, a considerable number of studies have been devoted to nonvolatile memory systems that include organic-resistive-switching diode memory and organic field-effect transistor (OFET) memory.[5–17] The organic-resistive-switching diode memory devices consist of organic-resistive layers between two electrodes, which typically act as either electrically insulating components or electrically conducting components under appropriate voltage conditions.[5–10] However, the organic-resistive-switching diode memory devices require transistors for addressing signals in two-dimensional memory arrays because they do not possess third electrodes for signal addressing. In contrast, OFET memory devices can essentially perform the signal addressing function alone because there are three electrodes in the unit transistors.[11–17]

The OFET memory devices can be classified into two types based on the memory effects. The first type is a ferroelectric OFET memory device and the second is a charge-storage OFET memory device. The functionality of the ferroelectric OFET memory devices arises from the ferroelectric gate insulating layers that are polarized under appropriate electric fields (gate voltages); therefore, the research objective is to maintain the polarized state under continuous (repetitive) reading operations.[11–13] In the case of charge-storage OFET memory devices, the gate insulating layers with polar groups have a charging role for controlling the gate voltage.[14–17] To improve the switching performance, further insulating layers have been inserted between the gate insulating layer and the channel layer (organic semiconductors).[18] However, this double insulating layer approach has a disadvantage in that the difference in the dielectric constants between the two layers is realistically limited due to the lack of highly polar (high-*k*) polymer materials.

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Therefore, we designed new charge-storage OFET memory devices with a partially charged polymer interlayer (with permanent charges) between the gate insulating layer and the channel layer, which has considerably higher polarizability (than typical polar polymers without ionic charges) such that it can store more charge carriers generated by the field-effect phenomena. In addition, these new OFET memory devices have a 'polymer energy well (PEW)' structure that is formed by the partially charged interlayer in which the energy band levels (lowest unoccupied molecular orbital (LUMO) and highest occupied molecular orbital (HOMO)) are significantly different from those of the adjacent polymer layers (the gate insulating layer and the channel layer). Therefore, in principle, the charge carriers, which are generated during field-effect operation in the present OFET with a PEW structure (PEW-OFET), are expected to be safely stored in the PEW because the large energy walls (high energy barriers) around the energy well can prevent the charges from escaping.

In this study, we used a self-doped polyaniline derivative (self-doped poly(*o*-anthranilic acid; SD-PARA))[19,20] as a partially charged interlayer because the SD polymer is resistant to any possible deterioration of the device performances by the migration of guest dopant molecules that are doped into polymers when external guest dopants are used (note that polar dopant molecules can be mobile under high electric fields for writing operation). For fabricating the PEW-OFET devices, we specifically attempted to use relatively cheap silver (Ag) source and drain electrodes rather than the expensive gold electrodes that have typically been used in previous reports[18] because the use of gold electrodes is one of the primary hurdles for the commercialization of organic memory devices.

MATERIALS AND METHODS

Materials

The SD-PARA polymer was synthesized as reported in our previous study.[19,20] The intrinsic viscosity (η) of the SD-PARA polymer product was determined to be 0.11 dl g^{-1} in *N*-methyl-2-pyrrolidinone at 25.0 °C using an Ubbelohde capillary viscometer (Fungilab, Sant Felin de Vogregat, Barcelona, Spain). Poly(3-hexylthiophene; P3HT; $\overline{M_w}$(weight-average molecular weight) = 6.0 × 10^4; polydispersity index = 2.0; regioregularity = 95%) was supplied from Lumtec (Science-Based Industrial Park, Hsin-Chu, Taiwan), whereas poly(vinyl phenol; PVP, $\overline{M_w} = 2.5 \times 10^4$) and methylated poly(melamine-co-formaldehyde; MMF, $\overline{M_w} = 432$) were purchased from the Sigma-Aldrich Co. (St Louis, MO, USA). The PVP and MMF materials were used without further purification.

Methods

The indium tin oxide (ITO)-glass substrates were patterned to have a 1 × 12 mm stripe for a gate electrode using photolithography techniques, which was followed by wet (acetone and isopropyl alcohol) and dry (ultraviolet ozone) cleaning processes. The PVP-MMF (PVP + MMF) precursor films were spin coated on top of the cleaned ITO-glass substrates and subjected to a thermal curing process at 250 °C for 60 min to create the corresponding insoluble PVP-MMF films (thickness (t) = 600 nm) for a gate insulating layer. Then, the SD-PARA layer (t = 100 nm) was spin coated onto the PVP-MMF layer. After soft baking the samples coated with the SD-PARA layer at 50 °C, the P3HT channel layer (t = 50 nm) was spin coated followed by soft baking at 50 °C. Finally, Ag source and drain electrodes were deposited through a shadow mask, which defines the channel length of 70 μm and the channel width of 3 mm in the PEW-OFET devices (see Figure 1a). All of the devices were stored in a nitrogen-filled glove box before the measurements. For the conductivity measurement of the SD-PARA film in the out-of-plane direction (normal to the film plane), the SD-PARA film was spin coated onto ITO-glass substrates. Then, metal (aluminum (Al)) electrodes were deposited on top of the SD-PARA layer under vacuum followed by soft baking at 50 °C, which led to the diode-type configuration devices (ITO/SD-PARA/Al). All the film samples for the measurement of dielectric constants were spin coated on ITO-glass substrates. The P3HT and SD-PARA films were soft baked at 50 °C after spin-coating, whereas the PVP-MMF film was thermally cured at 250 °C for 60 min. The film samples were then transferred to a nitrogen-filled glove box and metal (Al) electrodes were deposited under vacuum. One set of diode devices (ITO/P3HT/Al and ITO/SD-PARA/Al) was thermally annealed at 120 °C for 30 min before the dielectric constant (impedance) measurement.

Characterization

The optical absorption spectra of the SD-PARA film, the P3HT film and the P3HT-coated SD-PARA film were measured using a ultraviolet–visible absorption spectrophotometer (Optizen 2120UV, Mecasys, Daejeon, Republic of Korea). The ionization potential of the SD-PARA film coated on the ITO-glass substrate was measured using a photoelectron yield spectrometer (AC-2, Riken-Keiki, Tokyo, Japan; see the Supplementary information S1). The *J*–*V* curves of the diode device (ITO/SD-PARA/Al) were measured using an electrometer (Keythley 2400, Keithley Instruments Inc., Cleveland, OH, USA), while an impedance analyzer (VERSA STAT 4, Ametek, Berwyn, PA, USA) was used to measure the dielectric constants of the film samples (the frequency sweep was performed from 10 Hz to 1 MHz). The transistor and memory characteristics of the OFET devices were measured using a semiconductor parameter analyzer (SCS-4200, Keithley). All of the device measurements were performed in a nitrogen atmosphere because a nitrogen-filled sample holder was used.

RESULTS AND DISCUSSION

As shown in Figure 1a, the SD-PARA interlayer (thickness = 100 nm) was coated on top of the gate insulating layer (PVP-MMF), and then the channel layer P3HT was coated before the deposition of the Ag source and drain electrodes through a shadow mask. The SD-PARA film presented its major absorption edge at ~670 nm in the presence of weak absorption at the near-infrared regions (900–1000 nm), which may correspond to the self-doped regions in the SD-PARA chains (Figure 1b). This weak absorption in the near-infrared region was also observed after coating the P3HT layer. The ionization potential (or HOMO energy) of the SD-PARA film was measured using photoelectron yield spectroscopy. The measured onset value was ~5.4 eV, which corresponds to ~5.7 eV after calibration.[21–23] To measure the conductivity of the SD-PARA film in the out-of-plane direction, we fabricated a diode device in which the SD-PARA film was sandwiched between the bottom and top electrodes (see details in the experimental section). The current density–voltage (*J*–*V*) curves revealed that the SD-PARA film is not a perfect conductor but a semiconductor because of its diode-like shape and the asymmetric current density trend between the forward and reverse biases (see the inset in Figure 1c).

Based on the optical and electrical measurements of the SD-PARA film, we confirmed that the SD-PARA film is a semiconductor film in which the HOMO and LUMO energy levels are 5.7 and 3.9 eV, respectively (we note that a weak inter-band energy level (~4.4 eV) exists due to the doped regions (900–1000 nm) in the SD-PARA film). Using this information, we can construct the energy band diagram of the present devices in consideration of the applied electric field between the source and gate electrodes. The OFET without the SD-PARA layer has only one interface between the PVP-MMF layer and the P3HT layer (see the energy band diagram in Supplementary Figure S1). Therefore, no sufficient charge storage is expected for this device structure because the dielectric constant difference between these two layers (k = 2.0 for P3HT versus k = 4.1 for PVP-MMF) is unable to store sufficient charges for memory operation. In contrast, as shown in Figure 2, the OFET with the SD-PARA layer

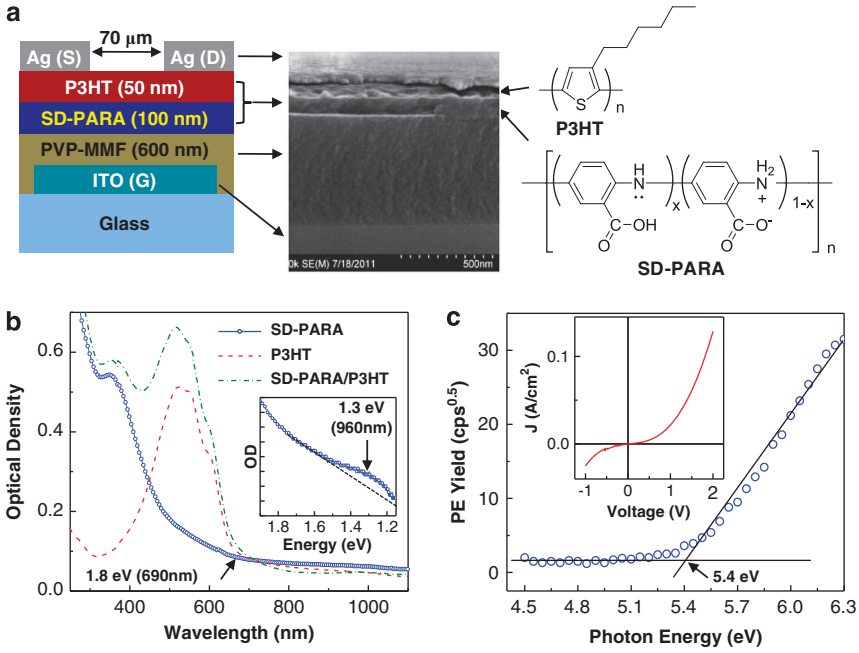

Figure 1 (**a**) Schematic illustration of the OFET with the SD-PARA layer (PEW-OFET; left), the cross-sectional FESEM image (middle) and the chemical structures of P3HT and SD-PARA (right). (**b**) Optical absorption spectra of the SD-PARA film, the P3HT film and the P3HT-coated SD-PARA film (inset shows the enlarged spectrum of the SD-PARA film for better visualization of the partially doped state). (**c**) Photoelectron yield spectrometer spectrum of the SD-PARA film coated on the ITO-glass substrate (inset shows the $J-V$ curve of the SD-PARA layer in a diode configuration (ITO/SD-PARA/Al)).

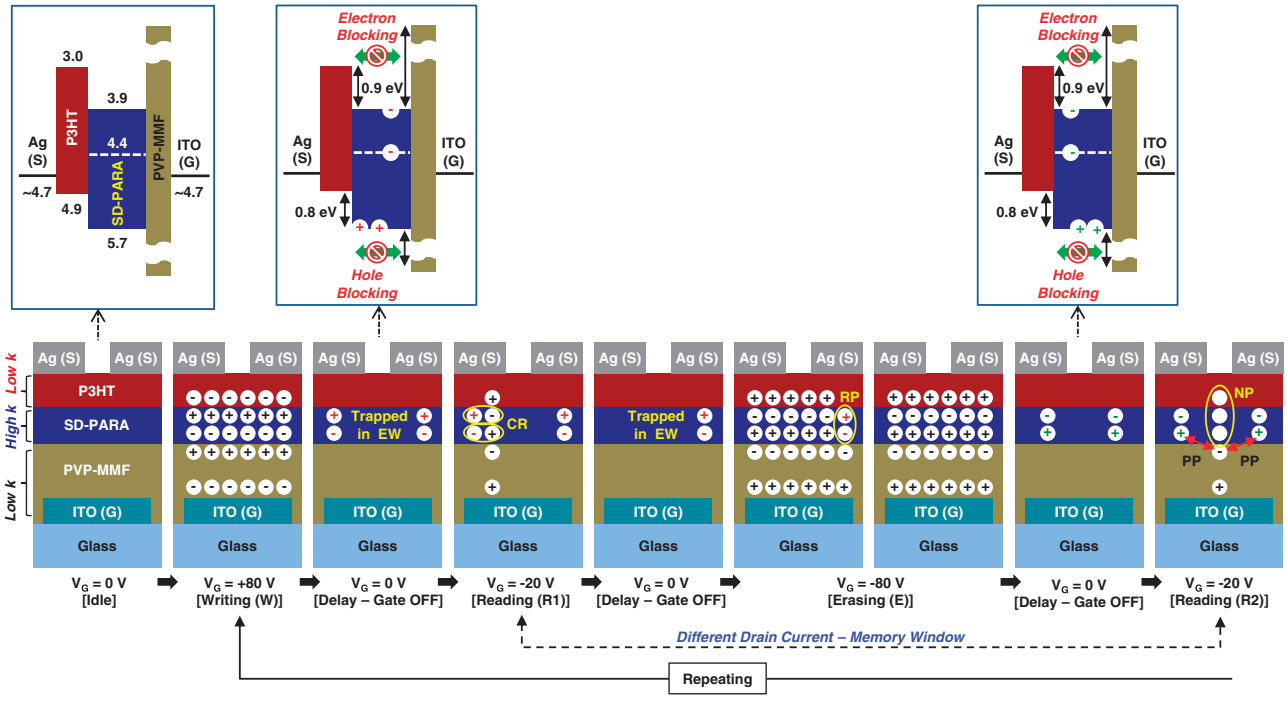

Figure 2 Illustration for the operation mechanism of PEW-OFET: 'EW', 'CR', 'RP', 'PP' and 'NP' denote 'energy well', 'charge recombination loss', 'strong reverse polarization', 'preventing polarization due to the existing positive charges' and 'no polarization and no charge generation', respectively. The status of the charges (electrons and holes) is displayed in the corresponding energy band diagrams. Note that the drain current at the R1 stage will be less than that at the R2 stage, which leads to a memory window.

(PEW-OFET) has two distinctive hetero-interfaces between the P3HT layer and the SD-PARA layer ($k = 2.0$ for P3HT versus $k = 14$ for SD-PARA) and between the SD-PARA layer and the PVP-MMF layer ($k = 14$ for SD-PARA versus $k = 4.1$ for PVP-MMF; see the details of dielectric constant measurements in the experimental section and the impedance–frequency plot of the SD-PARA layer in Supplementary Figure S2). Considering the large LUMO band energy offset (0.9 eV) between the P3HT layer and the SD-PARA layer, as well as the large band gap of the PVP-MMF layer (see the energy band diagram in Figure 2, top), the PEW-OFET has a charge (electrons and

holes)-trapping energy well structure such that the trapped charges (electrons/holes generated by the field-effect modulation, see Figure 2) in the SD-PARA layer can be effectively confined in the SD-PARA layer. In other words, the large energy barrier for charges (0.9 eV for electrons and 0.8 eV for holes) blocks the charge transfer from the LUMO (HOMO for holes) level of the SD-PARA layer to the LUMO (HOMO for holes) level of the P3HT layer in the presence of slight charge loss by Coulombic recombination between electrons and holes in the SD-PARA layer. In addition to the charge-trapping energy well mechanism, however, we note that the space charge polarization effect might contribute to the charging phenomenon because the SD-PARA layer has a high k value due to the partially self-doped sites. Note that the two low k layers (P3HT and PVP-MMF) have an important role in safely maintaining the trapped charges in the energy well without significant diffusion loss through a possible leakage path in consideration of the low/high/low-dielectric structure.

The detailed operation mechanism for the present PEW-OFET is depicted using the cross-sectional device structures (see Figure 2 (bottom)). Upon writing at the gate voltage (V_G) of $+80$ V, a strong polarization occurs leading to the generation of holes and electrons in the SD-PARA layer and electrons in the P3HT layer. After removing the gate voltage, the electrons in the P3HT layer disappear through rapid electron transfer toward the metal (Ag) electrodes (see also Supplementary Figure S1). However, the charges in the SD-PARA layer are confined due to the large energy barrier, as explained above, from the charge-trapping PEW structure. Turning on the gate voltage ($V_G = -20$ V) to read the drain current (R1) induces a weak polarization effect that is the reverse of the writing operation, which results in the loss of some trapped (confined) charges in the SD-PARA layer through charge recombination. Applying $V_G = -80$ V for erasing operation, a strong polarization removes the remainder of the trapped charges in the SD-PARA layer. Then, the charges are trapped again in the SD-PARA layer, but the arrangement (direction) of charges is reversed from the writing case. At this stage, upon applying the gate voltage ($V_G = -20$ V) for the reading operation (R2), the holes are rarely generated in the P3HT layer because the trapped holes (that is, an empty state of electrons) cannot allow sufficient polarization in the SD-PARA layer. Therefore, the R2 current is significantly less than the R1 current, which creates a memory window.

As expected from the conceptual mechanism (Figure 2), the OFET without the SD-PARA layer exhibited almost no noticeable hysteresis between the forward (gate voltage (V_G): from $+50$ to -80 V; drain voltage (V_D): from 0 to -80 V) and backward (V_G: from -80 to $+50$ V; V_D: from -80 to 0 V) direction sweeps in the output and transfer curves (Figures 3a and b). The very small hysteresis in the output curves in Figure 3a can be attributed to the influence of polar groups ($-$OH) that remained without reacting during the course of

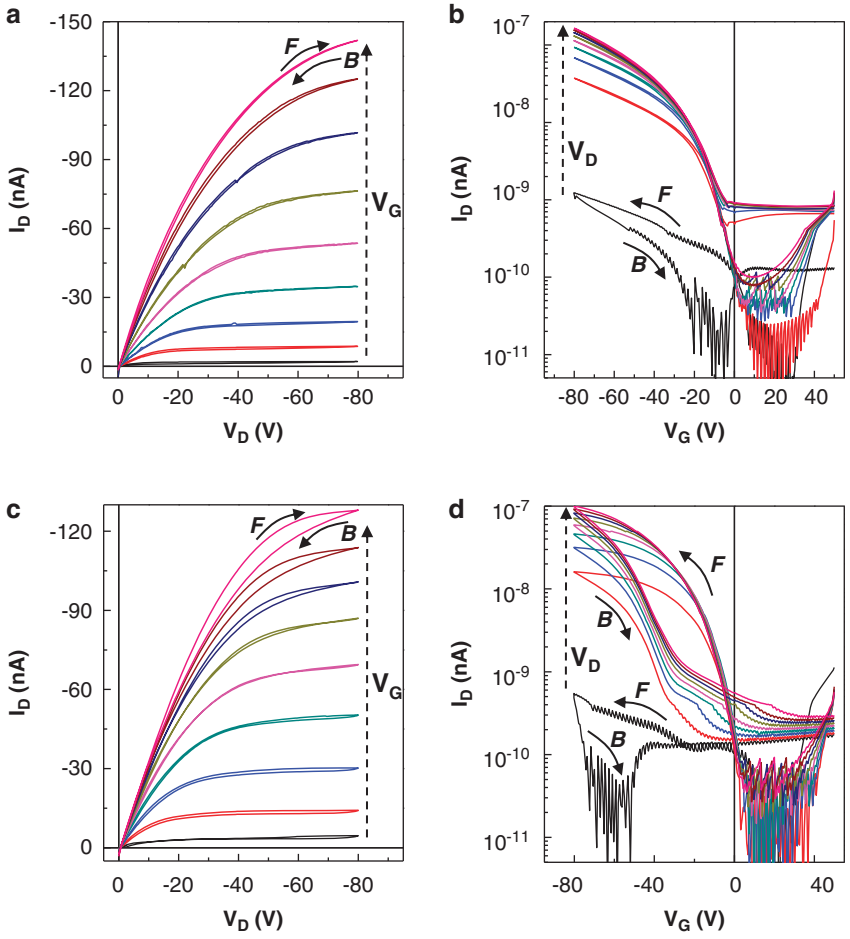

Figure 3 Output (left) and transfer (right) curves of the OFETs upon sweeping in the forward (F) and backward (B) directions: (**a**, **b**) OFET without the SD-PARA layer, (**c**, **d**) PEW-OFET. Note the V_G increase from 0 to -80 V in the arrow direction for (**a**) and (**c**) and the V_D increase from 0 to -80 V in the arrow direction for (**b**) and (**d**).

the thermal curing process (see Supplementary Figure S3). However, a relatively pronounced hysteresis was observed for the PEW-OFET (Figures 3c and d). This hysteresis phenomenon was observed in all the output and transfer curves without respect to the voltages in the presence of the varied hysteresis gap differences depending on the voltages, which implies that the present charge-trapping PEW structure works in a wide range of voltages. Here, we note that the difference in the degree of hysteresis between the output curves (Figure 3c) and transfer curves (Figure 3d) can be attributed to the charging characteristics of the present devices, which are primarily dependent on the gate voltage (between the gate and source electrodes) action across the SD-PARA layer (the SD-PARA layer does rarely affect the output curves because the current flow is primarily through the P3HT layer upon applying the drain voltages). The hole mobility of the devices in the forward and backward directions was calculated from the relationship ($I^{0.5} \sim V_G$; see Supplementary Figure. S4).[22,24,25] The hole mobility of the OFET without the SD-PARA layer was almost similar for both the forward and backward direction sweeps, whereas the PEW-OFET exhibited an almost one order of magnitude lower hole mobility for the backward direction sweep than for the forward direction sweep (see Supplementary Figure S5). This large change in the hole mobility for the PEW-OFET reflects the different charged states in the SD-PARA layer upon sweeping the gate voltages in the forward and backward directions. Here, we note that the slightly high operation voltage can be easily reduced by using a sophisticated lithography technique that can deliver narrow channel lengths; as we know very well, for example, the operation voltage can decrease to <3 V if the channel length approaches 2 μm. Further reduction of the operating voltage can also be possible by optimizing the OFET layers using a better gate insulating layer, as shown in Supplementary Figure S6, and higher regioregularity P3HT, as reported in our previous work.[26] The characteristics of the devices are summarized in Supplementary Table S1. The memory window of the PEW-OFET was 30–33 V, which is noticeably greater than the 1–2 V for the OFET without the SD-PARA layer.

To examine the memory characteristics of the present PEW-OFET, we applied the following gate voltage program: writing ($V_G = +80$ V), reading ($V_G = -20$ V) and erasing ($V_G = -80$ V; see details in the caption of Figure 4a). As shown in Figure 4a, the drain current (I_D) was regularly read five times at $V_G = -20$ V (see 'R' part) after writing (see 'W' part), though the reading action was performed every 10 s (holding at $V_G = 0$ V). This result indicates that the present device did indeed function as a basic nonvolatile memory device. After erasing at $V_G = -80$ V, the baseline of the drain current was clearly reduced close to almost 'zero' at $V_G = 0$ V. In particular, the drain current during the reading operation at $V_G = -20$ V after erasing was certainly lower than the baseline (I_D = ca. −5 nA) of the drain

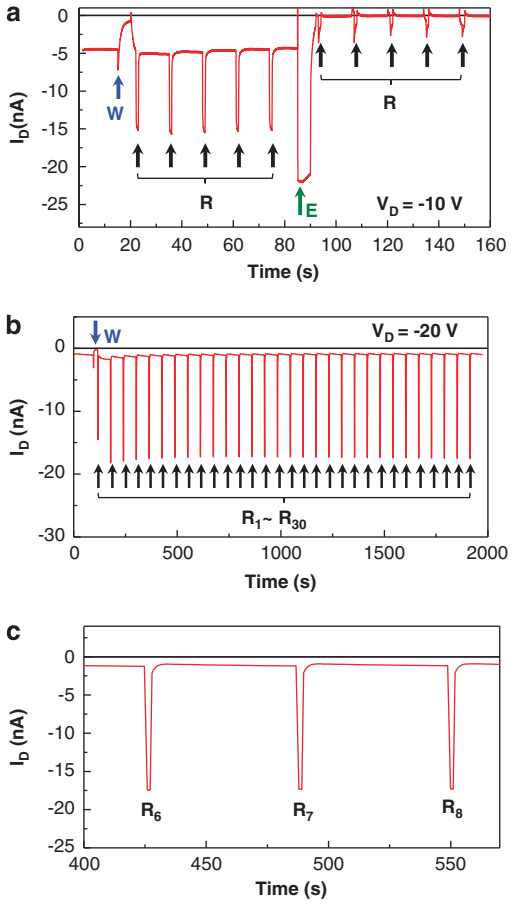

Figure 4 (**a**) Writing–reading–erasing memory operations for PEW-OFET: operation program (V_G) is (writing: +80 V for 5 s) → (waiting: +0 V for 2 s) → repeating five times ((reading: −20 V for 1 s) → (waiting: +0 V for 10 s)) → (erasing: −80 V for 5 s) → (waiting: +0 V for 2 s) → repeating five times ((reading: −20 V for 2 s) → (waiting: +0 V for 10 s)). (**b**) Stability (retention) test: operation program (V_G) is (writing: +80 V for 20 s) → repeating 35 times ((reading: −20 V for 2 s) → (waiting: +0 V for 60 s)). (**c**) Enlarged peaks for the R_6–R_8 reading events in (**b**).

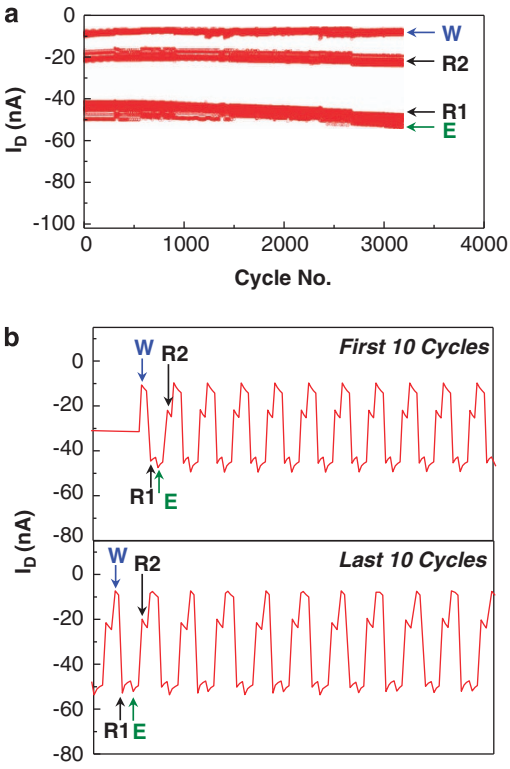

Figure 5 Over 3000 cycle writing(W)–reading(R1)–erasing(E)–reading(R2) test results for PEW-OFET: (**a**) drain current for each operation (W, R1, E, R2) as a function of cycle number, (**b**) drain current changes in the first (top) and last (bottom) 10 cycles. Operation program (V_G): repeating ((W: +80 V for 2 s) → (R1: −20 V for 2 s) → (E: −80 V for 2 s) → (R2: −20 V for 2 s)).

current before erasing, which supports clear writing–reading–erasing loop functions of the present device. Next, we attempted to investigate the stability (retention) characteristics of the present device by programming the reading gap to be 60 s after writing. As shown in Figure 4b, the drain current was almost regularly read for a 30-time repetition, although the drain voltage was set to be two times greater ($V_D = -20$ V) than the drain voltage in Figure 4a to make the reading condition harsher. The enlarged regions for the sixth to eighth reading operations are presented in Figure 4c, which represents extremely high data (retention) stability characteristics. To test the long-term retention characteristics, we attempted to perform >3000 cycles with the writing–reading–erasing–reading program. As shown in Figure 5a, the drain current was encouragingly well-maintained with a standard deviation of 6% (R1 after writing) and 3.8% (R2 after erasing). In particular, the shape of the drain current action spectra (I_D versus cycle number) was excellently maintained when we investigated the spectra for each cycle, although the drain current intensity was marginally changed under the given standard deviation when compared between the first and last 10 cycles (see Figure 5b). Finally, to obtain insight on the charge-trapping PEW effect in the present memory device structure even though the basic requirement for energy well construction is acceptable from the energy level difference (see Figure 2), we briefly examined the energy well effect by varying the thickness of the SD-PARA layer (see Supplementary Figures S7–9 and Supplementary Table S2). The result indicated that a particular charge confinement effect was indeed present for all the examined SD-PARA thicknesses and that the lowest threshold voltage was measured at 50 nm among three different thicknesses.

CONCLUSIONS

In summary, we have fabricated PEW-OFET devices with a SD-PARA semiconducting nanolayer, P3HT channel layer and PVP-MMF gate insulating layer. This arrangement of polymeric layers created a charge-trapping PEW structure that can efficiently store charges (electrons/holes) generated by the field-effect action. The PEW-OFET did indeed exhibit a pronounced hysteresis behavior, although almost no hysteresis was measured for the OFET without the SD-PARA layer. In addition, the hole mobility of the PEW-OFET device was noticeably (~10-fold) changed according to the charging–discharging operation (forward–backward sweep of gate voltages). The PEW-OFET device exhibited clear writing–reading–erasing functions and outstanding stability (data retention) upon long-term operations up to ca. 2000 s, which was supported by the writing–reading–erasing–reading test with >3000 cycles. Therefore, we believe that the present PEW-OFET memory is a simple yet powerful approach for realizing organic memory devices in the near future.

CONFLICT OF INTEREST

The authors declare no conflict of interest.

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