# Device engineering for silicon photonics

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Silicon photonics has attracted increasing attention and research effort in recent years because of its potential for low-cost integration using existing complementary metal–oxide–semiconductor technology. One motivation for research on silicon photonics has been its potential application in energy-efficient high-speed optical interconnects for computing systems, particularly in circumstances where large power dissipation from electrical interconnects will limit performance. The high-density integration of photonic devices, the wide availability of fabrication facilities and the potential for monolithic integration with electronic circuits offer the prospect for future low-cost, reliable and energy-efficient silicon photonic devices suitable for applications in computing, communications and sensing. Herein we review recent progress in the engineering of new devices and functional elements in silicon photonics, including low-loss waveguides, passive integrated devices, integrated lasers, modulators, photodetectors and fiber–chip coupling techniques. We also identify some emerging opportunities with potential for future development, such as mid-infrared silicon photonics and optomechanical devices, and summarize some current trends, including the development of photonic devices based on amorphous silicon and the use of foundries for silicon-photonic device fabrication.

After an impressive initial spurt of progress in device engineering during the early 2000s when the optical communications industry saw unprecedented levels of investment, silicon photonics continues to develop at an amazing pace. Many novel applications and devices are emerging. Silicon photonics has the potential to become a major platform for optoelectronic integrated circuits (OEICs) and to be used in high-speed optical interconnects for chip-level data communications because of the extremely large bandwidth and high speed offered by optical communications. Many challenges have been addressed through the introduction of innovative ideas, paving the way for the practical deployment of silicon-based optoelectronic devices and integrated photonic circuits in computing and telecommunication systems [1]. The commercialization of silicon photonics, originally driven by applications in telecommunications, is now also driven by the needs of the computing industry for high-speed, energy-efficient optical cable technology, such as the Light Peak Technology under development by Intel (USA). The California-based company Luxtera (USA) has also commercialized a series of silicon-photonic transceiver systems.

Silicon offers many advantages over alternative material systems (*e.g.* InP, GaAs, LiNbO$_3$) for OEIC applications. One major reason for the wide interest that silicon photonics is attracting is the cost advantage that silicon photonics can potentially offer through its compatibility with the complementary metal–oxide–semiconductor (CMOS) fabrication processes used in the microelectronics industry. The huge investments that have been made in CMOS microelectronics fabrication technologies has resulted in processes that offer much higher yield than is possible using alternative materials for photonics, thus making feasible large-scale integration and the production of silicon-photonic devices that are monolithically integrated with not only optical components but also electronic circuits in the same platform at ultrahigh density. Another reason for the attractiveness of silicon photonics is the high refractive index contrast between the silicon core (refractive index, 3.48) and silicon dioxide cladding (refractive index, 1.45) in
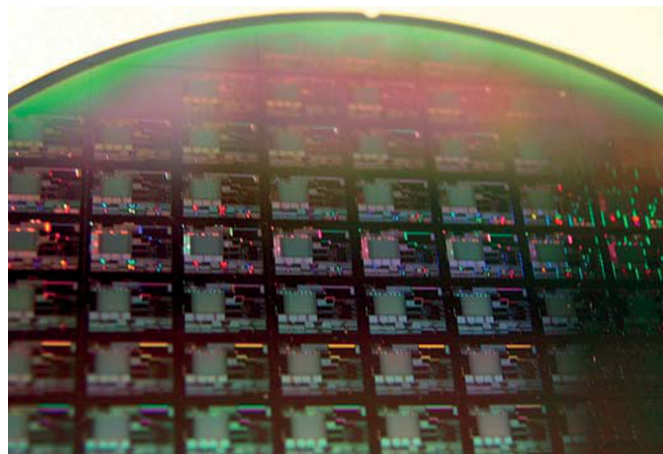

Figure 1. Integrated photonics devices fabricated on a 6-inch silicon-on-insulator (SOI) wafer using the CMOS fabrication facility at IMEC (Belgium).

silicon-on-insulator (SOI) devices, which ensures the submicrometer confinement of light and allows tight bending in optical waveguides. The high-density integration of photonic circuits on SOI platforms is thus feasible. The low cost of high-quality SOI wafers is another advantage of silicon photonics. All kinds of low-cost devices enabled by silicon photonics are therefore predicted, and these may also enjoy the other benefits of monolithic integration: smaller size, increased power efficiency and improved reliability. Figure 1 shows an example of a high-density integrated photonics devices fabricated on a 6-inch SOI wafer using CMOS-compatible technology.

In this article, we review some of the exciting progress that has been made in silicon photonics with the aim of providing a broad and balanced overview of the recent advances in device engineering.

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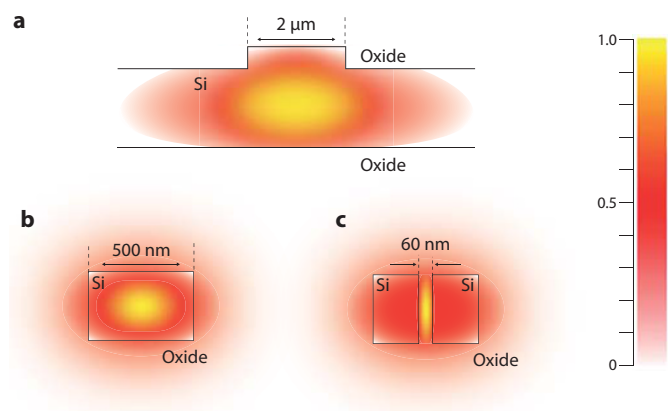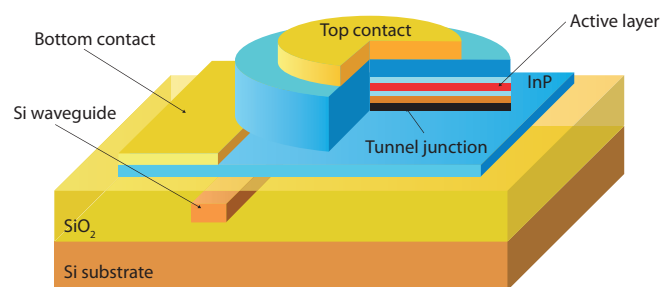
Figure 2. Schematic cross-sections for a (a) ridge waveguide, (b) photonic-wire waveguide and (c) slot waveguide on SOI wafer. The calculated fundamental optical modes (transverse electric) of the waveguides are shown.

Figure 3. Schematic illustration of an integrated microdisk laser structure on SOI showing the disk cavity, SOI wire waveguide, bottom contact layer, tunnel junction and metal contacts. Adapted from Ref. 24 (© 2007 OSA).

We shall concentrate on developments toward various passive silicon waveguide components, integrated lasers, high-speed modulators, photodetectors and fiber–chip coupling techniques. The emphasis will be on device engineering rather than general theory and detailed applications. Some emerging opportunities for future development of silicon photonics are also mentioned, such as mid-infrared silicon photonics, optomechanical devices and amorphous-silicon devices. There is also a trend toward the fabrication of silicon-photonic devices through external foundries. Many interesting review articles on different fields of silicon photonics have been published recently and we would like to refer the readers to the reviews by Reed *et al.* [2] on silicon optical modulators; the review by Liang *et al.* [3] on lasers and other recent reviews on germanium-based integrated photodetectors and silicon optical nonlinear effects [4,5].

Passive waveguide devices

Extremely low propagation loss (approaching 0.1 dB cm⁻¹) in SOI waveguides can be achieved with ridge waveguides (Figure 2(a)), where waveguide dimensions of several micrometers are used. The fundamental optical mode is confined by the shallow-etched slab on both sides. Low loss is ensured by the low field intensity at the sidewalls of the waveguide. As there is virtually no absorption loss in silicon, the propagation loss in straight waveguides is dominated by scattering loss caused by the sidewall roughness, which is dependent on the lithography and dry-etching processes. One successful example of the application of such silicon waveguides with large cross-sectional area is the multichannel variable optical attenuator produced by Kotura (USA). However, micrometer-sized waveguides typically require a large bending radius of the order of a few millimeters and are thus unsuitable for applications in highly miniaturized devices or high-density integration.

Photonic-wire waveguides (Figure 2(b)), with a cross-sectional area of about 0.1 μm² have become widely used in recent years for integrated photonic devices. Tight light confinement up to the diffraction limit is achieved through the introduction of two deep-etched trenches that cut down to the buried oxide of the SOI wafer. The bending radius can be reduced to a few micrometers with negligible loss for such miniaturized waveguides. Therefore, highly compact photonic devices can be realized using such photonic-wire waveguides. One example is an on-chip optical delay line achieving >500 ps delay with a device footprint of smaller than 0.09 mm² [6]. A drawback of such tight light confinement is the increased sensitivity to sidewall roughness; much larger scattering loss is typically observed in such devices. Around 2 dB cm⁻¹ loss was reported for a device prepared using deep-ultraviolet photolithography and dry-etching processes [7]. More recently, <1 dB cm⁻¹ loss was reported for devices fabricated by electron-beam lithography and dry-etching [8].

Novel structures such as silicon slot waveguides (Figure 2(c)) have been introduced to guide light in narrow slots using low-refractive-index materials [9]. Such waveguides are particularly useful for sensing applications because of the large fraction of light in the slot, which is normally filled with air or liquid and which contains the particles or molecules to be detected. Another major application of slot waveguides is in high-speed nonlinear signal processing for communication systems. Record nonlinearity for a silicon waveguide was achieved recently by filling the slot with an organic material, which can offer much higher nonlinearity than silicon crystal [10]. Meanwhile, ultralow-loss waveguides fabricated using the local oxidation of silicon (LOCOS) technology have been used for realizing commercial silicon-based optoelectronic products [11].

Photonic crystal structures, based on hole or pillar structures of dimensions on the order of the optical wavelength, can guide or reject light according to photonic band theory. Photonic crystal has been widely explored for silicon-photonic devices because of its tight and intrinsic lossless light confinement and ease of fabrication [12]. Many novel functional components have been realized. Two outstanding examples are a slow-light device fabricated as a buffer for optical signals [12], and an experimentally demonstrated nanocavity with an ultrahigh quality (Q) factor of 600,000 [13]. Signal routing and wavelength multiplexing/demultiplexing are also important functions that are required for optical communication systems. Various optical wavelength-selective passive components based on silicon are discussed by Bogaerts *et al.* from Ghent University (Belgium) [14], including arrayed waveguide gratings (AWGs), Mach–Zehnder lattice filters and ring resonators. All of these passive devices can be fabricated using CMOS-compatible processes including deep-ultraviolet lithography. That group has demonstrated a compact AWG on an SOI platform with photonic wire waveguides with crosstalk of −20 dB and insertion loss of 2.2 dB for the center channels. An ultracompact four-channel SOI planar concave grating demultiplexer fabricated with CMOS-compatible technologies has been reported by the same group [15], achieving crosstalk better than 25 dB and a dramatically reduced on-chip loss of 1.9 dB. More recently, a compact 8×8 λ-router comprised of multimode-interference (MMI) couplers and microring resonators was demonstrated by Fan *et al.* [16] This device has an on/off contrast of 20 dB with about 4 dB loss per channel and less than 2 dB variation among channels.

Silicon integrated lasers

Integrated laser sources are some of the most basic elements in an optical communications link. Unlike the group-III/V materials, the indirect band gap of silicon prohibits efficient radiative recombination of carriers. A major milestone in the development of silicon photonics was reached with the demonstration of efficient silicon Raman

amplifiers [17,18] and a room-temperature continuous-wave (CW) Raman laser [19] that can be fully integrated with CMOS circuits. Raman scattering in silicon is much stronger than in silicon dioxide because of the well-defined crystal lattice of silicon. However, early attempts to achieve net gain by stimulated Raman scattering in a silicon waveguide were hindered by the absorption of free carriers generated by two-photon absorption (TPA) of the pump light [20]. Pulsed pumping was first used to achieve amplification and lasing by avoiding the accumulation of carriers, which would otherwise give rise to free carrier absorption (FCA). Continuous-wave amplification and lasing was found to be possible by applying an electric field across the silicon waveguide to reduce the carrier density [20]. Enhanced surface recombination in photonic wire waveguides and ion-implantation-induced defects in the waveguide have also been shown to reduce the carrier lifetime [21]. A group at Intel reported Raman lasing in a 25 V reverse-biased p–i–n silicon waveguide with a threshold of 20 mW in 2007 [22]. That waveguide displays a slope efficiency of 28% and an output power of 50 mW. Besides the advantage of being an all-silicon approach for realizing integrated lasers, the high spectral purity of Raman lasers is also of interest for spectroscopic applications, particularly in the mid-infrared spectral region.

The requirement of optical pumping for Raman lasers limits the application of this technology; electrically pumped integrated lasers on silicon are more desirable. Electrically pumped hybrid III/V-silicon lasers have been demonstrated [3], and so far they are the most advanced form of integrated laser on silicon. By employing wafer bonding of group-III/V materials on top of a patterned SOI wafer, a group from the University of California at Santa Barbara, USA, in collaboration with Intel have developed a hybrid AlGaInAs–Si evanescent laser with CW operation [23]. Light amplification in the laser cavity of this device is achieved by the direct-bandgap material bonded to the silicon. A highly compact realization (Figure 3) involving the bonding of InP-based microdisk lasers on top of silicon nanophotonic waveguides was reported by a group from Ghent University-IMEC [24]. After the first demonstration, more sophisticated designs of III/V–Si hybrid laser were demonstrated by the groups at UC Santa Barbara and at Ghent University, such as the cascaded microdisk lasers and the distributed feedback laser. Those designs have the potential to be grouped into a multiwavelength source for wavelength division multiplexing communication systems [3].

Research on CMOS-compatible, monolithically integrated and electrically pumped lasers on SOI platforms is an ongoing effort. Other approaches to making integrated lasers on silicon have also been explored, such as methods using rare-earth-ion-doped silicon and various types of silicon nanocrystals, although it is still challenging to achieve room-temperature CW lasing using these systems. Room-temperature luminescence was also observed recently using germanium-on-silicon waveguides [25]. A direct band transition in germanium-on-silicon was realized by bandgap engineering using tensile-strain and n-type doping. This is one of the most promising candidates for a CMOS-compatible electrically pumped integrated silicon laser.

High-speed optical modulators

High-speed modulators are one of the most important components in integrated photonics for optical communications. Conventional optical modulators typically employ crystalline materials that do not have inversion symmetry in the crystal structure. Optical modulators made from such materials rely on the change in refractive index induced by an applied electric field (*e.g.* via the Pockels effect). However the crystal structure of bulk silicon does have inversion symmetry and thus the electro-optical coefficients in silicon are zero unless the symmetry is broken (*e.g.* by application of strain). The refractive index change induced by the presence of free charge carriers, known as the plasma effect, has been generally used for making silicon optical modulators [2]. The plasma effect was systematically characterized

by Soref and Bennett in 1987 [26]. Both the refractive index and optical absorption are changed by free carriers. The first monolithic silicon high-speed modulators (>1 GHz) were demonstrated in 2004 by Intel [27]. These devices, with a Mach–Zehnder interferometer (MZI) structure, were based on the free carrier plasma effect in silicon and carrier accumulation in a metal–oxide–semiconductor structure. Optical modulation was achieved by propagating light in the region where the carrier concentration was changed by an applied electric field. Most recently (2009), carrier-accumulation-based modulators capable of a data rate of 10 Gb s^{-1} and with an extinction ratio of 9 dB were reported by Lightwire.

To reduce the device footprint and therefore lower power consumption, microresonator-based modulators have been studied. A high-speed silicon microring modulator operating at 1 GHz was demonstrated by Xu *et al.* in 2005 [28] based on a carrier injection scheme. The confinement of light power in a tiny resonating structure can enhance the sensitivity to refractive index change and dramatically reduce the device footprint. The drawbacks to such an approach are the limited modulation bandwidth and stringent requirements on the fabrication process. Performance comparable to that of carrier-accumulation-based modulators was achieved recently by the same group using an optimized design with a pre-emphasis driving signal [29]. Similar to the case for carrier-accumulation-based modulators, in which the speed is limited by the device resistance and capacitance, the speed of carrier-injection-based modulators is limited by the minority carrier lifetime [2].

Carrier-depletion-based MZI modulators have received mainstream attention for the development of modulators in recent years because of their higher intrinsic modulation speed. Silicon modulators operating at 40 Gb s^{-1} were reported by Liao *et al.* [30] in 2007. Microresonator-based modulators based on carrier depletion have also been developed in order to achieve high-speed modulation in a smaller device with lower power consumption. One recently result presented by Dong *et al.* [31] achieved energy consumption of 50 fJ b^{-1}, a 3 dB bandwidth of 11 GHz and 2 V peak-to-peak voltage. The fastest ring resonator carrier-depletion-based modulator reported to date operates with a small signal bandwidth of >35 GHz [32].

Although impressive results have been achieved recently in this field, to commercialize CMOS-compatible silicon high-speed optical modulators, further device engineering efforts will be needed in order to improve their performance in terms of other performance metrics such as loss, bandwidth, footprint and power consumption. The speed at which the concentration of electrical charge carriers can be modulated imposes an ultimate speed limit on silicon modulators through the free carrier effect, meaning that it will be difficult to design modulators substantially faster than the ~40 Gb s^{-1} reported to date [30,32]. The Franz–Keldysh and the quantum confined stark effects do not have this speed limitation and there is much interest in engineering silicon-based materials for high-speed optical modulators using these schemes with, for example, silicon–germanium superlattice structures [2].

Integrated silicon photodetectors

Silicon has a bandgap of about 1.12 eV. It is therefore transparent for radiation at wavelengths higher than about 1.2 μm, which makes it a perfect material for waveguiding and optical signal transmission at telecommunications wavelengths (1.3–1.6 μm). However, its low absorption is opposite to what is required when trying to make integrated photodetectors on silicon. Efficient light signal detection, as a key process for communications, is thus difficult using silicon. Following an approach similar to that used for silicon hybrid integrated lasers based on the wafer bonding of group-III/V materials on top of patterned SOI wafers, silicon waveguides with group-III/V capping materials have been demonstrated as evanescent-field detectors by various groups [33,34]. The 30 μm-long hybrid waveguide evanescent-field detector developed by Brouckaert *et al.* [34] has
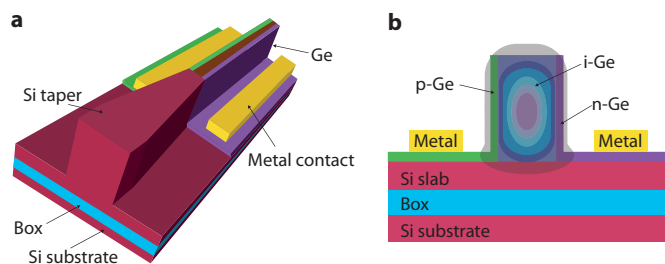
Figure 4. Schematic illustration of a butt-coupled germanium photodetector integrated with an SOI waveguide. (a) Three-dimensional structure. (b) Cross-section view of the germanium p–i–n region. Adapted from Ref. 42 (© 2009 AIP).

a response of was $1.0 \, A \, W^{-1}$ at a wavelength of 1,550 nm with dark current of 4.5 nA and bias voltage of 5 V. Although the performance of such hybrid photodetectors is satisfactory, the wafer bonding process is not CMOS-compatible.

Germanium, with a bandgap of 0.67 eV, has strong absorption at telecommunications wavelengths. It is also potentially suitable for CMOS-compatible processing through the epitaxial growth of pure germanium on top of silicon. Much engineering effort was devoted to improving the efficiency of germanium-on-silicon photodetectors in the early stage of their development [35]. However, the lattice constant of germanium is 4% larger than that of silicon, which poses a problem when germanium is employed as a photon-absorbing material grown on a silicon substrate. Engineering of the strain in SiGe structures for detectors has produced impressive results. compressive-strain-induced defects will normally increase the dark current of p–i–n photodiodes. A two-step germanium growth technique with subsequent annealing is now widely used to prevent 'islanding' during ultrahigh-vacuum chemical vapor deposition and to reduce defect generation [36]. By releasing the compressive strain arising from lattice mismatch through the introduction of a low-temperature buffer layer, the tensile strain caused by the difference in thermal expansion coefficients was shown to improve the performance of germanium-on-silicon diode photodetectors [37]. The performance of these photodetectors today is approaching that of III-V detectors in terms of speed and sensitivity. A more detailed review on the recent progress in germanium-on-silicon photodetectors can be found in Refs 4 and 38.

In 2007, high-performance germanium detectors integrated into silicon waveguides were reported by various groups [39–41]. Longer absorption lengths and much smaller devices could be realized by waveguide integration, leading to higher quantum efficiency, higher bandwidth and lower dark current. The most recently reported device, a silicon waveguide with integrated germanium p–i–n detector, has a sensitivity of $1.1 \, A \, W^{-1}$ and a 3 dB bandwidth of over 32 GHz [42]. The device structure is shown in Figure 4. Dark current, however, is somewhat high (1.3 μA). In 2009, a germanium/silicon avalanche photodetector (APD) was demonstrated [43]. This device had a 340 GHz gain-bandwidth product and a sensitivity equivalent to the commercially available III-V compound APDs. A new type of germanium APD structure integrated on SOI reported recently has a smaller footprint, lower bias voltage and lower noise [44]. There are also efforts to combine novel components into the device structure, such as dipole antennas in order to enhance the performance of integrated germanium photodetectors [45].

Pure silicon crystals can absorb below-bandgap radiation (*e.g.* telecommunications wavelengths) via two-photon absorption (TPA) at high intensities. TPA in a silicon waveguide p–i–n diode has been used to detect light pulses for autocorrelation measurement [46]. The approach has also been adopted in communications systems, for example, to facilitate pulse compression and laser mode-locking. The feasibility of TPA-based high-speed photodetectors, as an all-silicon solution for integrated optoelectronic circuits with useful square-law

properties, has been studied theoretically [47]. Experimental results have since demonstrated cavity enhancement in TPA on silicon waveguides through the design of photonic crystal structures [48] and microdisk resonators [49]. However, the sensitivity and bandwidth of TPA-based photodetectors remain several orders lower than those for integrated germanium-on-silicon photodetectors, making TPA-based devices suitable only for certain specialized applications such as optical power monitoring or channel tone detection, rather than as general-purpose receivers for optical signals.

The absorption of below-bandgap radiation can be dramatically enhanced by defect states in silicon crystal, which can be induced by ion implantation. An in-line channel power monitor based on helium ion implantation in SOI waveguides was demonstrated by Liu *et al.* in 2006 [50]. Geis *et al.* [51] achieved a photon sensitivity of $0.5–0.8 \, A \, W^{-1}$ and 3 dB bandwidth of 10–20 GHz at a reverse bias voltage of 5 V for all-silicon, ion-implanted, submicrometer-sized waveguide p–i–n diodes. This type of integrated photodetector requires just two fabrication steps, both of which are fully CMOS-compatible: ion implantation and low-temperature annealing. The fabrication is much easier than that requiring the epitaxial growth of 100% germanium on a silicon wafer or wafer bonding of III/V materials on top of a silicon waveguide layer as mentioned above. However, the absorption coefficient of ion-implanted silicon is still much lower than that for germanium at a wavelength of 1.55 μm, which will limit the performance of photodetectors in terms of device footprint, 3 dB bandwidth and leakage current.

Fiber–chip coupling

Most applications of silicon-based OEICs require an interface that connects with the single-mode optical fibers used widely in telecommunications systems. Simple butt-coupling of the single-mode fiber to the facet of a silicon nanophotonic waveguide will give a coupling efficiency of less than −20 dB because of the large mode mismatch between the optical fibers (~75 μm² effective area) and the nanophotonic waveguides (~0.2 μm² effective area). Improving the coupling efficiency is therefore a major task in device engineering to facilitate the further commercialization of OEICs. End-fire coupling techniques using inverse tapers [52,53], grating directional couplers [54] and 3D tapers [55] as mode converter have been studied. Coupling efficiency of better than −1 dB can normally be achieved using the inverse taper approach, the best results for which, 0.25 dB polarization-insensitive coupling loss and a 1 dB bandwidth of 150 nm, were obtained recently by Bakir *et al.* [56].

However, these couplers need to be located at the edge of the chip, and cannot be used without careful polishing of the edge facets or precise control of the cleave process. A small-core optical fiber would also be required for highly efficient coupling in butt-coupling approaches. Strongly diffractive waveguide grating couplers [57] were initially demonstrated in 2002 by the group from Ghent University as an alternative coupling technique. These waveguide grating couplers have become of immense practical interest in recent years because of their many advantages, which include simpler back-end processing without facet polishing, flexibility of placement of the optical input/output (anywhere on the chip), and compatibility with wafer-scale testing before dicing.

In a grating coupler, the fundamental mode from the nanophotonic waveguide is first expanded laterally by an adiabatic taper into a waveguide of about 10 μm width, which matches the mode size of an optical fiber on the *y* axis (Figure 5). The light is then coupled out by the diffraction of shallow-etched gratings into the optical fiber. The etching depth of the grating is calculated to achieve optimized coupling strength and diffraction directionality. The period needed for out-of-plane coupling with diffraction angle θ (the angle of the output light to the surface normal of the SOI wafer) is calculated from the phase matching condition.
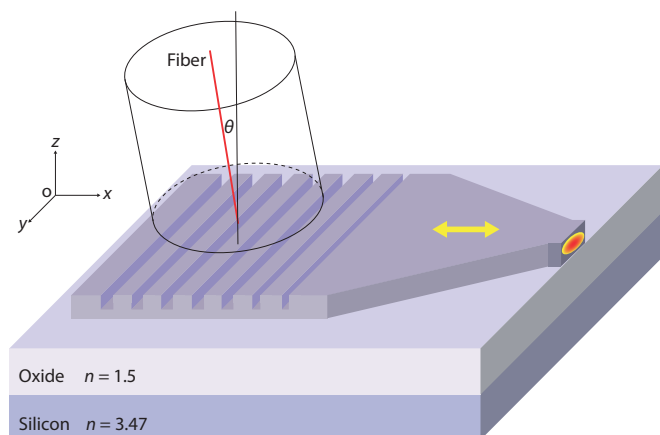
Figure 5. Schematic illustration of an apodized waveguide grating coupler between an optical fiber and nanophotonic waveguide. θ is the angle of the fiber axis to the surface normal of the SOI wafer, and the yellow arrow indicates the direction of light propagation.

For most of the grating couplers demonstrated to date, the optical fiber is orientated with an angle θ of about 10° [58]. This is to avoid the large second-order Bragg back reflection, which would otherwise reflect about half of the optical power back into the waveguide. Precise alignment of the angle between the optical fiber and the grating would introduce additional complexity into the optical alignment process compared with the alignment of a fiber orientated normal to the surface. Various grating coupler designs for realizing efficient coupling between photonic-wire waveguides and vertical optical fibers have been proposed on the basis of simulation results. However, the fabrication processes for vertical-coupling designs are more complicated compared with normal grating couplers. The first practical design achieving highly efficient coupling to a vertical optical fiber was demonstrated recently based on the use of a section of chirped grating [59]. Coupling efficiency of 34%, comparable with that for shallow-etched grating couplers with tilted optical fibers, was achieved experimentally using this device.

Although several different designs of fiber-to-chip grating couplers have been demonstrated, including shallow-etched gratings [57–59], slanted gratings [60] and metallic gratings [61], the coupling efficiency reported for practical implementations and experimental measurements of those designs is limited to around 40%. Two main factors limit the coupling efficiency of grating couplers. One is the poor directionality of grating diffraction. Directionality in this sense is usually defined as the fraction of light power that is coupled upwards, normalized with respect to the total out-coupled optical power. A significant part of the light power leaks into the substrate during grating diffraction. Substrate mirrors based on a metallic layer or Bragg grating can be added to reflect the down-coupled light [62]. The directionality can also be improved by inserting an additional polysilicon layer and optimizing the etch depth of the grating [63]. By applying either of these approaches, a coupling efficiency of 69% has been obtained experimentally [62]. The other factor limiting the coupling efficiency is the mode mismatch between the field profiles of the diffracted light from the waveguide gratings and the fiber mode. An exponentially decaying field profile is generally expected when light is diffracted from a uniform grating, and this would theoretically limit the coupling efficiency to 80% for coupling with the Gaussian-like mode profile of an optical fiber. By engineering the coupling strength (or leakage factor) of the grating structure, a Gaussian-like profile from waveguide gratings can be achieved. Such an approach was recently experimental demonstrated with apodized gratings [64,65]. The highest coupling efficiency obtained to date, 76% experimentally measured, was reported for this type of grating coupler with optimized directionality of diffraction [65].

In addition to the coupling of light between waveguides and optical fibers, waveguide grating couplers can offer additional functionality such as polarization or power splitting [66,67]. Compact grating components can be used in many useful SOI devices. For example, two-dimensional grating couplers can be used for polarization-diversity schemes in order to facilitate polarization-independent operation of OEIC devices [68]. The randomly changing polarization in the optical signal received from a conventional optical fiber communications link can be coupled into the transverse electric mode of two orthogonally orientated SOI waveguides connected to two sets of identical photonic integrated circuits, or to the same photonic circuit but with the light propagating in opposite directions. Grating power splitters can be used in MZI devices for functions such as wavelength filtering, signal modulation and demodulation, and package switching.

For all the grating couplers mentioned above, the lithography and etching processes needed to fabricate the grating structures must be distinct from the corresponding fully etched waveguides because of the different etch depths or special fabrication techniques required for the grating couplers. Fully etched subwavelength grating couplers that can be fabricated in the same etch step as the waveguides were first experimentally demonstrated in 2009 [69]. Subwavelength structures were adopted to reduce the large refractive index step of the grating so as to reduce the back reflection into the waveguides. Thus, no additional fabrication step is required for these grating couplers. Apodized subwavelength grating couplers have also been recently demonstrated [70].

Future trends

Beyond silicon-based devices for data communications applications, silicon photonics at mid-infrared wavelengths is now emerging as a new frontier. Many groups around the world are starting to work in this area because of the important potential applications envisaged for this technology, including chemical and biological sensing, trace-gas detection and environmental monitoring [71]. The potential of seamless integration of multiple components on a single chip offers an attractive solution for mid-infrared applications. Soref *et al.* [72] preformed a theoretical study of various types of optical waveguides for longer wavelength transmission in 2006. Silicon-on-sapphire grating couplers [73] and waveguides [74] have since been experimentally demonstrated at mid-infrared wavelengths. A silicon cascaded Raman laser was demonstrated by Rong *et al.* [75], who developed an interesting approach with the potential for use in the fabrication of room-temperature lasers at mid-infrared wavelengths. Raman amplification in the mid-infrared has also been demonstrated in bulk silicon [76]. The absence of TPA at mid-infrared wavelengths offers intriguing opportunities for the study and applications of nonlinear optical effects, and may find applications in new laser systems or gas-sensing platforms [71,76].

Optomechanical devices on the SOI platform are also attracting interest because of the potential for their integration into novel nanooptoelectromechanical systems-on-a-chip. A detailed review is presented by van Thourhout and Roel [77].

Although crystalline silicon on SOI has been the dominant material of choice for integrated silicon photonics, practical considerations for integration of high-density photonic circuits with complex multilayer CMOS electronic circuitry may make it necessary to use materials that are more compatible with mainstream microelectronics, which typically rely on silicon rather than SOI wafers. There is an increasing need for a novel approach for the fabrication of photonic circuits that provide the freedom to stack multilayer photonic layers in between electronic layers. Such a process should also be also compatible with CMOS back-end processes, where the maximum temperature is restricted to 400 °C. Hydrogenated amorphous silicon (a-Si:H) is a promising candidate for this type of application. Photonic-wire waveguides with dimensions of 480 nm in width and 220 nm in

thickness were demonstrated in 2008, achieving a loss of $3.46\,dB\,cm^{-1}$ at 1,550 nm [78]. This performance is approaching that (1–$3\,dB\,cm^{-1}$) for crystalline-silicon waveguides with a similar structure. The bulk material loss of a-Si:H is estimated to be ~$0.7\,dB\,cm^{-1}$. A racetrack ring resonator with a Q of 10,000 has been demonstrated, together with many other passive integrated devices. Even lower loss in wire waveguides based on amorphous silicon was reported recently by Zhu *et al.* [79]. Their device was prepared by plasma-enhanced chemical vapor deposition using an optimized deposition process. However, the thermal stability of such materials is still questionable. The optical loss of a-SI:H will increase dramatically under low-temperature treatment, caused mainly by hydrogen out-diffusion.

The high cost of fabrication facilities has started a trend towards 'fabless' silicon photonics [80], comparable to similar developments in CMOS technology. In this approach, a research group can design photonic circuits occupying a footprint of a few square millimeters and rely on a foundry for a multiproject run at a cost of tens of thousands of dollars US for fabrication, a fraction of the total cost of the fabrication process for full SOI wafers. The fabrication equipment needed for making integrated photonic circuits is very expensive. The costs incurred in the preparation of high-resolution reticles, the depreciation of expensive equipment and other overheads associated with the running of high-quality cleanrooms would normally pose a significant hurdle for research groups working on silicon photonics. Organizations offering the ability to build passive and active photonic circuits, such as EPIXfab in Europe, provide affordable access to near state-of-the-art CMOS fabrication facilities, and such facilities have certainly boosted the development of silicon photonics.

Conclusion

The development of silicon photonics has seen enormous progress over the last decade. Silicon photonics is being used to make commercially competitive devices that provide the modulation and detection functions needed in data communications, telecommunications systems and optical interconnects. Exciting new applications are emerging in sensing, mid-infrared optics and optomechanical systems. Silicon photonics will likely eventually make a revolutionary impact in the high-volume data communication and computing industries.

Acknowledgments

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