Thin dielectric films

Uncorrelated breakdown of integrated circuits

In thick dielectrics, electrical breakdown is caused by the generation of spatially and temporally correlated defects that are produced — as in lightning[1] — by feedback between defect formation and local stress[2]. New defects are created in the vicinity of existing defects, leading to rapid and correlated propagation of field-induced defect chains that cause breakdown. By contrast, we show here that defects formed in ultrathin films subjected to realistic electrical stress remain spatially and temporally uncorrelated, even when multiple 'shorts' (chains of defects) begin to bridge the thickness of the films. Besides their relevance to different applications of thin dielectric films, our results have positive implications for the scalability of modern integrated circuits[3–6].

To investigate the correlation in defect generation and formation of shorts, we electrically stressed the thin gate dielectrics in about 100 field-effect transistors (FETs) by applying a voltage to the gates and then monitoring the terminal currents as defects accumulated (Fig. 1a).

The discrete and irreversible jumps in the gate current (Fig. 1b) that accompany the formation of individual shorts, as current increases through the low-resistivity paths, enabled us to determine the number of shorts (n) present at a given time, and the time of appearance (t_n) of each short. Likewise, the ratio of the discrete increases in the source and drain currents determines the position (x_n) of these shorts[7].

To analyse the degree of correlation in our measurements, we used the theoretical framework of a three-dimensional cubic-lattice percolation model[8,9]. If a film of thickness T_{film} and area A_{film} is stressed at constant voltage, and if the defect generation is spatially and temporally uncorrelated, then the theory makes two key predictions.

First, the cumulative probability distribution of the distances between pairs of shorts should be characterized by the correlation distance $L_c \to 1$ (M.A.A. and R.K.S., unpublished results). The measured locations of the shorts are characterized by an effective correlation distance of $L_c^{eff} \geq 0.83$, indicating that the spatial correlation is weak. Second, a single-parameter scaling relation

$$F_n = 1 - e^{-\chi}\left(\sum_{k=0}^{n-1} \chi^k/k!\right) \qquad (1)$$

where F_n is the fraction of samples with at least n shorts at time t, must hold. The scaling parameter $\chi = KA_{film}t^{\beta}$, where K is the stress-dependent constant, and $\beta \propto T_{film}$. The results shown in Fig. 1c for each F_n can be inverted by using equation (1) to obtain χ, and then used to predict $F_{1\to n} = 1 - e^{-\chi}$.

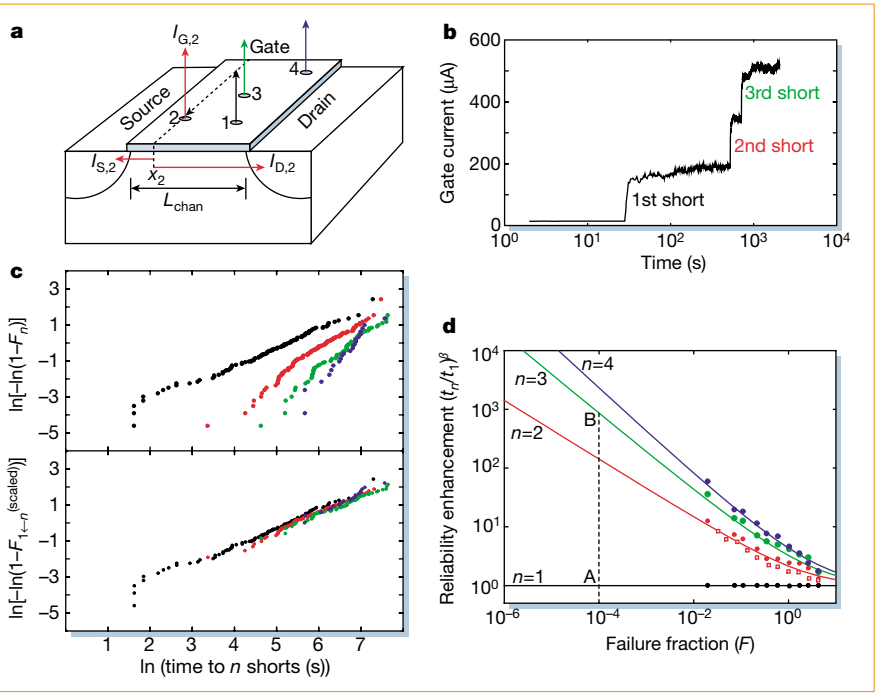

Figure 1 Uncorrelated breakdowns in thin dielectric silica films. **a,** Gate dielectric of a field-effect transistor (shaded) configured to study the evolution of n shorts (n is 1, 2, 3 or 4) and the underlying correlation in defect generation in thin films. Each new short is registered by a discrete jump in the gate current, $I_{g,n}$, balanced by discrete increases in source and drain current, $I_{s,n}$ and $I_{d,n}$, which can be used to time and locate the shorts (for example, short 2 occurred at a distance x_2 from the source along the channel length L_{chan}). **b,** Timing of shorts as a function of gate current. **c,** Measured time sequence for samples with identical area and thickness to develop at least n shorts. Top, traces measured as for **b** are used to compute F_n, the cumulative failure distributions with at least n measured shorts (n is 1–4; $T_{film} = 1.7$ nm, $A_{film} = 2.5$ μm^2); bottom, the coincidence of the $F_{1\leftarrow n}$, derived from F_n using equation (1), shows that these shorts are uncorrelated in location and time ($n = 1$, measured; when n is 2–4, scaled). **d,** Improvement in functional reliability as a function of F. The time, t_n, at which a fraction of integrated circuits with n faults (F_n) fails depends on the ability of the FET to survive $n-1$ shorts without logic failure. Data from oxides of different thickness and area (filled and open symbols), stressed under different conditions, support the scaling theory (solid line). If only 1 out of 10,000 integrated circuit failures is acceptable for a technology, A→B shows the relative improvement in reliability provided that the circuit can sustain just two shorts.

The coincidence of these plots in Fig. 1c shows that equation (1) describes the data well. We find that equation (1) holds for films of different thickness and area, subjected to electrical stresses of different duration and field strength, indicating that the spatial and temporal distributions of the shorts in thin films are essentially uncorrelated.

Historically, silicon FETs used thicker silica films as gate insulators. For these films, the initial short was so catastrophic and subsequent defect generation so strongly correlated that the FET, and consequently the integrated circuit, could no longer perform logic operations. By contrast, modern FETs[4] use thinner films operated at lower voltages, so that the individual uncorrelated shorts are too 'soft' to cause logic malfunctions[10].

If an FET is fault-tolerant up to $(n-1)$ shorts, the operating lifetime (t_n) of the integrated circuit will increase geometrically (from equation (1)) over the traditional fault-intolerant lifetime (t_1); that is, $(t_n/t_1)^{\beta} \approx (n/e)(2\pi n)^{(1/2n)}/F_n^{(1-1/n)}$ (Fig. 1d). For $\beta \approx 1$, an acceptable failure fraction of $F_n = 10^{-4}$ (point A, Fig. 1d), and an integrated circuit that is fault-tolerant to two shorts, the integrated circuit will function for almost 1,000 times as long as would be predicted on the basis of the model for bulk dielectric breakdown ($t_3 \approx 850t_1$; point B, Fig. 1d).

Our results indicate that most modern integrated circuits may have been unintentionally overdesigned for reliability, and that it is possible to design faster integrated circuits with higher operating voltage without sacrificing functional reliability. Although issues such as power management, shallow junction formation and so on remain and must be addressed[5,6], our findings allow a relaxation of the speed–reliability constraint that effectively removes oxide breakdown as a fundamental obstacle to continued scaling of silicon integrated circuits.

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