New recipe for a wee DRAM

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As electronics technology moves to ever-increasing densities and speeds, it is necessary to shrink the footprint of the integrated capacitors that represent digital bits in devices such as dynamic random access memories (DRAMs), and to integrate previously discrete components such as the decoupling capacitors used for noise suppression in high-frequency digital applications. Unless new architectures are developed, the charge stored per capacitor must also remain fairly constant from device generation to generation, so as to ensure reliable operation with a reasonable signal-to-noise ratio. Clearly these conflicting design rules imply that cell capacitance per unit area must increase, even as conventional integrated dielectrics based on silicon dioxide and Si_3N_4 approach their scaling limits. On page 215 of this issue, Cava *et al.*[1] describe the synthesis, through TiO_2 substitution into Ta_2O_5, of an attractive replacement candidate.

Shrinking strategies

To increase the capacitance per unit of projected area (footprint) occupied by an integrated capacitor structure, three strategies may be pursued. First, one may simply decrease the thickness of the dielectric layer, as capacitance is inversely proportional to electrode separation for a planar device. But with the introduction of 64-Mbit DRAM designs, traditional dielectrics such as amorphous silicon oxide and silicon oxide–nitride–oxide heterostructures will reach practical limits, given by such factors as minimum thickness required to form a pinhole-free layer and to prevent significant leakage through electron tunnelling.

Second, one may increase the capacitor area per footprint area of the cell by introducing such three-dimensional structures as trenches, stacks, fins and crowns, or by introducing microstructural roughness by growing the dielectric on a rough bottom electrode[2]. This approach is bounded from two directions — by the increase in leakage current with increasing roughness, and by the depth-of-field limitations of photolithography and other planarity requirements on device integration and circuit fabrication. This approach should provide sufficient stored charge per bit using currently available materials for the 256-Mbit and perhaps 1-Gbit generations.

The final strategy is clear: use of new materials with higher permittivities as the capacitor dielectric. But introduction of novel materials into a semiconductor fabrication facility is not approached lightly, given the sensitivity of semiconductor devices to contamination and the billion-dollar investment that manufacturing facilities represent. Clever manipulation of device geometry has postponed this eventuality and greatly prolonged the service lifetime of the standard integrated dielectrics. Inevitably, though, the silicon-based materials currently in use will have to be replaced by advanced materials with much higher dielectric constants.

The foremost long-term candidates for this application are all members of the class of perovskite-derived ferroelectrics, including $SrTiO_3$, $BaTiO_3$ and other compounds, with relative permittivities (or dielectric constants, ε_r) ranging from about 200 to well into the thousands (SiO_2 has $\varepsilon_r=4$; Si_3N_4 has $\varepsilon_r=7$). $(Ba,Sr)TiO_3$ (ε_r= 300–800) is perhaps the leading contender in this class, and most of the main DRAM manufacturers in the United States and Asia are devoting much research to it. For Ba/Sr ratios chosen so that the Curie point is pushed below operating temperatures, it benefits from low frequency dependence and excellent temperature stability of its permittivity.

Still, substantial barriers stand in the way — poor understanding of material properties and their variability (particularly leakage current and time-dependent polarization phenomena, which affect the voltage retention and switching speed of the capacitor); the lack of a well-established electrode technology, and process integration with the underlying silicon integrated-circuit technology; and questions about the long-term reliability. Film fabrication by chemical vapour deposition is the accepted way to achieve sufficient step coverage at the length scales and aspect ratios that will be dictated by future DRAM design rules. The process has been demonstrated for the ferroelectrics[3–5], but scale-up to industrial size for these oxides is only now beginning and presents its own challenges. Last and by no means least, these materials would require the introduction of barium and strontium into the fabrication process — relatively unfamiliar elements with unknown consequences.

Single-component oxides are the primary short-term competitors of the ferroelectrics, generally offering far fewer process integration problems, but with much lower relative permittivities (in the range of 20 to 100). Of these, Ta_2O_5 has been mooted for many years[6–8]. Tantalum is already accepted in manufacturing facilities, and chemical vapour deposition of its oxide is well established. However, its relative permittivity is at best only 35, and when integrated directly onto a polysilicon bottom electrode, an SiO_2 interfacial layer is formed that limits the maximum attainable capacitance of the heterostructure. This offers just one device generation beyond current dielectrics, not enough to warrant extensive commercialization.

Cava and co-workers[1] may now have shifted this materials equation. By incorporating TiO_2 (another acceptable manufacturing material) into Ta_2O_5, they have succeeded in substantially raising the permittivity of the compound, peaking with $\varepsilon_r=126$ at 1 MHz for substitution of 8 per cent TiO_2. If the permittivity increase can be replicated in thin films with a suitable bottom electrode, and other materials properties such as leakage current are acceptable, it would make possible a reduction in capacitor area satisfactory for at least two future DRAM generations, using a dielectric that may be more readily accommodated into existing strategies for device fabrication.

Structural change

How does it work? That question cannot yet be answered properly. The dielectric constant of polycrystalline TiO_2 reaches about 100, so it is attractive as a dopant simply on the basis of its own polarizability (pure TiO_2 itself is not of use because it reduces easily, leading to unacceptably large leakage currents). The authors note that the observed permittivity increase occurs with a change in crystal structure of the oxide to a monoclinic modification and only with TiO_2 substitution. So they propose that a structural distortion specific to Ti incorporation into the Ta–O framework leads to the increase in dielectric constant. The crystal chemistry of Ta_2O_5 is complex, however, and the specifics of the phenomenon warrant more investigation.

Ultimately, the choice of dielectric for commercialization will depend on dielectric constant and other properties related to capacitor performance, and on ease of incorporation into a mass-produced device. It remains to be seen whether thin-film Ta_2O_5–TiO_2 will present enough of an advantage over current materials, and have a sufficient manufacturability edge over ferroelectrics, to make the transition to market. □

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