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Interface Engineering for the Enhancement of Carrier Transport in Black Phosphorus Transistor with Ultra-Thin High-*k* Gate Dielectric

Zhi-Peng Ling[1], Jun-Tao Zhu[1], Xinke Liu[2] & Kah-Wee Ang[1]

Black phosphorus (BP) is the most stable allotrope of phosphorus which exhibits strong in-plane anisotropic charge transport. Discovering its interface properties between BP and high-*k* gate dielectric is fundamentally important for enhancing the carrier mobility and electrostatics control. Here, we investigate the impact of interface engineering on the transport properties of BP transistors with an ultra-thin hafnium-dioxide (HfO_2) gate dielectric of ~3.4 nm. A high hole mobility of ~536 $cm^2V^{-1}s^{-1}$ coupled with a near ideal subthreshold swing (*SS*) of ~66 mV/dec were simultaneously achieved at room temperature by improving the BP/HfO_2 interface quality through thermal treatment. This is attributed to the passivation of phosphorus dangling bonds by hafnium (Hf) adatoms which produces a more chemically stable interface, as evidenced by the significant reduction in interface states density. Additionally, we found that an excessively high thermal treatment temperature (beyond 200 °C) could detrimentally modify the BP crystal structure, which results in channel resistance and mobility degradation due to charge-impurities scattering and lattice displacement. This study contributes to an insight for the development of high performance BP-based transistors through interface engineering.

The potential of atomically thin two-dimensional layered materials in meeting the performance requirements of international technology roadmap for semiconductors[1] has spun off intense research efforts on graphene[2,3], transition metal dichalcogenides (TMD)[4], and most recently black phosphorus (BP) crystal[5]. In particular, BP is known to be a promising channel material for future nanoelectronics applications owing to its superior carrier transport and direct bandgap properties for all layer thicknesses. This ranges from ~0.3 eV in the bulk form[6,7] and increases to ~2 eV when the BP thickness is reduced to monolayer form[8]. Excellent electron and hole mobilities reaching ~15,000 $cm^2V^{-1}s^{-1}$ and ~50,000 $cm^2V^{-1}s^{-1}$, respectively, have also been reported in bulk BP single crystal[7]. Although a handful of BP transistors have been previously demonstrated[9–17], the device performance is still far from satisfactory. Furthermore, to be CMOS compatible, the integration of a high-temperature thermal anneal is typically required to improve device performance. Some initial studies on the role of temperature on BP film structure and device performance have been reported[18–22]. With increasing anneal temperatures, Liu *et al.*[19] showed the decomposition of BP film at 400 °C and a temperature induced increase in lattice parameters as confirmed by *in situ* scanning/transmission electron microscopy measurements in the vacuum state. For practical applications, surface passivation of the BP channel is necessary to address photo-oxidation issue[23]. When BP is passivated with hexagonal boron nitride (h-BN), an insulating 2D material, the device shows a significantly higher temperature tolerance up to 500 °C[18]. The high temperature anneal can help to suppress the charge trap states, leading to low hysteresis, improved mobility and high on-off ratios (>10[5]). Although h-BN is a possible candidate for device integration, the relatively low dielectric constant (<4)[24] severely limits its potential for highly scaled transistors. Thus, there is a demand for suitable high-*k* gate dielectrics to improve the device performance. One possible high-*k* dielectric candidate is hafnium-dioxide (HfO_2) which has a dielectric constant of ~25[25], which is six times higher than the conventional SiO_2 dielectric. Although some preliminary BP transistors have been

[1]Department of Electrical and Computer Engineering, National University of Singapore, 4 Engineering Drive 3, Singapore 117583. [2]College of Materials Science and Engineering, Shenzhen Engineering Laboratory for Advanced Technology of Ceramics, Nanshan District Key Lab for Biopolymer and Safety Evaluation, Shenzhen University, 3688 Nanhai Ave, Shenzhen 518060, People's Republic of China. Correspondence and requests for materials should be addressed to X.L. (email: xkliu@szu.edu.cn) or K.-W.A. (email: eleakw@nus.edu.sg)
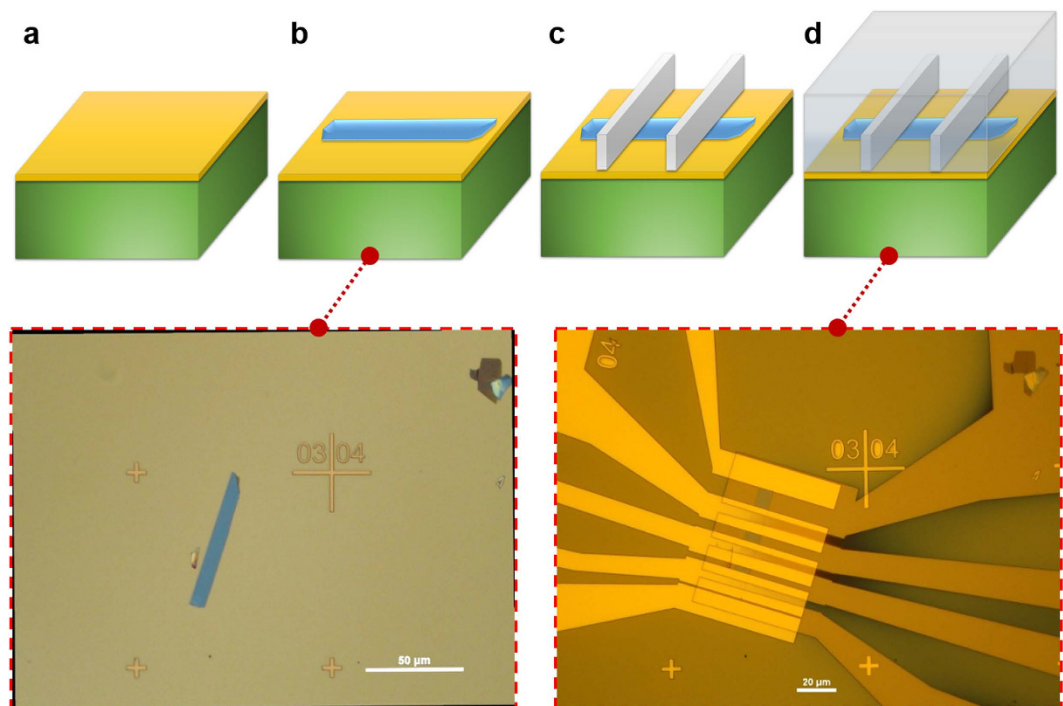
Figure 1. The fabrication flow for the black phosphorus transistor based on low temperature CMOS-compatible processes. (**a**) Using a degenerately doped Si substrate, an ultra-thin hafnium-dioxide gate dielectric of ~3.4 nm is deposited using atomic layer deposition (ALD) technique at a temperature of 250 °C. (**b**) BP nanosheet with a ~15 nm thickness is micromechanically exfoliated onto the high-k gate dielectric. (**c**) Metal electrodes utilizing nickel with a thickness of 120 nm are formed by a combination of electron beam lithography and electron-beam evaporation followed by the lift-off process. (**d**) An additional surface passivation by a 30 nm thick SiO_2 layer is deposited to protect the as-fabricated devices from photo-oxidation in ambient conditions.

realized on HfO_2 or Al_2O_3 gate dielectric, poor subthreshold swing performance of the order of 0.3~1.1 V/dec and carrier mobility below ~310 $cm^2V^{-1}s^{-1}$ were reported. Moreover, there are limited reports on the application of thermal treatment to improve the BP/high-k interface quality for enabling further performance enhancement.

In this work, we report the realization of BP transistors with a near ideal subthreshold swing (~66 mV/dec) and enhanced hole mobility (~536 $cm^2V^{-1}s^{-1}$) through the use of an ultra-thin hafnium-dioxide (HfO_2) gate dielectric and interface engineering. We further investigate the influence of thermal treatment on the structural and electrical properties of the BP transistors. Detailed material studies are performed using X-ray photoelectron spectroscopy, Raman spectroscopy and energy-dispersive X-ray spectroscopy to analyze the structural integrity and interface properties between the BP and HfO_2 gate dielectric. Comprehensive electrical performance metrics including subthreshold swing, hole mobility, transfer characteristics, and channel resistance are systematically analyzed.

Results and Discussion

Figure 1 shows the low temperature fabrication flow used to realize the black phosphorus (BP) transistor with an ultra-thin high-k gate dielectric. The devices feature a back-gate configuration with a minimum gate length of ~3 μm. A CMOS-compatible metal such as nickel (Ni) was used to form the metal electrodes[26]. The as-fabricated transistor was passivated with a 30 nm silicon-dioxide (SiO_2) layer deposited by e-beam evaporator at room temperature to protect the device from photo-oxidation in the ambient condition. A detailed description of the process is provided in the experimental method section. The devices realized in this work demonstrate a clear p-type behavior as depicted in Fig. 2, in which the room temperature transfer curves (I_{DS} - V_G) are plotted at the same drain voltage (V_{DS}) of −100 mV. In the as-fabricated state, the BP transistor shows a significantly improved subthreshold swing (SS) of ~76 mV/dec as compared to other BP transistors based on traditional SiO_2 gate dielectric ($SS > 1$ V/dec)[9–17] or Al_2O_3 gate dielectric ($SS \sim$ 350–850 mV/dec)[15,27], as benchmarked in Fig. 3. The improved SS performance implies the effectiveness of ultra-thin high-k gate dielectric in providing excellent gate control over the source-to-drain current, which enables BP transistor to achieve better electrostatics control. When subjected to an additional interface anneal for one minute under nitrogen (N_2) ambient, the SS performance was shown to improve further and reaching a near ideal value of 66 mV/dec at room temperature ($T = 300$ K). Such a significant improvement is resulted from a better BP/HfO_2 interface due to the passivation of phosphorus dangling bonds by hafnium (Hf) adatoms as promoted by the thermal treatment. This can be evidenced from the strong P-Hf binding energy at ~135.6 eV over the P-P binding energy at ~131.1 eV, as confirmed by the P 2p core level obtained from X-ray photoelectron spectroscopy (XPS) measurement in Fig. 4. The binding energies of all spectra
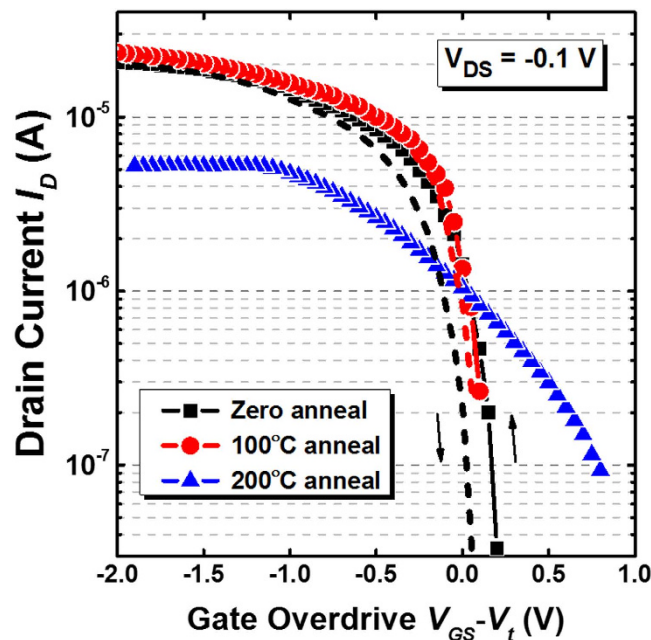
Figure 2. A comparison of the transfer characteristics of the black phosphorus transistors with and without interface annealing. With an excessively high thermal budget, the subthreshold swing of the BP transistor can be significantly degraded, which is attributed to the detrimental change of the BP film crystallinity. When subjected to a 100 °C thermal anneal, an off-state current of $\sim 8.09 \times 10^{-7}$ A was measured in the BP transistor. However, an improved hysteresis performance was estimated in devices which were annealed at 100 °C as compared to the un-annealed devices. This further confirms the achievement of lower D_{it} due to an optimum thermal annealing.
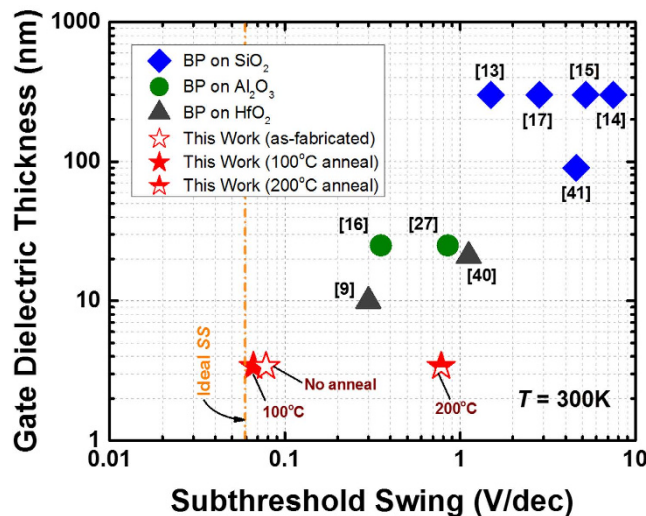
Figure 3. Figure-of-merit showing the relationship between gate dielectric thickness and the subthreshold swing (SS) performance of black phosphorus transistors. A significant SS improvement is observed by downscaling the thickness to ~3.4 nm coupled with an interface anneal process, showing a near ideal value of ~66 mV/dec. This is by far the lowest SS reported, which indicates an enhanced electrostatics control in the BP transistors.

are referenced to C1s which is set to 285 eV. The appearance of P-P peak or the single spin-orbit split doublet at a binding energy of ~131 eV indicates the intrinsic crystallinity of the exfoliated BP on HfO_2 gate dielectric, which is consistent with previous XPS measurements on BP bulk crystals[28,29]. To understand the interaction between Hf and P, first-principles calculations were performed within the density-functional theory (DFT) framework. The results show that Hf adatom prefers the adsorption position above the center of P_6 hexagonal ring or H-site of the phosphorene layer (see inset of Fig. 4), which is consistent with other transition metals reported in previous
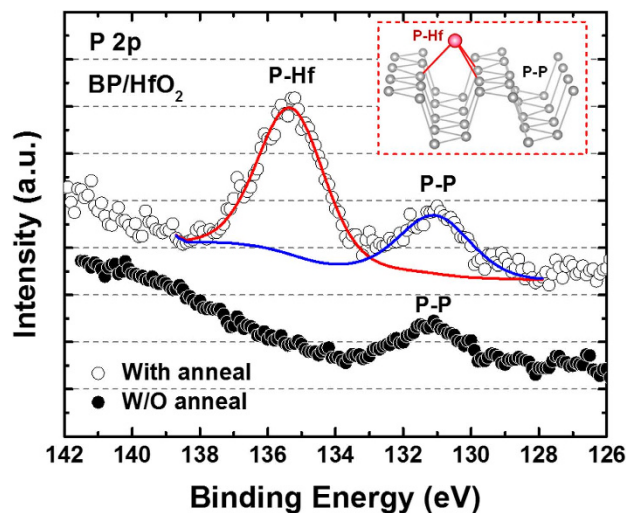
Figure 4. The P 2p core level of X-ray photoelectron spectra (XPS) for the black phosphorus nanosheet formed on HfO₂ gate dielectric. A thermal treatment at 100 °C under nitrogen ambient improves the binding energy of P-Hf, which allows the achievement of better interface quality between BP and HfO₂. The inset shows the formation of covalent bonds between P and Hf adatoms with a strong binding energy of −4.17 eV, as confirmed by the first-principles calculation within the density-functional theory (DFT) framework.

studies[30]. When this occurs, Hf adatom forms strong covalent bond with phosphorene with a binding energy of −4.17 eV. The stronger P-Hf binding has been found to be consistent with a shorter P-Hf bond and larger deformation of phosphorene layer.

To estimate the effective interface state density D_{it}, the subthreshold swing equation $SS = \frac{kT}{q} \ln(10) \cdot \left(1 + \frac{C_S + C_{it}}{C_{OX}}\right)$ can be employed[31], where k is the Boltzmann constant, T is the temperature in Kelvin, q is the electronic charge, C_S is the depletion capacitance of BP, C_{it} is the BP/HfO₂ interface state capacitance, and C_{OX} is the unit gate capacitance. When the applied gate voltage approaches the threshold voltage, the thin pristine BP channel is expected to be fully depleted where the depletion capacitance (C_s) is small as compared to the interface state capacitance (C_{it}). The effective interface state density D_{it} at BP/HfO₂ interface can then be estimated using the expression $D_{it} = \frac{C_{it}}{q} \approx \left(\frac{q \cdot SS}{kTln(10)} - 1\right) \cdot \frac{C_{OX}}{q} - \frac{C_S}{q}$. To give better D_{it} estimation, we have included the contribution of C_s in the calculation where the dielectric constant of BP is taken as $6.1\varepsilon_o$[32] while the depletion width is equal to the thin BP thickness of 15 nm. Based on the extracted SS of 66 mV/dec (annealed) and ~76 mV/dec (un-annealed), the effective interface state density D_{it} at the BP/HfO₂ interface is estimated to be ~6.08×10^{11} cm⁻²eV⁻¹ and ~5.07×10^{12} cm⁻²eV⁻¹, respectively. The substantial reduction in D_{it} by ~88% further confirms the effectiveness of Hf adatoms in passivating the P dangling bonds at the BP/HfO₂ interface, which accounts for the SS improvement.

By extracting the slope in the linear region of the transfer curve, the mobility can be evaluated using the expression $\mu_{FE} = \frac{dI_{DS}}{dV_G} \cdot \frac{L}{WC_{OX}V_{DS}}$ where L is the channel length, W is the channel width, C_{OX} is the capacitance between the channel and the back-gate per unit area and V_{DS} is the voltage between the source and drain electrodes[5]. The extracted field-effect mobility (μ_{FE}) at room temperature is plotted in Fig. 5 and benchmarked against other BP transistors based on traditional SiO₂ or Al₂O₃ gate dielectrics. Even in the absence of thermal treatment, the as-fabricated BP transistor achieves a relatively high μ_{FE} of 413 cm²V⁻¹s⁻¹. Note worthily, the μ_{FE} was shown to significantly improve by ~30% to 536 cm²V⁻¹s⁻¹ when the device was treated at an elevated temperature of 100 °C in nitrogen (N₂) ambient. This is believed to be a record-high hole mobility among other reported data based on HfO₂ or Al₂O₃ high-k gate dielectrics at room temperature ($T = 300$ K). Such an improvement was believed to be attributed to a better BP/HfO₂ interface as a result of phosphorus dangling bonds passivation as discussed in the preceding section. However, a further increase in the thermal budget has been found to degrade the carrier mobility. Noticeably, the μ_{FE} was drastically reduced to 120 cm²V⁻¹s⁻¹ after going through a 200 °C anneal. In order to understand the underlying mechanisms, the BP film structure properties were analyzed using confocal Raman spectroscopy. Figure 6(a) plots the Raman spectra of the BP flake formed on 3.4 nm HfO₂ gate dielectric with a 30 nm SiO₂ passivation layer. When annealed at an elevated temperature, a shift in the Raman phonon peak positions corresponding to A¹_g, B_{2g} and A²_g was clearly evident which is indicative of the film structure modification. A deconvolution of the characteristics out-of-plane mode (A¹_g) and in-plane modes (B_{2g} and A²_g) in Fig. 6(a–c), respectively, further confirms the Raman peak position shifts. Interestingly, the samples in this work exhibited a general blue shift with increasing temperatures up to 200 °C. A significant blue shift of 0.53 cm⁻¹, 1.0 cm⁻¹, and 1.1 cm⁻¹ for the A¹_g, B_{2g} and A²_g vibrational modes, respectively, was observed as compared to the un-annealed case. In contrast, when a conventional SiO₂ dielectric was utilized, both Dattatray[21] and Zhang et al.[22] experimentally showed a rather linear red shift in all three vibrational modes with increasing temperatures from 77 K up to 673 K.
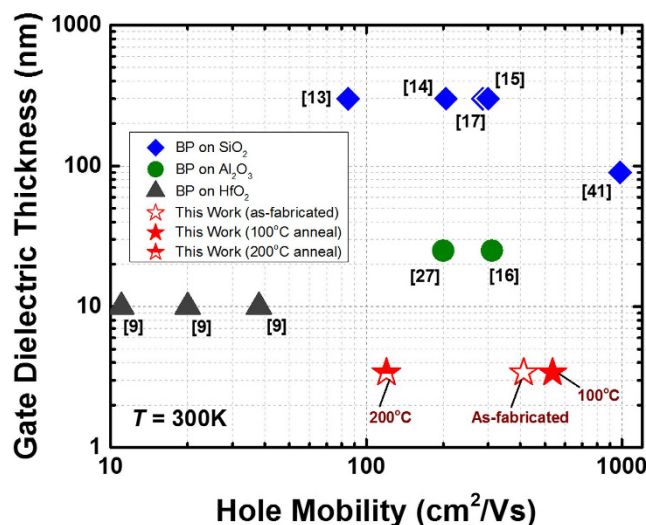
Figure 5. Figure-of-merit showing the relationship between gate dielectric thickness and room temperature hole mobility of black phosphorus transistors. A better BP/HfO_2 interface quality due to the passivation of phosphorus dangling bonds by hafnium (Hf) adatoms has been shown to result in an enhanced hole mobility over the un-annealed device. A mean mobility of $\sim413\,cm^2V^{-1}S^{-1}$ and $\sim536\,cm^2V^{-1}S^{-1}$ were achieved for devices with no anneal and 100 °C anneal, respectively. A further increase of thermal budget beyond 200 °C could significantly degrade the carrier transport due to crystal lattice distortion and impurity scattering effect, leading to a low mean mobility of $\sim120\,cm^2V^{-1}S^{-1}$.
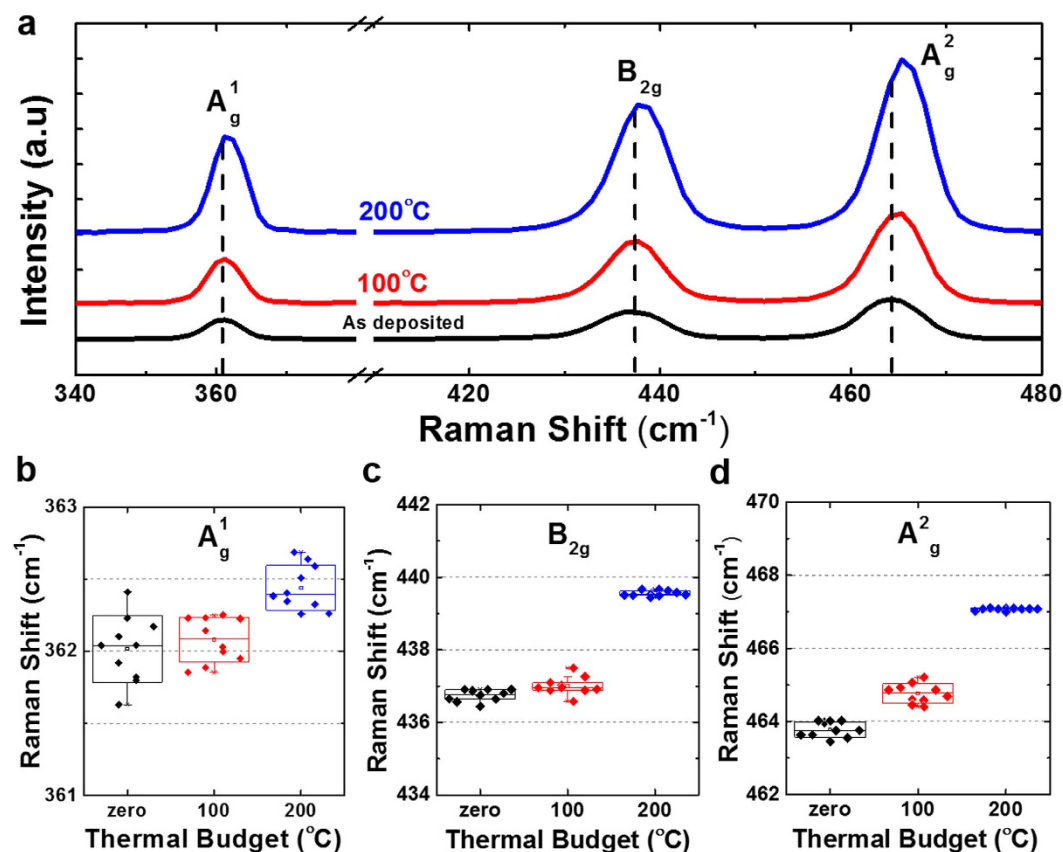
Figure 6. (**a**) Raman spectra of the exfoliated BP nanosheets showed the three characteristic vibrational modes after underwent different thermal anneal for a duration of one minute in nitrogen (N_2) ambient. The deconvoluted Raman peaks corresponding to the out-of-plane phonon mode A^1_g, and in-plane phonon modes B_{2g} and A^2_g, are plotted in (**b–d**), respectively. A clear Raman peak shift is evident with increasing interface anneal temperature, which indicates film structure modification.
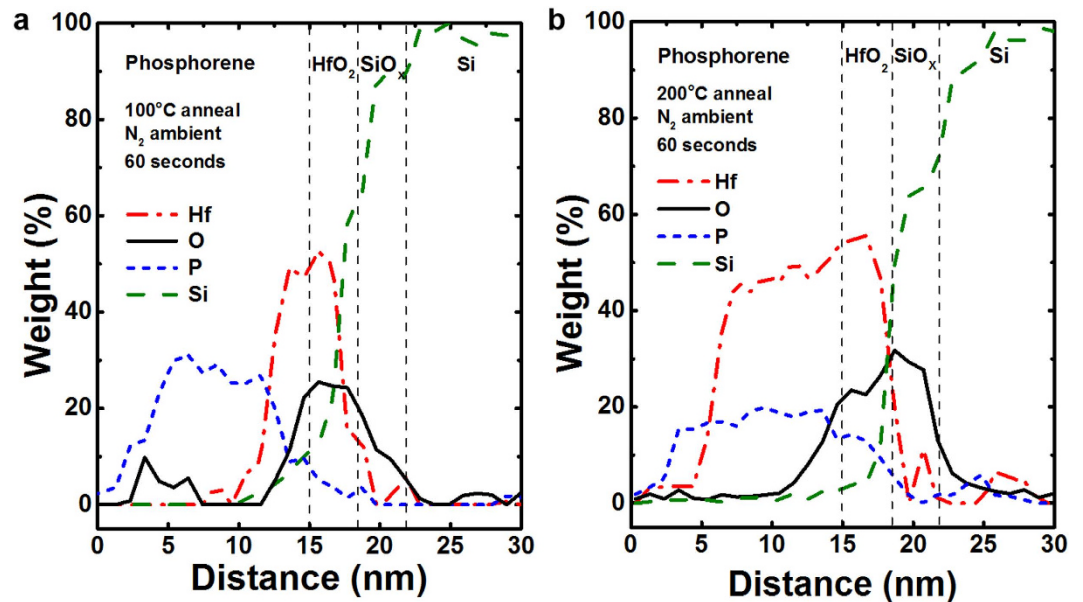
Figure 7. The energy-dispersive X-ray (EDX) spectroscopy measurement confirms the out-diffusion of Hf adatoms from the underlying HfO₂ gate dielectric into BP film when subjected to thermal treatment. (**a**) With a lower thermal budget of 100 °C, the out-diffused Hf adatoms were predominantly found at the BP/HfO₂ interface which promotes the passivation of P dangling bonds. (**b**) However with a further increase of thermal budget to 200 °C, a substantial out-diffusion of Hf adatoms was detected in the BP channel which is responsible for the carrier transport degradation in BP transistors.

To understand this shift further, the first-principles linear response method from Fei et al.[33] can be employed. In particular, the effect of zigzag and armchair strain on the puckered honeycomb structure of the black phosphorus will lead to a shift in the Raman peak positions of the characteristics phonon modes depending on the nature of the strain (tensile or compressive). Comparing our results to the first-principles studies, it appears to indicate the presence of compressive strain in both the zigzag and armchair directions for an anneal temperature up to 200 °C, which is clearly evident from the blue shift of the A^1_g, B_{2g} and A^2_g modes. This could be attributed to the out-diffusion of hafnium (Hf) adatoms from the underlying high-k gate dielectric which compresses the BP channel. According to Clementi et al.[34], the atomic radii of the hafnium (Hf) atoms is 2.08 Å, which is almost two times that of the silicon atoms. In comparison, the atomic radii of the oxygen atoms is 0.48 Å, significantly lower than the hafnium (Hf), silicon (Si), and even the phosphorus (P) atoms (0.98 Å). Hence, in the event of out-diffusion into the BP film, the atom with the largest atomic radii (Hf in our case) is likely to dominate the compressive strain observed. Thus, the incorporation of Hf with a larger atomic radii will be expected to result in crystal lattice distortion in the zigzag direction which will lead to elastic strain effect. However, with a further increase in strain beyond its critical limit, plastic relaxation will eventually occur which causes the crystal lattice to be distorted. When this occurs, the crystalline quality of black phosphorus would be expected to degrade, as evident by the broadening of the full-width at half maximum (FWHM) for both the B_{2g} and A^2_g vibrational modes[35].

To confirm the out-diffusion of adatoms, energy-dispersive X-ray spectroscopy (EDX) measurements were performed on the annealed samples to analyze the BP/HfO₂ interface, as plotted in Fig. 7. It is worthy to note that the degree of hafnium (Hf) and oxygen (O) out-diffusion from the underlying HfO₂ gate dielectric depends strongly on the thermal budget[38,39]. When annealed at a temperature of 100 °C, the out-diffused Hf adatoms were predominantly found at the BP/HfO₂ interface which could promote the passivation of P dangling bonds [Fig. 7(a)]. However, when the thermal budget was further increased to 200 °C, a substantial amount of Hf adatoms were found to diffuse deeper into the BP channel [Fig. 7(b)]. Given the puckered honeycomb structure of BP, these out-diffused adatoms are likely to preferentially occupy the H-site in the zigzag (B_{2g} and A^2_g) direction which has been theoretically predicted for most transition metals in phosphorene[30]. This is believed to be responsible for the compressive strain observed in the BP nanosheet after a high temperature anneal. Moreover, these out-diffused adatoms could also act as impurities scattering centers which would detrimentally increase the channel resistance and degrade the carrier transport properties.

To gain a further insight into the impact of impurities scattering centers on channel resistance, the transfer length method (TLM) was employed in which the total normalized resistance ($R_{tot}W$) was plotted as a function of channel length (L) as shown in Fig. 8. Using this approach, the contact resistance can be determined by the y-intercept of the width normalized total resistance. The channel resistance can also be determined by subtracting the contact resistance from the total resistance, which is summarized in the inset of Fig. 8 as a function of thermal budget. When subjected to a thermal treatment at 100 °C, the BP structural integrity was found to remain intact, as evident by the comparable channel and contact resistances over the un-annealed case. On the contrary, a high degree of crystal lattice distortion was present in the BP film after a 200 °C thermal treatment, as supported by the Raman phonon shifts in Fig. 6. This is found to be detrimental for device performance, which
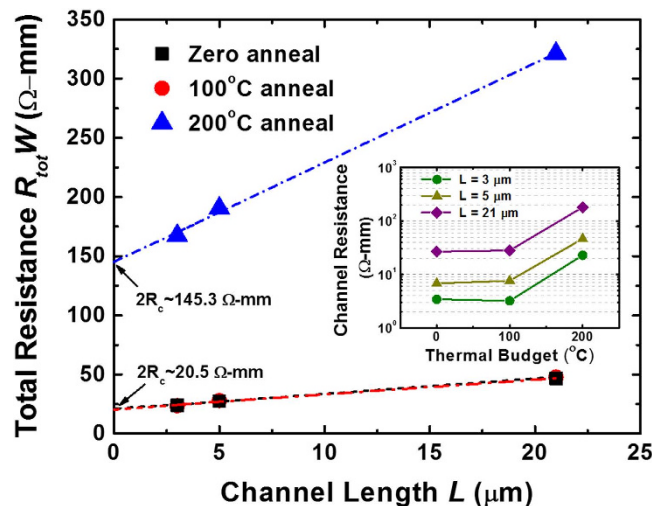
Figure 8. Using the transfer length method (TLM), the total normalized resistance ($R_{tot}W$) was plotted as a function of channel length (L). Comparable contact and channel resistance were achieved for a thermal anneal of 100 °C as compared to the un-annealed case. However, an elevated thermal treatment at 200 °C could result in a detrimental change to the BP film structure, which leads to both channel and contact resistance degradation.

is evident from the higher channel resistance by 5× as compared to the un-annealed devices. Apart from channel resistance degradation, the contact resistance has also been found to increase after a 200 °C anneal in which the $2R_c$ approaches ~145.3 Ω-mm. This is substantially higher than the contact resistance measured in devices which underwent 100 °C or no anneal, where the $2R_c$ was merely ~20.5 Ω-mm. Such a degradation is likely to be attributed to the crystal lattice distortion which causes a poorer interface quality between the metal and the BP layer. The adsorption of Hf adatoms in BP could also additionally cause an increased impurities scattering effect[37] which would compromise the carrier transport in BP transistors. This is consistent with the lower hole mobility of 120 $cm^2V^{-1}s^{-1}$ and poorer subthreshold swing SS of ~780 mV/dec discussed earlier. Hence, an optimization of the thermal treatment process is critically important to effectively engineer the interface quality between BP and HfO_2 high-k gate dielectric for enabling further performance boost.

Conclusions

In conclusion, we have experimentally demonstrated black phosphorus transistor with enhanced carrier transport through interface engineering between BP and high-k gate dielectric. A high room temperature hole mobility of ~536 $cm^2V^{-1}s^{-1}$ and a near ideal subthreshold swing of ~66 mV/dec were simultaneously achieved. Such a performance enhancement is attributed to the better interface quality between BP and HfO_2 as a result of phosphorus dangling bonds passivation by hafnium adatoms, which leads to a significant reduction in interface state density. Excessively high treatment temperature could promote the out-diffusion of hafnium adatoms into the BP channel, which distorts its crystal lattice and results in carrier transport degradation. Our study contributes to the development of BP-based transistor with enhanced performance through interface engineering.

Experimental Methods

Sample Preparation and Device Fabrication. Black phosphorus flake with a thickness of ~15 nm was micromechanically exfoliated onto p-type silicon substrate with an ultra-thin HfO_2 high-k gate dielectric of ~3.4 nm. The HfO_2 was deposited by atomic layer deposition (ALD) process. Utilizing tetrakisethylmethylamino hafnium (TEMAH) and water precursors at a deposition temperature of 250 °C, a deposition rate of ~1 Å/cycle is achieved. For every cycle of deposition, the TEMAH precursor and the water precursors are pulsed at 0.015 seconds and 0.01 seconds respectively, followed by a waiting time of 10 seconds. During the deposition, nitrogen with a flow rate of 20 sccm is utilised as the carrier gas. This was followed by a sequential cleaning in acetone followed by isopropyl alcohol before the deposition of metal electrodes using nickel (Ni) through a combination of electron beam lithography (JEOL, JBX-6300FS) and electron-beam evaporation (Oerlikon, Univex 450B). The remaining photoresist was then lifted-off to complete the device fabrication. A 30 nm silicon-dioxide passivation layer was then deposited at room temperature using electron-beam evaporation (Oerlikon, Univex 450B) over the entire BP transistor to protect the device from photo-oxidation in ambient condition[23]. Subsequently, the devices were subjected to interface thermal treatment. The anneal conditions were varied from zero to 200 °C for one minute in nitrogen (N_2) ambient to investigate the impact of thermal treatment on the structural and electrical properties of the BP transistors. Confocal Raman spectroscopy (WITec, Alpha300R) was utilized to analyze the influence of interface anneal temperature on the Raman shifts corresponding to the out-of-plane (A^1_g), and in-plane (B_{2g}, A^2_g) phonon modes[36].

References

1. Gargini, P. *The International Technology Roadmap for Semiconductors* (2015). Available at: http://www.itrs.net/. (Date of access: 01/04/2015).

2. Geim, A. K. & Novoselov, K. S. The rise of graphene. *Nat Mater* **6,** 183–191 (2007).
3. Novoselov, K. S. *et al.* A roadmap for graphene. *Nature* **490,** 192–200 (2012).
4. Wang, Q. H. *et al.* Electronics and optoelectronics of two-dimensional transition metal dichalcogenides. *Nat Nano* **7,** 699–712 (2012).
5. Liu, H., Du, Y., Deng, Y. & Ye, P. D. Semiconducting black phosphorus: synthesis, transport properties and electronic applications. *Chemical Society Reviews* **44,** 2732–2743 (2015).
6. Keyes, R. W. The Electrical Properties of Black Phosphorus. *Physical Review* **92,** 580–584 (1953).
7. Maruyama, Y., Suzuki, S., Kobayashi, K. & Tanuma, S. Synthesis and some properties of black phosphorus single crystals. *Physica B+C* **105,** 99–102 (1981).
8. Takao, Y. & Morita, A. Electronic structure of black phosphorus: Tight binding approach. *Physica B+C* **105,** 93–98 (1981).
9. Haratipour, N. & Koester, S. J. Ambipolar Black Phosphorus MOSFETs with Record n-Channel Transconductance. *IEEE Electron Device Letters* **37,** 103–106; doi: 10.1109/LED.2015.2499209 (2016).
10. Hong, T. *et al.* Polarized photocurrent response in black phosphorus field-effect transistors. *Nanoscale* **6,** 8978–8983 (2014).
11. Kamalakar, M. V., Madhushankar, B. N., Dankert, A. & Dash, S. P. Low Schottky Barrier Black Phosphorus Field-Effect Devices with Ferromagnetic Tunnel Contacts. *Small* **11,** 2209–2216 (2015).
12. Du, Y., Liu, H., Deng, Y. & Ye, P. D. Device Perspective for Black Phosphorus Field-Effect Transistors: Contact Resistance, Ambipolar Behavior, and Scaling. *ACS Nano* **8,** 10035–10042 (2014).
13. Na J. *et al.* Few-Layer Black Phosphorus Field-Effect Transistors with Reduced Current Fluctuation. *ACS Nano* **8,** 11753–11762 (2014).
14. Xia, F., Wang, H. & Jia, Y. Rediscovering black phosphorus as an anisotropic layered material for optoelectronics and electronics. *Nat Comm* **5,** 4458 (2014).
15. Koenig, S. P., Doganov, R. A., Schmidt, H., Neto, A. H. C. & Özyilmaz, B. Electric field effect in ultrathin black phosphorus. *Appl. Phys. Lett.* **104,** 103106 (2014).
16. Zhu, W. *et al.* Flexible Black Phosphorus Ambipolar Transistors, Circuits and AM Demodulator. *Nano Lett.* **15,** 1883–1890 (2015).
17. Liu, H. *et al.* Phosphorene: An Unexplored 2D Semiconductor with a High Hole Mobility. *ACS Nano* **8,** 4033–4041 (2014).
18. Chen, X. *et al.* High-quality sandwiched black phosphorus heterostructure and its quantum oscillations. *Nat Comm* **6,** 7315 (2015).
19. Liu, X. *et al. In Situ* Thermal Decomposition of Exfoliated Two-Dimensional Black Phosphorus. *The Journal of Physical Chemistry Letters* **6,** 773–778 (2015).
20. Wang, Z., Islam, A., Yang, R., Zheng, X. & Feng, P. X.-L. Environmental, thermal, and electrical susceptibility of black phosphorus field effect transistors. *Journal of Vacuum Science & Technology B* **33,** 052202 (2015).
21. Late, D. J. Temperature Dependent Phonon Shifts in Few-Layer Black Phosphorus. *ACS Applied Materials & Interfaces* **7,** 5857–5862 (2015).
22. Zhang, S. *et al.* Extraordinary Photoluminescence and Strong Temperature/Angle-Dependent Raman Responses in Few-Layer Phosphorene. *ACS Nano* **8,** 9590–9596 (2014).
23. Favron, A. Exfoliating pristine black phosphorus down to the monolayer: photo-oxidation and electronic confinement effects. arXiv:1408.0345.
24. Kim, K. K. *et al.* Synthesis and Characterization of Hexagonal Boron Nitride Film as a Dielectric Layer for Graphene Devices. *ACS Nano* **6,** 8583–8590 (2012).
25. Robertson, J. High dielectric constant oxides. *Eur. Phys. J. Appl. Phys.* **28,** 265–291 (2004).
26. Ling, Z.-P. *et al.* Black Phosphorus Transistors with Near Band Edge Contact Schottky Barrier. *Sci. Rep.* **5,** 18000 (2015).
27. Kim, J.-S. *et al.* Toward air-stable multilayer phosphorene thin-films and transistors. *Sci. Rep.* **5,** 8989 (2015).
28. Goodman, N. B., Ley, L. & Bullett, D. Valence-band structures of phosphorus allotropes. *Physical Review B* **27,** 7440 (1983).
29. Harada, Y., Murano, K., Shirotani, I., Takahashi, T. & Maruyama, Y. Electronic structure of black phosphorus studied by X-ray photoelectron spectroscopy. *Solid State Communications* **44,** 877–879 (1982).
30. Kulish, V. V., Malyi, O. I., Persson, C. & Wu, P. Adsorption of metal adatoms on single-layer phosphorene. *Physical Chemistry Chemical Physics* **17,** 992 (2015).
31. Taur, Y. & Ning, T. H. In *Fundamentals of Modern VLSI Devices* 2nd edn Ch. 3, 166 (Cambridge University Press, 2009).
32. Berger, L. I. In *Semiconductor Materials* (CRC Press, 1997).
33. Fei, R. & Yang, L. Lattice Vibrational Modes and Raman Scattering Spectra of Strained Phosphorene. *Appl. Phys. Lett.* **105,** 83120 (2014).
34. Clementi, E., Raimondi, D. L. & Reinhardt, W. P. Atomic Screening Constants from SCF Functions. II. Atoms with 37 to 86 Electrons. *The Journal of Chemical Physics* **47,** 1300–1307 (1967).
35. Ling, Z.-P. & Ang, K.-W. Thermal effects on the Raman phonon of few-layer phosphorene. *APL Materials* **3,** 126104 (2015).
36. Morita, A. Semiconducting black phosphorus. *Applied Physics A* **39,** 227–242 (1986).
37. Jena, D. & Konar, A. Enhancement of Carrier Mobility in Semiconductor Nanostructures by Dielectric Engineering. *Phys Rev Lett* **98,** 136805 (2007).
38. Cho, M. *et al.* Thermal stability of atomic-layer-deposited HfO_2 thin films on the SiNx-passivated Si substrate. *Appl. Phys. Lett.* **81,** 3630–3632 (2002).
39. Lee, B. H., Kang, L., Nieh, R., Qi W.-J. & Lee, J. C. Thermal stability and electrical characteristics of ultrathin hafnium oxide gate dielectric reoxidized with rapid thermal annealing. *Appl. Phys. Lett.* **76,** 1926–1928 (2000).
40. Wang, H. *et al.* Black Phosphorus Radio-Frequency Transistors. *Nano Lett.* **14,** 6424–6429 (2014).
41. Li, L. *et al.* Black phosphorus field-effect transistors. *Nat Nano* **9,** 372–377 (2014).

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Author Contributions

K.-W.A. conceived and supervised the project. Z.-P.L. and X.L. performed the device fabrication, characterization and X-ray photoelectron spectroscopy measurements. Raman measurements were carried out by J.-T.Z. All authors analyzed the results and wrote the manuscript together.

Additional Information

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