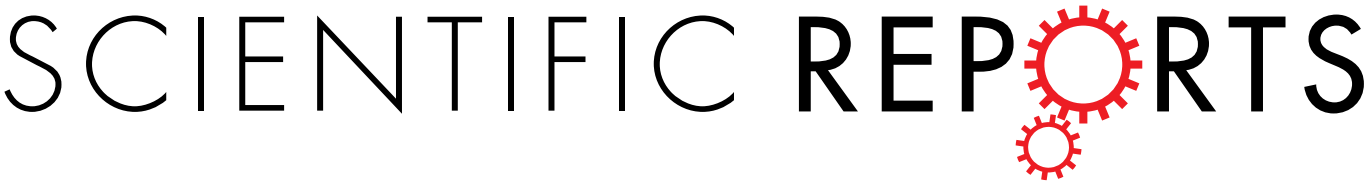

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Improved Drain Current Saturation and Voltage Gain in Graphene–on–Silicon Field Effect Transistors

Received: 19 June 2015
Accepted: 11 April 2016
Published: 04 May 2016

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Graphene devices for radio frequency (RF) applications are of great interest due to their excellent carrier mobility and saturation velocity. However, the insufficient current saturation in graphene field effect transistors (FETs) is a barrier preventing enhancements of the maximum oscillation frequency and voltage gain, both of which should be improved for RF transistors. Achieving a high output resistance is therefore a crucial step for graphene to be utilized in RF applications. In the present study, we report high output resistances and voltage gains in graphene-on-silicon (GoS) FETs. This is achieved by utilizing bare silicon as a supporting substrate without an insulating layer under the graphene. The GoSFETs exhibit a maximum output resistance of 2.5 MΩ·μm, maximum intrinsic voltage gain of 28 dB, and maximum voltage gain of 9 dB. This method opens a new route to overcome the limitations of conventional graphene-on-insulator (GoI) FETs and subsequently brings graphene electronics closer to practical usage.

The enormous interest in graphene for electronic device applications originates from its outstanding charge transport properties and atomic-scale thickness[1–3]. However, graphene devices suffer from poor on/off current ratios, which are caused by a zero band gap property. This limits their applications in logic transistors. Nevertheless, owing to graphene's exceptionally high carrier mobility and saturation velocity, it is a strong candidate for RF device applications, since RF transistors do not have to be switched off in operating conditions[1,4,5].

Intensive research activities examining graphene RF FETs thus far have mainly focused on achieving higher cut-off frequencies (f_T) with the help of gate length scaling[6]. Recently, f_T values as high as 400 GHz were reported from state-of-the-art graphene RF FETs[7–16]. However, from a circuit designer's point of view, rather than f_T, the maximum oscillation frequency (f_{max}) and intrinsic voltage gain (A_{V0}) are more important factors for RF devices[1], and very recently f_{max} values as high as 105 GHz were reported[17]. The poor f_{max} and A_{V0} values of conventional GoIFETs mainly originate from the absence of current saturation in the output characteristics due to the absence of a band gap and the Klein tunneling effect[18].

It is therefore highly desirable to obtain robust current saturation in the output characteristics from graphene FETs, which would result in a higher f_{max} and A_{V0}[19–21]. FET current saturation can be observed, either due to the decrease of carrier density in the channel near the drain side or to the velocity saturation of the carriers caused by phonon scattering[22]. For non-zero band gap semiconductors such as Si, a depletion region is formed at the drain side under $V_{GS} - V_{TH} = V_{DS}$, and the width of the depletion region extends as V_{DS} increases, where V_{GS} is the gate-to-source voltage, V_{TH} is the threshold voltage, and V_{DS} is the drain-to-source voltage. On the other hand, zero band gap materials such as graphene do not form depletion regions in the channel. Rather than forming a depletion region, a different polarity charge is generated at the drain side, and this charge extends as V_{DS} increases. This generation of other charged carriers in the channel leads to the presence of a kink-like feature in the output curve of the GoIFETs, resulting in lower output resistance (r_o) and thereby degraded RF performance. Thus, by suppressing the generation of the other charged carrier in the channel near the drain, the graphene device is able to obtain a higher r_o.

One of the methods that has been attempted to suppress the generation of the other charged carriers is the strengthening of the gate electrostatic control. In other words, the influence of the drain voltage is weakened with respect to the graphene channel near the drain side. Thus, previous attempts have focused on increasing the gate coupling by increasing the gate capacitance[19–21] and/or minimizing the residual carrier concentration (n_0)[22,23].

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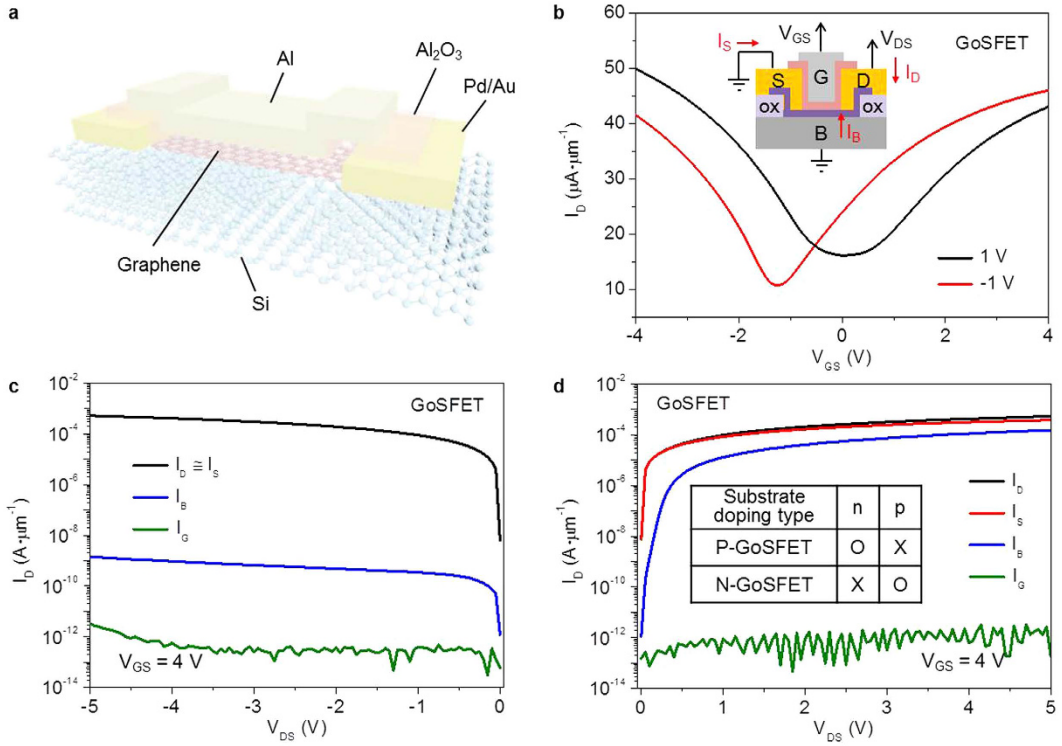

Figure 1. Graphene–on–silicon field effect transistors (GoSFETs) with W/L = 10/20 μm. (**a**) Schematic of a GoSFET with a lightly doped Si wafer acting as an insulator. The metal was patterned on top of the graphene. (**b**) Drain current (I_D) versus top gate voltage (V_{GS}) curves with positive (black) and negative (red) drain bias (V_{DS}) on an n-type substrate. Drain current (I_D), source current (I_D), gate leakage (I_G), and body current (I_B) versus drain voltage (V_{DS}) with $V_{GS} = 4$ V at the reverse bias condition of the Si substrate (negative V_{DS}) in (**c**) and at the forward bias condition of the Si substrate (positive V_{DS}) in (**d**). The table in **c** presents the proper GoSFET operating conditions depending on the substrate doping type.

Recently, hexagonal boron nitride (*h*-BN) has been adopted as a bottom gate dielectric to minimize n_0[22,23] since *h*-BN exhibits lower charged impurities and provide higher optical phonon energy than a conventional SiO_2 substrate[19,23]. The minimum n_0, which was proportional to the charged impurities, disorder, and thermal excitation, was found to significantly affect the drain conductance ($g_{ds} = \partial I_D/\partial V_{DS} = 1/r_o$)[24,25]. Despite the importance of obtaining current saturation in the output characteristics, robust current saturation has not yet been demonstrated in graphene FETs that offer highly compatible integration with current transistor processes.

In this study, we present simple but improved output characteristics by utilizing silicon instead of conventional SiO_2 or *h*-BN as a substrate. The implementation of Si as a substrate material for graphene has additional advantages over *h*-BN and other insulators in that the integration in wafer-sized scales is comparable to conventional FET technologies. Several other groups have also reported that graphene transfers onto Si surfaces, but their studies focused on the formation of a Schottky junction to modulate the current, which entails charge transport vertically from the graphene to silicon[26–28]. Moreover, their devices still suffered from poor output resistance. In contrast to previous approaches[28], in this work the charged carriers only move through the graphene layer. In other words, the current flows in a horizontal direction parallel to the silicon surface, and the carriers are confined within the graphene. The proposed device shows improved output resistance.

The typical architecture of a GoSFET is shown in Fig. 1a. The only difference between the GoSFET and conventional GoIFETs is the absence of an oxide layer under the graphene. Due to the lack of an insulating layer under the graphene in GoSFETs, the potential in the graphene is strongly affected by the charge carrier density and carrier type of the Si substrate. Figure 1b shows typical GoSFET transfer characteristics at both $V_{DS} = 1$ V and $V_{DS} = -1$ V, where lightly doped n-type silicon was used as a substrate. Excellent transfer characteristics were observed under $V_{DS} = -1$ V, where the charge in the Si was depleted at the drain side due to the reverse bias condition, as shown in the inset of Fig. 1b. Unlike the reverse bias condition at $V_{DS} = -1$ V, the performance of the GoSFET degraded under $V_{DS} = 1$ V due to the non-negligible contribution of the body current, I_B, which was caused by the forward bias condition. A further investigation of I_B, depending on the type of Si substrate, was conducted, and the results are shown in Fig. 1c,d. In Fig. 1c, I_B is 10^5 times lower than the drain current (I_D), indicating that the silicon substrate successfully acted as an insulator under the reverse bias condition. In contrast to the reverse bias condition at $V_{DS} < 0$ (Fig. 1c), the electrons in the body flowed to the graphene, and I_B became comparable to I_D under the forward bias condition at $V_{DS} > 0$ (Fig. 1d). I_B should be suppressed in the output characteristics. The doping type of the Si substrate thus should be considered depending on the operating voltage conditions to form a depletion region in the channel near the drain side, as shown in the inset of Fig. 1d.

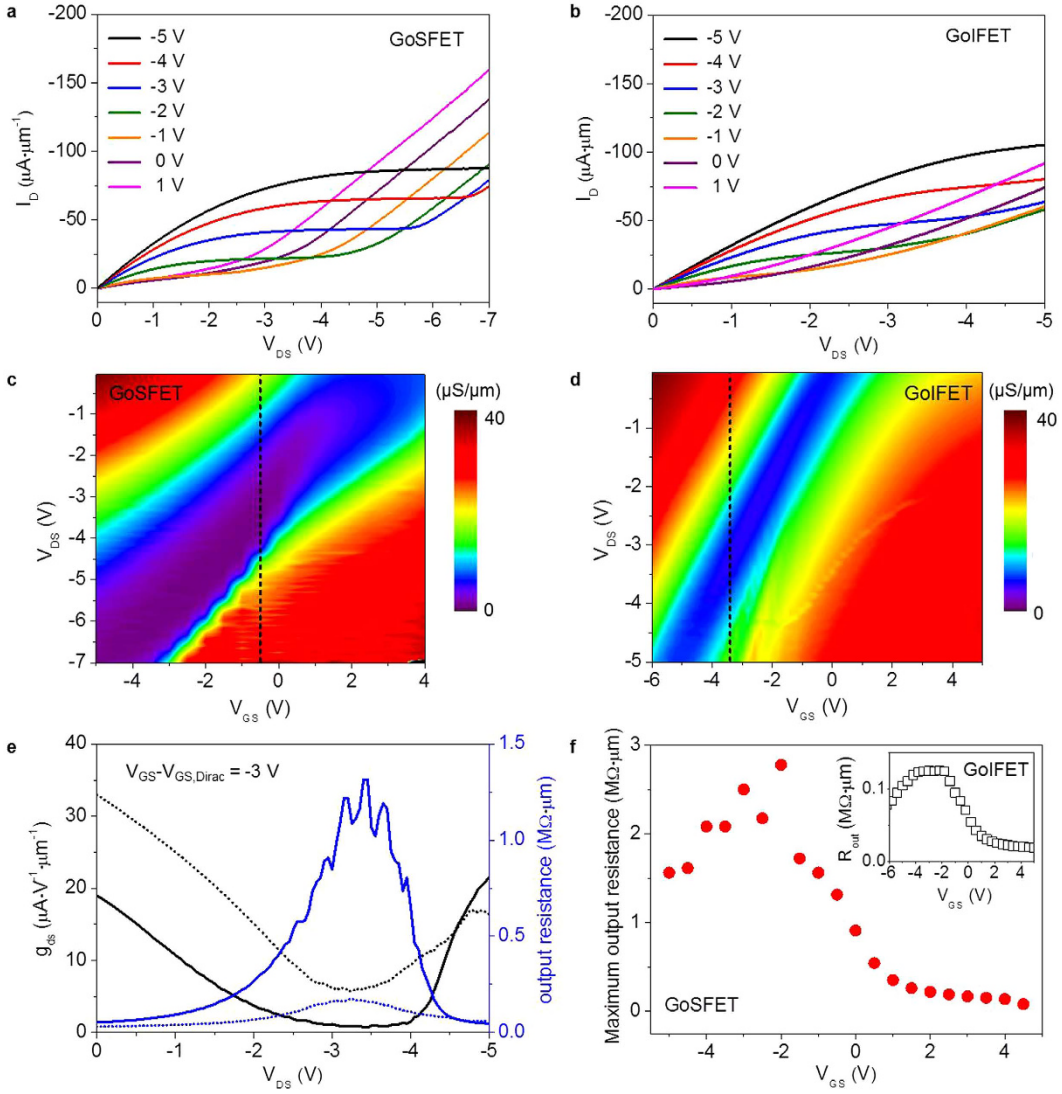

Figure 2. Output characteristics of GoSFETs and conventional GoIFETs. (**a**,**b**) The output characteristics of GoSFETs in (**a**) and GoIFETs in (**b**) at various $V_{GS} - V_{GS,Dirac}$, where $V_{GS,Daric}$ is the voltage at the minimum drain current near $V_{DS} = 0$ V. (**c**,**d**) The contour plots of the drain conductance (g_{ds}) of the GoSFETs in **c** and GoIFETs in (**d**) show that the current saturation range of the GoSFETs is wider than the GoIFET saturation range. The dashed line indicates the condition of $V_{GS} - V_{GS,Dirac} = -3$ V. (**e**) Comparison of the g_{ds} of the GoSFETs (solid line) and GoIFETs (dotted line) at $V_{GS} = -0.5$ V and $V_{GS,Dirac} = -2.5$ V, directly showing the robust output characteristic of the GoSFET over those of the graphene FET. (**f**) The maximum output resistance (r_o) of the GoSFETs and GoIFETs as a function of V_{GS}, indicating that a higher r_o is obtained from the GoSFETs than from the GFETs.

Figure 2a shows typical GoSFET output characteristics, revealing improved current saturation in a wide drain voltage range. Unlike the improved current saturation in the GoSFETs, current saturation in a narrow drain voltage range was observed in the output characteristics of the conventional GoIFETs in Fig. 2b, which is typical in graphene FETs. The contour plots of g_{ds} in Fig. 2c,d clearly show that the current saturation of the GoSFETs is much more robust than that of the conventional GoIFETs. The improved drain current saturation in the GoSFETs results in a lower g_{ds} and higher output resistance, as shown in Fig. 2e. The maximum r_o at a given V_{GS} is plotted in Fig. 2f, showing that a r_o value as high as 2.5 MΩ·μm was obtained from the GoSFETs, in contrast to the r_o value of 0.12 MΩ·μm obtained from the GoIFETs. This improved GoSFET drain current saturation is mainly attributed to the suppression of electron carrier generation as the drain voltage increases, which is described in Fig. 3b,c. The potential energy of the drain is coupled with the energy level of the Si substrate. Thus, the positive fixed charge is generated in the depletion region near the drain side. This additional potential from the Si substrate allows a higher graphene energy level and thus the graphene is able to maintain its p-type behavior even at higher drain voltages. On the other hand, in the GoIFETs, other polarity carriers are generated near the drain side at higher drain voltages, which causes the kink effect in the GoIFETs, as shown in Fig. 3a–c. It is worth noting that the current takeoff at high drain voltage in the GoSFET is steeper than that in the GoIFET. The surface potential at

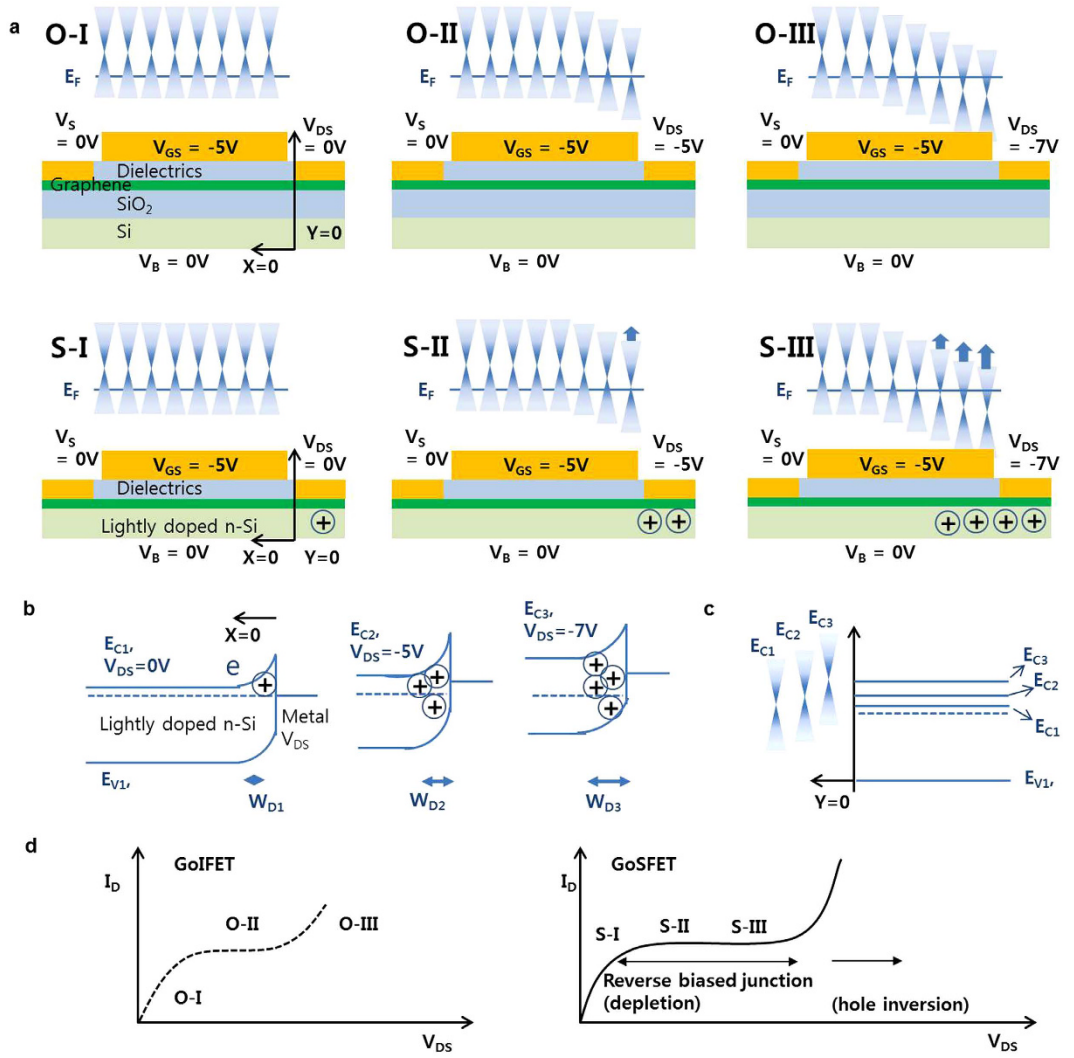

Figure 3. Conventional kink effect in a GoIFET and improved current saturation in a GoSFET. (**a**) A schematic demonstration of the energy band diagram of the graphene in both a GoIFET and GoSFET. The generation of an electron in the channel near the drain side under high drain voltage leads to a kink effect in the output characteristics of the GoIFET, while the fixed charge in the depletion region of the GoSFET allows the energy band diagram of the graphene to pull up so that the graphene is able to maintain its p-type behavior. (**b**,**c**) The pulling-up mechanism of the graphene energy band diagram, which is caused by the Si energy band in the GoSFET. (**d**) The measured output characteristics of the GoIFET and GoSFET, respectively. The sudden takeoff of the current in the GoSFET is steeper than that of the GoIFET because the current takeoff in the GoSFET is attributed to the body current (the depletion region disappears and the hole is inverted) rather than simply being due to the generation of the other carrier, as occurs with the GoIFETs.

the onset of the strong inversion in the Si at high drain voltage leads to a hole inversion layer, generating a mobile carrier charge and eventually contributing to the drain current, as shown in Fig. 3d.

The cumulative results of the maximum r_o in Fig. 4a clearly show that, in terms of the RF characteristics, the GoSFETs outperformed the conventional GoIFETs due to the higher r_o. We further investigated the correlation between the maximum r_o and several device parameters, including the residual carrier concentration, n_0, contact resistance, R_C, and FET carrier mobility, μ, as shown in Fig. 4b–d. Their values were extracted from the fitting using the model (Equation (1) in the supplementary information) for both the GoSFETs and GoIFETs[29]. It was found that both n_0 and R_C were inversely proportional to the maximum r_o in logarithmic scale, especially for the GoSFETs, as shown in Fig. 4b,c. The robust current saturation required strong gate coupling, which could be obtained at low parasitic capacitance, i.e., a low n_0[17,24]. Generally, low GoSFET values are attributed to the non-polar property of the silicon surface, which suppresses residual impurities between the graphene and the silicon surface. Unlike on the silicon surface, charged residues can easily attach to the SiO_2 surface (polar behavior), which results in the doping of the graphene and degradation of the graphene devices[30]. The residual charges on the SiO_2 were reported to be around $2 \sim 5 \times 10^{11}\,cm^{-2}$, while those on the silicon surface were around $0.3 \sim 2.8 \times 10^{10}\,cm^{-2}$[31,32], which were also verified by the Raman analysis as shown in the supplementary (Fig. S2).

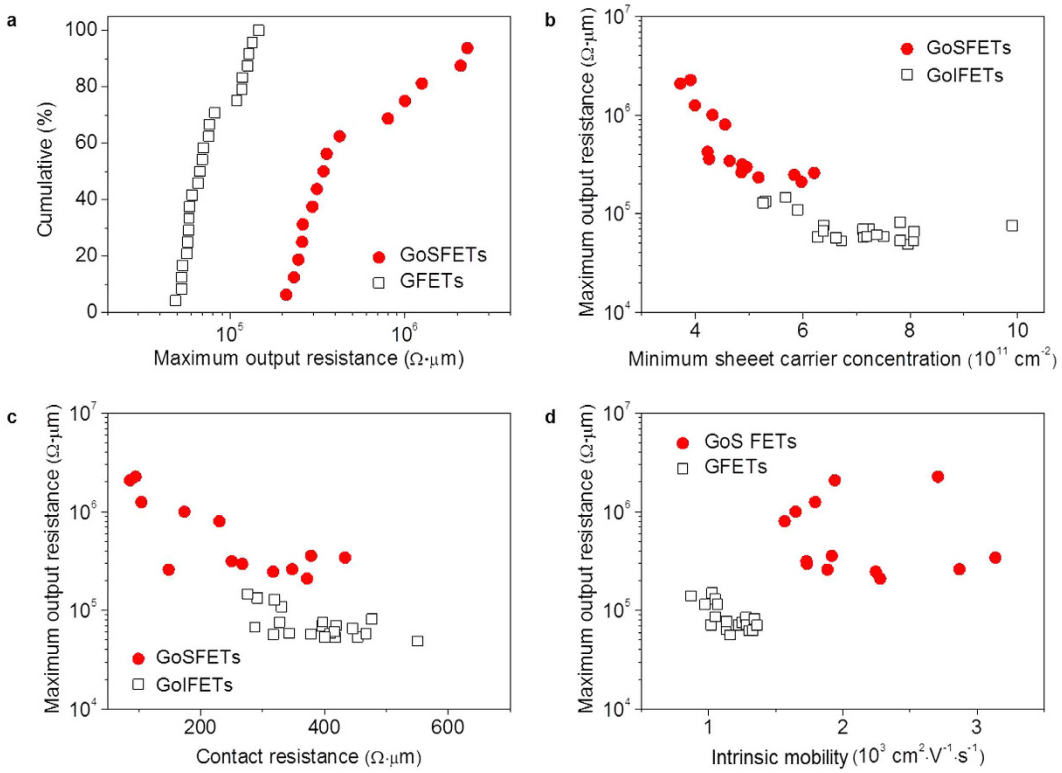

Figure 4. Comparison of GoSFET and GFET output characteristics. (**a**) Cumulative results of the maximum output resistance (r_o), of the GFETs (black open squares) and GoSFETs (red filled circles). (**b**) Maximum r_o as a function of the minimum sheet carrier concentration (n_0) of the GoSFETs and GoIFETs. (**c**) Maximum r_o, as a function of the contact resistance (R_C) of the GoSFETs and GoIFETs. The inset shows a schematic drawing of the potential profile of the graphene at the contact edge. (**d**) Maximum r_o as a function of the external mobility of the GoSFETs and GoIFETs.

The experimental results indicated that there are more residual charges on graphene/SiO_2 than graphene/Si interfaces.

The suppression capabilities that prevent the generation of the other polarity carrier in the channel near the drain are directly affected by the electron potential energy in the Si, which is influenced by the metal/graphene voltage drop. Therefore, it is expected that the maximum r_o is inversely proportional to R_C for the GoSFETs, while r_o exists irrespective of R_C for the GoIFET. The lower contact resistance in the GoSFETs compared to that of the GoIFETs is attributed to the presence of additional charge injection into the graphene from the Si bottom substrate, in addition to the metal pad. Both Pd and Si atoms are able to inter-diffuse through the defects in the graphene, such as carbon atom vacancies, thereby form a conductive Pd silicide (Fig. S1) in the Si substrate[33], which is the source of the additional charge injection into the graphene. The lower contact resistance of the graphene devices is inter-correlated with the higher FET mobility in the GoSFETs. Finally, a weak correlation between the maximum r_o and μ can be observed in Fig. 3d. Nevertheless, it is evident that the FET mobility of GoSFETs is higher than that of GoIFETs due to the higher phonon energy of Si (63 meV) compared to that of SiO_2 (50 meV)[34,35].

Figure 5a shows that the maximum r_o was proportional to the maximum A_{V0}, and that a maximum A_{V0} as high as 28 dB was achieved from the GoSFETs, which is comparable to that of Si-based RF FETs. In order to verify the performance of the voltage amplifier, a common-source voltage amplifier was implemented with a P-GoSFET, as shown in Fig. 5b. The voltage amplifier showed excellent voltage amplification behavior, as presented in Fig. 5c. A maximum A_V as high as 9 dB was obtained at a load resistance (R_D) of 50 kΩ (Fig. 5d).

In summary, the utilization of a silicon substrate in graphene FETs without an insulating layer leads to robust current saturation under wide-ranging and exceptionally high output resistance. In addition, the proposed GoSFETs show excellent process compatibility with conventional FET processes. This method potentially can enable the implementation of graphene in RF device applications.

Methods

Device fabrication. The graphene used in this work was synthesized using the inductive coupling plasma chemical vapor deposition method on a thin copper film, and it was transferred using the typical wet transfer method with PMMA. For the conventional GoIFETs, the graphene was transferred onto thermally grown SiO_2 (100 nm) on a heavily doped p-type silicon wafer (resistivity of ~0.01–0.05 Ω·cm). For the GoSFETs, the thermal oxide (50 nm) in the active region on lightly doped n- or p-type silicon (resistivity of ~1–5 Ω·cm) was patterned

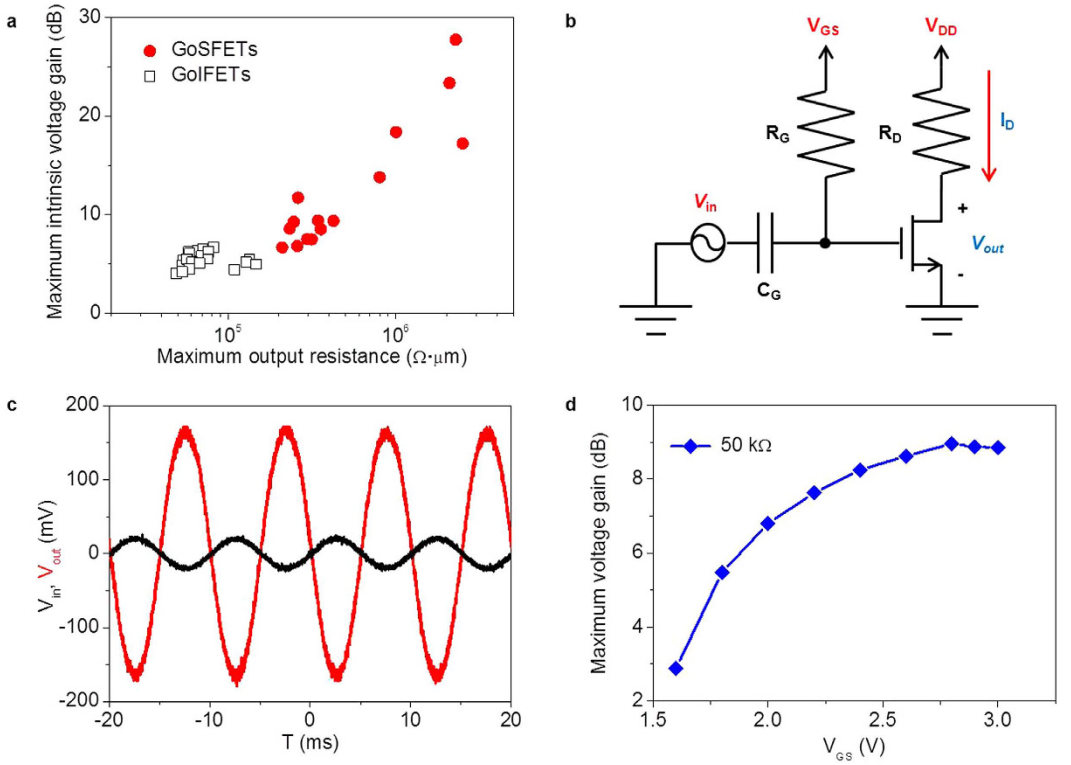

Figure 5. (**a**) Maximum intrinsic voltage gain (A_{V0}) as a function of the maximum output resistance (r_o) of the GoSFETs and GoIFETs. (**b**) A common source voltage amplifier schematic. One of the GoSFETs exhibiting a maximum intrinsic voltage gain of ~9.4 dB is applied to the circuit in order to measure the voltage gain (A_V). The output voltage signal is obtained between the drain and ground. (**c**) Input (V_{in}, black) and output (V_{out}, red) signals measured using an oscilloscope. (**d**) A maximum A_V as a function of gate voltages at a load resistance (R_D) of 50 kΩ.

using a buffered oxide etchant, and the graphene was transferred immediately after the removal of the photoresist and the native oxide. The subsequent processes were identical for both the GoSFETs and GoIFETs. After patterning the channel graphene, the source and drain were defined using a Pd (5 nm)/Au (50 nm) lift-off process. Next, 20 nm of Al_2O_3 was deposited by atomic layer deposition (ALD) process on the graphene surface. Prior to the ALD process, 0.5 nm aluminum layer was evaporated on the graphene surface as a nucleation layer. The ultrathin aluminum nucleation layer is soon oxidized during the ALD process. The 150 nm Al gate metal was formed using a thermal evaporator and the lift-off process. Finally, the device went through a thermal budget of 300 °C for 12 hrs.

Electrical measurement. All of the devices were measured at room temperature in ambient air with a B1500 parameter analyzer. In order to implement a common source voltage amplifier with a graphene–on–silicon transistor, the external resistances ($R_G = 1$ MΩ, $R_D = 10, 30, 50$ kΩ) and capacitor ($C_G = 1$ μF) set on a breadboard, as well as a DC supplier and function generator, were connected. The transistors were staged in a probe station and connected to the circuit with a biaxial cable. The input signal was sinusoidal with an amplitude of 20 mV and a frequency of 1 kHz.

References

1. Schwierz, F. Graphene transistors: status, prospects, and problems. *Proceedings of the IEEE* **101,** 1567–1584 (2013).
2. Bolotin, K. I. *et al.* Ultrahigh electron mobility in suspended graphene. *Solid State Communications* **146,** 351–355 (2008).
3. Schwierz, F. Graphene transistors. *Nat Nanotechnol* **5,** 487–496 (2010).
4. Banerjee, S. K. *et al.* Graphene for CMOS and beyond CMOS applications. *Proceedings of the IEEE* **98,** 2032–2046 (2010).
5. Novoselov, K. *et al.* A roadmap for graphene. *Nature* **490,** 192–200 (2012).
6. Meric, I. *et al.* Channel length scaling in graphene field-effect transistors studied with pulsed current– voltage measurements. *Nano letters* **11,** 1093–1097 (2011).
7. Meric, I., Baklitskaya, N., Kim, P. & Shepard, K. L. RF performance of top-gated, zero-bandgap graphene field-effect, Electron Devices Meeting (IEDM), 2008 IEEE International, San Francisco, CA, USA. doi: 10.1109/IEDM.2008.4796738 (2008, Dec. 15–17).
8. Wu, Y. *et al.* High-frequency, scaled graphene transistors on diamond-like carbon. *Nature* **472,** 74–78 (2011).
9. Badmaev, A., Che, Y. C., Li, Z., Wang, C. & Zhou, C. W. Self-Aligned Fabrication of Graphene RF Transistors with T-Shaped Gate. *Acs Nano* **6,** 3371–3376 (2012).
10. Pince, E. & Kocabas, C. Investigation of high frequency performance limit of graphene field effect transistors. *Appl. Phys. Lett.* **97,** 173106 (2010).
11. Dimitrakopoulos, C. *et al.* Wafer-scale epitaxial graphene growth on the Si-face of hexagonal SiC (0001) for high frequency transistors. *J Vac Sci Technol B* **28,** 985–992 (2010).
12. Lin, Y. M. *et al.* Operation of Graphene Transistors at Gigahertz Frequencies. *Nano letters* **9,** 422–426 (2009).

13. Lin, Y. M. *et al.* 100-GHz Transistors from Wafer-Scale Epitaxial Graphene. *Science* **327,** 662–662 (2010).
14. Liao, L. *et al.* High-speed graphene transistors with a self-aligned nanowire gate. *Nature* **467,** 305–308 (2010).
15. Wu, Y. Q. *et al.* State-of-the-Art Graphene High-Frequency Electronics. *Nano letters* **12,** 3062–3067 (2012).
16. Cheng, R. *et al.* High-frequency self-aligned graphene transistors with transferred gate stacks. *P Natl Acad Sci USA* **109,** 11588–11592 (2012).
17. Feng, Z. H. *et al.* An ultra clean self-aligned process for high maximum oscillation frequency graphene transistors. *Carbon* **75,** 249–254 (2014).
18. Meric, I. *et al.* Current saturation in zero-bandgap, top-gated graphene field-effect transistors. *Nat Nanotechnol* **3,** 654–659 (2008).
19. Meric, I. *et al.* Graphene field-effect transistors based on boron–nitride dielectrics. *Proceedings of the IEEE* **101,** 1609–1619 (2013),
20. Han, S.-J. *et al.* High-frequency graphene voltage amplifier. *Nano letters* **11,** 3690–3693 (2011).
21. Han, S.-J., Reddy, D., Carpenter, G. D., Franklin, A. D. & Jenkins, K. A. Current saturation in submicrometer graphene transistors with thin gate dielectric: Experiment, simulation, and theory. *ACS nano* **6,** 5220–5226 (2012).
22. Szafranek, B., Fiori, G., Schall, D., Neumaier, D. & Kurz, H. Current saturation and voltage gain in bilayer graphene field effect transistors. *Nano letters* **12,** 1324–1328 (2012).
23. Meric, I. *et al.* Graphene field-effect transistors based on boron nitride gate dielectrics, Electron Devices Meeting (IEDM), 2010 IEEE International, 23.2.1–23.2.4, San Francisco, CA, USA. doi: 10.1109/IEDM.2010.5703419 (2010, Dec. 6–8).
24. Wu, Y. *et al.* Three-terminal graphene negative differential resistance devices. *ACS nano* **6,** 2610–2616 (2012).
25. Adam, S., Hwang, E. H., Galitski, V. M. & Das Sarma, S. A self-consistent theory for graphene transport. *P. Natl. Acad. Sci. USA* **104,** 18392–18397 (2007).
26. Li, X. M. *et al.* Graphene-On-Silicon Schottky Junction Solar Cells. *Adv Mater* **22,** 2743 (2010).
27. Yang, H. *et al.* Graphene Barristor, a Triode Device with a Gate-Controlled Schottky Barrier. *Science* **336,** 1140–1143 (2012).
28. Bartolomeo, A. D. Graphene Schottky diodes: An experimental review of the rectifying graphene/semiconductor heterojunction. *Physics Reports* **606,** 1–58 (2015).
29. Kim, S. *et al.* Realization of a high mobility dual-gated graphene field-effect transistor with Al_2O_3 dielectric. *Appl. Phys. Lett.* **94,** 062107 (2009).
30. Lafkioti, M. *et al.* Graphene on a hydrophobic substrate: doping reduction and hysteresis suppression under ambient conditions. *Nano letters* **10,** 1149 (2010).
31. Deshpande, A., Bao, W., Milao, F., Lau, C. N. & LeRoy, B. J. Spatially resolved spectroscopy of monolayer graphene on SiO_2. *Phys. Rev. B* **79,** 205411 (2009).
32. Dorgan, V. E., Bae, M.-H. & Pop, E. Mobility and Saturation Velocity in Graphene on SiO_2. *Appl. Phys. Lett.* **97,** 082112 (2010).
33. Suryana, R., Nakatsuka, O. & Zaima, S. Formation of palladium silicide thin layers on Si(100) substrates. *Jap. J. Appl. Phys.* **50,** 05EA09 (2011).
34. Wu, Y. *et al.* State-of-the-Art graphene high-frequency electronics. *Nano Letters* **12,** 3062 (2012).
35. Fischetti, M. V., Neumayer, D. A. & Cartier, E. A. Effective electron mobility in Si inversion layers in metal–oxide–semiconductor systems with a high-κ insulator: The role of remote phonon scattering *J. Appl. Phys.* **90,** 4587 (2001).

Acknowledgements

This work was supported by research grants from the National Research Foundation (NRF) of Korea (2010-0029132 and 2011-0031638).

Author Contributions

S.M.S. and B.J.C. designed the experiments; S.M.S. and B.J.H. performed the device fabrication and characterization. S.M.S., B.J.H., W.S.H. and B.J.C. analyzed the data and wrote the manuscript. All authors discussed the results and commented on the manuscript.

Additional Information

Supplementary information accompanies this paper at http://www.nature.com/srep

Competing financial interests: The authors declare no competing financial interests.

How to cite this article: Song, S. M. *et al.* Improved Drain Current Saturation and Voltage Gain in Graphene–on–Silicon Field Effect Transistors. *Sci. Rep.* **6**, 25392; doi: 10.1038/srep25392 (2016).

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Corrigendum: Improved Drain Current Saturation and Voltage Gain in Graphene–on–Silicon Field Effect Transistors

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Scientific Reports **6**:25392; doi: 10.1038/srep25392; published online 04 May 2016; updated 27 June 2016

This Article contains errors in the Acknowledgements section.

"This work was supported by research grants from the National Research Foundation (NRF) of Korea (2010-0029132 and 2011-0031638)."

should read:

"This work was supported by the Center for Advanced Soft-Electronics funded by the Ministry of Science, ICT and Future Planning as Global Frontier Project (CASE-2011-0031638)."