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Investigation and Manipulation of Different Analog Behaviors of Memristor as Electronic Synapse for Neuromorphic Applications

Changhong Wang*, Wei He*, Yi Tong & Rong Zhao

Low-power and high-density electronic synapse is an important building block of brain-inspired systems. The recent advancement in memristor has provided an opportunity to advance electronic synapse design. However, a guideline on designing and manipulating the memristor's analog behaviors is still lacking. In this work, we reveal that compliance current ($I_{\rm comp}$) of electroforming process played an important role in realizing a stable analog behavior, which is attributed to the generation of conical-type conductive filament. A proper $I_{\rm comp}$ could result in a large conductance window, good stability, and low voltage analog switching. We further reveal that different pulse conditions can lead to three analog behaviors, where the conductance changes in monotonic increase, plateau after initial jump, and impulse-like shape, respectively. These behaviors could benefit the design of electronic synapse with enriched learning capabilities. This work will provide a useful guideline for designing and manipulating memristor as electronic synapses for brain-inspired systems.

Developing brain-inspired computer has been an ultimate goal for scientists to pursue for decades^{1,2}. It is widely accepted that synapses are responsible for the massive parallelism and structural plasticity in neurobiology, and crucial to biological computations that underlie perception and learning^{3,4}. Therefore, electronic synaptic devices that could display the functionalities of neural synapse such as plasticity and learning are the most important building blocks of brain-inspired computer and neuromorphic systems. Electronic synapse traditionally is designed based on complementary metal-oxide-semiconductor (CMOS) technology, which is impossible to be scaled up due to high power consumption and low density, let alone reach the human brain's level at 100 trillion of synapses^{4,5}. The recent advancement in memristor has provided a promising opportunity to advance the electronic synapse design, which is attributed to the unique properties of memristor including analog behavior, plasticity, non-volatile, nanoscale size, and low power⁶⁻¹⁰. This has sparked a new wave of enthusiasm in developing brain-inspired computer and neuromorphic systems. To achieve this goal, one of the keys is to develop a memristor with robust and low power analog behaviors and learning capabilities, which can be scaled up to an ultra large system. Even though many memristive devices have been demonstrated by using different materials (e.g. metal oxides like SiO_2 , WO_x , InGaZnO, chalcogenides like Cu_2S , Ag_2S , and phase change materials like $Ge_2Sb_2Te_5$) $^{11-18}$, they are mostly developed in an exploration way. A guideline on designing and manipulating the memristor's analog behaviors, which is much crucial and necessary for the synapse and neuromorphic engineering, is still lacking yet. Furthermore, because the biological learning rules are diverse in nature, memristor displaying different analog behaviors is greatly needed to enhance the learning capabilities of electronic synapse.

In this work, we investigate the effect of compliance current ($I_{\rm comp}$) of electroforming process on forming the analog resistive switching of memristor using iron oxide (FeO_x) based memristor. FeO_x was selected as the active layer due to the good repeatability and consistency of the devices⁴. It is found that $I_{\rm comp}$ dramatically affects the analog resistive switching of memristor in terms of conductance window, operational voltage, and stability. A conductive filament model is proposed to explain the observed analog behaviors, and the conduction mechanism of FeO_x based memristor is also discussed. Moreover, the analog behaviors are found to be further affected by pulse conditions. Three kinds of analog behaviors with different conductance changing trends (i.e. monotonic

Engineering Product Development Singapore University of Technology and Design 8 Somapah Road, Singapore 487372. *These authors contributed equally to this work. Correspondence and requests for materials should be addressed to Y.T. (email: yi_tong@sutd.edu.sq) or R.Z. (email: zhao_rong@sutd.edu.sq)

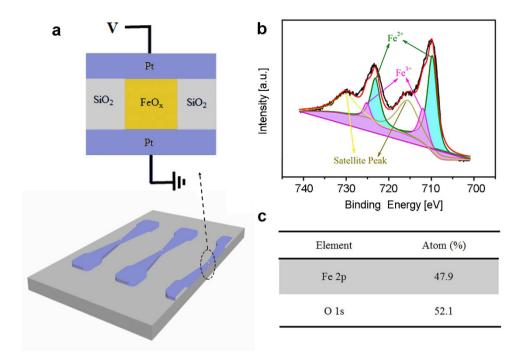


Figure 1. Device Characterizations. (a) Schematic illustration of the FeO_x based memristor devices on silicon wafer (bottom) with the cross-sectional view of the structure and the testing configuration (upper). (b) X-ray photoelectron spectroscopy (XPS) spectrum for FeO_x thin film, and (c) The atomic ratio of FeO_x film detected by XPS.

increase, plateau after initial jump, and impulse-like change) are observed, which can be utilized to enrich the learning capabilities of electronic synapse. These findings could provide a useful guideline for designing memristor devices as electronic synapses with comprehensive learning capabilities for brain-inspired computing systems.

Results and Discussion

The FeO_x based memristor was fabricated on silicon wafers with 1 μ m thick SiO₂ layer on top. A schematic drawing of the cross-sectional view and top view of the device structure is shown in Fig. 1(a). A layer of 30 nm FeO_x film was deposited by radio frequency (RF) magnetic sputtering, which was sandwiched by two inert platinum (Pt) electrodes to form a Pt/FeO_x/Pt structure. The details can be found in the section of experimental method. X-ray photoelectron spectroscopy (XPS) measurement was performed to analyze the chemical composition of the as-deposited FeO_x film (Fig. 1(b)). The peaks at 709.77 eV and 723.02 eV correspond to Fe²⁺ 2p_{3/2} and Fe²⁺ 2p_{1/2}, respectively. The peaks at 712.40 eV and 725.05 eV correspond to Fe³⁺ 2p_{3/2} and Fe³⁺ 2p_{1/2}, respectively. The peaks at 715.33 eV and 729.89 eV represent two satellite peaks^{4,19,20}. Since the relative peak intensity of Fe²⁺ is larger than that of Fe³⁺, the deposited FeO_x layer is mainly composited of Fe²⁺, which is consistent with the atomic ratio of Fe and O in the FeO_x film (Fe:O = 1:1.09) as shown in Fig. 1(c). The X-ray diffraction patterns shown in Fig. S1 further confirm that the as-deposited FeO_x film is at amorphous state²¹.

To study the electroforming process, $I_{\rm comp}$ with different values was applied to form the pristine FeO_x based memristors. All the memristor devices were at the low conductance state ($\sim 10^{-7}$ mS) initially. Figure 2(a–c) show the electroforming profile with $I_{\rm comp}$ of 0.1 mA, 0.5 mA, and 1 mA, respectively. After electroforming process, it can be seen that the conductance of the memristor was increased to ~ 10 mS, ~ 70 mS, and ~ 225 mS, for $I_{\rm comp}$ of 0.1, 0.5, and 1.0 mA, respectively. The reset process was conducted subsequently using direct current (DC) sweeping for devices under various $I_{\rm comp}$. As shown in Fig. 2(d–f), the conductance of all devices gradually decreases while increasing the stopping voltage of negative sweep. After that, set process was subsequently conducted as shown in Fig. 2(g–i). It is observed that the conductance of the devices increases with the increase of the stopping voltage of positive sweep.

After electroforming with three different $I_{\rm comp}$, the analog behaviors of memristor were investigated and compared. For small $I_{\rm comp}$ with a value of 0.1 mA, after electroforming, the subsequent reset/set process was able to occur at small stopping voltage (i.e. $-1.20\,\rm V$ and $1.70\,\rm V$) with small conduction current (i.e. $-0.010\,\rm mA$ and 0.014 mA) as shown in Fig. 2(d,g). In addition, it is noticed that there are some fluctuations and overlaps between each pinched-hysteresis I-V loop, this suggests that the conductive filament (CF) formed by the electroforming process with a small $I_{\rm comp}$ of 0.1 mA is unstable and the self-degradation of CF occurs which contributes to the overlaps of pinched-hysteresis I-V loop. After electroforming by the increased $I_{\rm comp}$ of 0.5 mA (Fig. 2(b)), the subsequent reset/set current increased to $-0.5\,\rm mA$ and 0.4 mA (Fig. 2(e,h)), respectively. Comparing to the analog behavior of small $I_{\rm comp}$ of 0.1 mA, there is no fluctuation observed between each I-V loop, indicating a strong CF formed by an increased $I_{\rm comp}$ of 0.5 mA. The slightly smaller set voltage in Fig. 2(h) compared to that in Fig. 2(g) may be due to different dynamics of the CF induced by different amount of oxygen vacancies $I_{\rm comp}$ of 0.5 mX, when

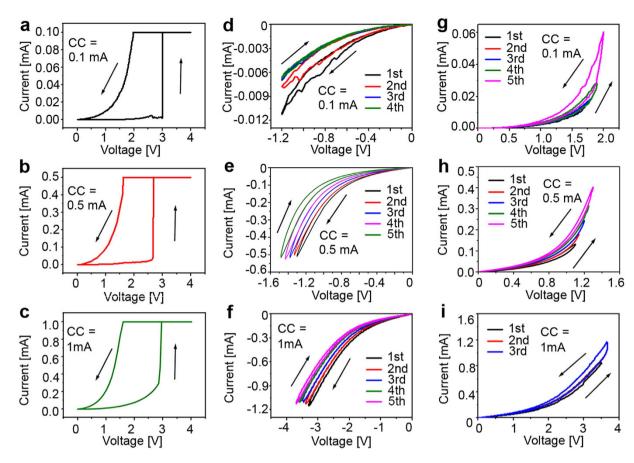


Figure 2. Electroforming process with different compliance current (I_{comp}) and its consequent analog behaviors. For I_{comp} of 0.1 mA, (a) electroforming profile, (d) and (g) the analog I-V curves under negative and positive sweep voltage, respectively. For I_{comp} of 0.5 mA, (b) electroforming profile, (e) and (h) the analog I-V curves under negative and positive sweep voltage, respectively. For I_{comp} of 1 mA, (c) electroforming profile, (f) and (i) the analog I-V curves under negative and positive sweep voltage, respectively.

we further increased $I_{\rm comp}$ to a large value of 1.0 mA, the conductance of memristor kept increasing to 225 mS as shown in Fig. 2(c). The corresponding reset/set process only occurred at very large stopping voltage (i.e. -3.5 V and 3.5 V) with large conduction current (i.e. -1.1 mA and 0.9 mA) as shown in Fig. 2(f,i). Based on the above observations, a clear trend is observed that larger $I_{\rm comp}$ causes stronger and more stable CF during the operation of FeO_x based memristor. Moreover, we calculated the conductance change ΔG which is defined as $G_{\rm int} - G_{\rm fin}$, where $G_{\rm int}$ is the initial conductance, and $G_{\rm fin}$ is the final conductance after the voltage sweeping. It can be noted that the largest ΔG is achieved for moderate $I_{\rm comp}$ of 0.5 mA. Therefore, a proper $I_{\rm comp}$ in electroforming process is critically needed for achieving good analog performance of memristors.

Nowadays, it is widely accepted that the initial electroforming process is related to the generation of defects (e.g. oxygen vacancies) within the transition oxides, which are responsible for constructing CF within the oxides during the electroforming process^{23–27}. Our findings disclose that the I_{comp} of the electroforming process would significantly affect the formation of CF and its dynamics, which consequently determine the following analog behavior. When I_{comp} is small, the formed CF is most likely in a pyramidal shape, as illustrated in Fig. 3(a). It is narrow due to less oxygen vacancies for constructing CF under small compliance current, which is the possible reason for the overlap and fluctuation in the *I-V* loops in Fig. 2(d,g). Normally, resistive switching (RS) occurs at the tip of CF because oxygen vacancies are easily driven by electric field and joule heating at this location²⁸. When I_{comp} increases, more oxygen vacancies are generated such that a conical CF could be formed as shown in Fig. 3(b). Comparing to the case of small I_{comp} , the size of CF should increase in both length and width, resulting in no overlap in the I-V loops in Fig. 2(e,h). The increase of size of CF has been investigated by theoretical simulation and confirmed by in-situ transmission electron microscopy (TEM) observation^{27,29,30}. The rupture and combination of conical filament, which is the most common type of CF in memristors, normally occurs at the top of the conical filament, leading to a favorable memory window^{8,27,29,31–34}. When a very large I_{comp} is applied to memristor, the filament will further broaden and lengthen, resulting in a high conductance which is consistent with the electrical results extracted from Fig. 2(c). The filament may become a cylinder shape as shown in Fig. 3(c). This kind of cylindrical filament tends to display digital switching but not analog switching^{26,35}. RS in this case often occurs at the middle of the cylindrical filament, which is caused by the higher temperature at that location due to the metal electrodes possesses high thermal conductivity^{28,31,36,37}. It is worthwhile to note that the above models are solely hypotheses. However, these hypotheses are based on the reported results of resistive memory (ReRAM)

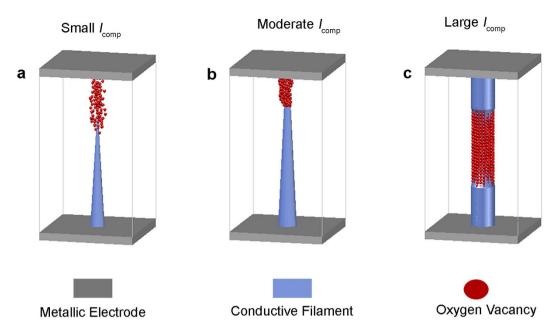


Figure 3. Conductive Filaments (CFs) generated by different I_{comp} . (a) The pyramidal CF formed by the small I_{comp} . (b) The conical CF formed by the moderate I_{comp} . (c) The cylindrical CF formed by the large I_{comp} .

as the memristor and ReRAM may share the similar switching mechanism³⁸. We will continue to investigate the real time filament formation process using advanced microscopy system in the future. In summary, the findings reported in this work unveil a strong dependence of $I_{\rm comp}$ for the electroforming process and the subsequent analog switching behavior, which will provide a useful guideline for engineering of memristor and neuromorphic systems.

To investigate the dynamic properties of different CFs, the conductance of memristor after electroforming was continuously read using a bias of 0.1 V for 100 cycles as shown in Fig. 4. Firstly, it is found that the conductance decayed sharply from the initial state and gradually saturates after electroforming by $I_{\rm comp}$ of 0.1 mA, indicating an unstable CF. The decay of conductance becomes moderate and is negligible for $I_{\rm comp}$ of 0.5 and 1.0 mA, respectively. After 100 cycles, the conductance reduces to 60%, 95%, and 99.5% of the original value for $I_{\rm comp}$ of 0.1, 0.5, and 1.0 mA. In addition, it is noticed that the initial spontaneous decay of the conductance is gradually inhibited by increasing $I_{\rm comp}$. It can be concluded that the stability of the CF formed in the electroforming process is able to be controlled by setting $I_{\rm comp}$ properly. Small $I_{\rm comp}$ would generate relatively less oxygen vacancies and construct pyramidal CF (inset in Fig. 4(a)) with poor data stability, while moderate $I_{\rm comp}$ would generate appropriate oxygen vacancies to construct a conical CF (inset in Fig. 4(b)) with improved data stability. However, the memristor will lose analog behavior if the $I_{\rm comp}$ is too large (inset in Fig. 4(c)) due to the formation of a strong cylindrical CF, which is not easily ruptured by joule heating. Therefore, a trade-off exists between the analog behavior and data stability of memristors.

To further investigate the charge transportation in FeO_x based memristors, I-V curves were obtained from the device formed by the moderate $I_{\rm comp}$ of 0.5 mA. Figure 5(a) displays the I-V curve of set process replotted in a dual logarithmic graph. The linear fitting of the curve at the low voltage range (0 ~ 0.10 V) has a slope of 1, indicating that ohmic conduction dominates at low electric field. The equation for ohmic conduction can be expressed as,

$$J = qN_c \mu E \exp\left(\frac{-\Delta E_{ac}}{kT}\right) \tag{1}$$

where, q is the electronic charge, N_c is the density of states of conduction band, μ is the mobility of the carrier, E is the applied electric field, ΔE_{ac} is the activation energy of electron, E is Boltzmann's constant, and E is the temperature.

For the charge transport process at high electric field, there are four main conduction mechanisms including Schottky emission $(LnI \propto \sqrt{V})$, space charge-limited conduction $(I \propto V^2)$, Fowler-Nordheim tunneling $(Ln(I/V^2) \propto V^{-1})$, and Poole-Frenkel (P-F) emission $(Ln(I/V) \propto \sqrt{V})^{16,39}$. Figure 5(b) shows the Ln(I/V) versus \sqrt{V} plot of the set process using positive DC. P-F emission was found to best fit the results, which indicates that P-F emission dominates the charge transport process at high electric field. The equation for P-F emission is given as.

$$I = q\mu EA n_0 \exp\left(-\frac{\varphi_B - \sqrt{\frac{qE}{\pi\varepsilon}}}{kT}\right)$$
 (2)

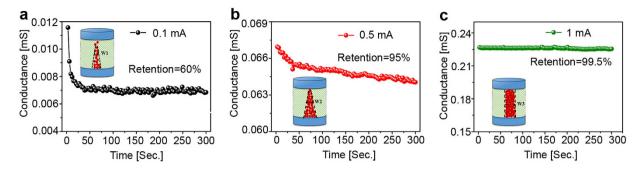


Figure 4. The data stability of FeO_x based memristor after electroforming by different I_{comp} . The resistances read at 0.1 V bias with the duration of 3 seconds for 100 cycles after forming with I_{comp} of (a) 0.1 mA, (b) 0.5 mA, and (c) 1 mA, respectively.

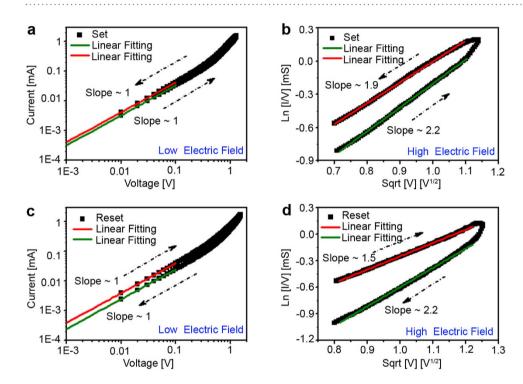


Figure 5. Typical analog *I-V* **curves and fittings.** (a) The double logarithmic graph of *I-V* curve of set process and linear fitting at low electric field $(0 \sim 0.10 \, \text{V})$. (b) Ln(I/V) vs. \sqrt{V} plot of set process at high electric field $(0.70 \sim 1.30 \, \text{V})$. (c) The double logarithmic graph of *I-V* curve of reset process as well as linear fitting at low electric field $(0 \sim 0.10 \, \text{V})$. (d) Ln(I/V) vs. \sqrt{V} plot of reset process at high electric field $(0.80 \sim 1.55 \, \text{V})$.

where, A is the area of the device, n_0 is the defect concentration, and φ_B is the depth of trap from conduction band of FeO_x which is corrected for the electric field in the exponential way, and ε is the dynamic permittivity. The temperature-dependent resistance measurement at the high resistance state further confirms that the P-F emission accounts for the charge transport process within the FeO_x layer as shown in Fig. S2. Furthermore, the charge transport mechanism is explored for the reset process in which ohmic conduction (Fig. 5(c)) and P-F emission (Fig. 5(d)) dominate for the memristor at low and high electric field, respectively.

To integrate the memristor as the electronic synapse in neuromorphic systems, besides the demonstration of spike-timing dependent plasticity (STDP) learning rule, the training characteristics by pulse train are also very important. However, it was neglected in the previous studies ^{12,14,31,40,41}. Therefore, we investigated the training characteristics by pulse train input in this work. It is widely accepted that learning and memorization process is associated with the synaptic weight modification in biology as shown in Fig. 6(a), and the synaptic weight can be modified by temporally correlated pre- and post-synaptic spiking via STDP³. Figure 6(b) manifests that the conductance of memristor can be successfully potentiated by thirty positive pulses and depressed by the subsequent thirty negative pulses. The retention of the memristor shown in Fig. S3 demonstrates that the conductance state could be retained in the long term timescale. These long-term potentiation (LTP) and long-term depression (LTD) characteristics can be applied to emulate the synapse plasticity of human brain^{3,4,10}. In addition, the pulse training performance as a function of pulse amplitude and width was further investigated. Figure 6(c) shows the

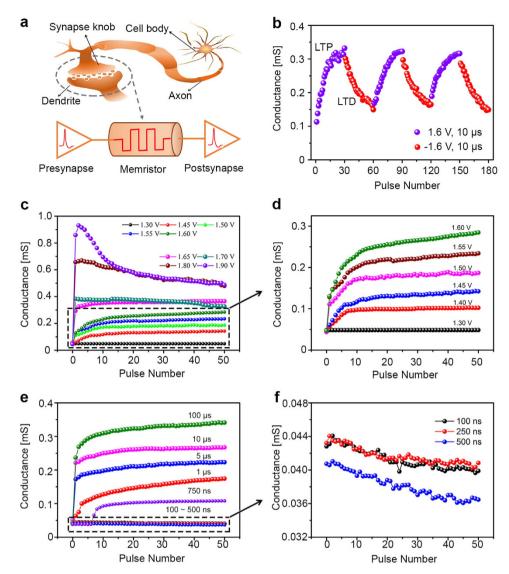


Figure 6. Implementation of long-term potentiation (LTP) and long-term depression (LTD) and pulse training performance on FeO_x based memristor. (a) Schematic illustration of using a memristor to emulate synapse function in neural networks. (b) Observation of long-term potentiation (LTP) and long-term depression (LTD) under 30 positive pulses $(1.60 \text{ V}, 10 \, \mu\text{s})$ and 30 negative pulses $(-1.60 \, \text{V}, 10 \, \mu\text{s})$, respectively. (c) Pulse amplitude-dependent conductance with 50 set pulses, pulse width fixed at $10 \, \mu\text{s}$ and pulse interval is 1 s, pulse amplitude varies from $1.30 \, \text{V}$ to $1.90 \, \text{V}$, (d) Pulse amplitude-dependent conductance with pulse width fixed at $10 \, \mu\text{s}$ and amplitude varied from $1.30 \, \text{V}$ to $1.60 \, \text{V}$. (e) Pulse width-dependent conductance with 50 set pulses, the pulse amplitude fixed at $1.60 \, \text{V}$, the pulse interval is 1 s and pulse width varies from $1.00 \, \text{ns}$ to $1.00 \, \mu\text{s}$. (f) The zoom-in display of the conductance against the short pulse width from $100 \, \text{ns}$ to $500 \, \text{ns}$ with fixed $1.60 \, \text{V}$ amplitude.

pulse amplitude dependence using 50 training pulses with a fixed width of $10\,\mu s$. Depending on the pulse amplitude, three kinds of analog behaviors are observed with various conductance changing trends. When the pulse amplitude ranges from $1.40\,V$ to $1.60\,V$, the memristor conductance gradually increases in a monotonic fashion as the pulse number increases, where a zoom-in plot is shown in Fig. 6(d). When pulse amplitude increases to $1.65\,V$ or $1.70\,V$, a plateau of conductance is observed following the initial jump generated by the first pulse. When the pulse amplitude is above $1.80\,V$, an impulse-like shape in conductance change is observed. In the first few pulses, the conductance increases dramatically. After reaching a peak, the conductance inversely decreases as the pulse number continuously increases. The variation of conductance changing behavior at different voltages is expected to relate to joule heating and electric field. In general, joule heating generated by the current enhances the drift and diffusion of oxygen vacancies $^{4.2}$, while electric field introduced by pulse voltage bias induces the drift of oxygen vacancies along the direction of electric field. As voltage amplitude increases, electric field and joule heating may reach a balance causing a dynamic equilibrium of oxygen vacancies after an initial conductance jump. Hence, the conductance may remain the same, as shown in the plateau region. Below this voltage amplitude, the effect of electric field dominates the conductance changing behavior leading to a monotonic increase of conductance.

Above this voltage amplitude, in the first few pulses, the large electric field drives the oxygen vacancies to form the cylinder-shaped filament as shown in Fig. 3(c). Once filament is formed, the current is significantly increased and joule heating dominates the movement of oxygen vacancies. Because of the high thermal conductivity of metal electrodes, the heat is expected to accumulate at the middle of filament and drives the oxygen vacancies moving away from the filament, resulting in a decrease of the conductance. These different analog behaviors could enhance the learning capabilities of memristor as electronic synapse to emulate comprehensive biological learning rules. When pulse amplitude is 1.30 V, no obvious conductance change is observed as shown in Fig. S4, which suggests the movement of oxygen vacancies is insufficient to influence the conductance.

To examine the effect of pulse width on memristors, pulses with amplitude of $1.60\,\mathrm{V}$ were applied since it provided a relatively large conductance window as observed in Fig. 6(d). The pulse width varied from $20\,\mathrm{ns}$ to $100\,\mu\mathrm{s}$. The conductance increases with the increase of pulse number whilst the pulse width increases from $750\,\mathrm{ns}$ to $100\,\mu\mathrm{s}$ as shown in Fig. 6(e). It is found that more number of pulses is required to trigger the increment of the conductance when pulse width reduces, such as 8 pulses are required to induce the conductance increment for pulse width of $750\,\mathrm{ns}$ and only 3 pulses are required for pulse width of $1\,\mu\mathrm{s}$. However, when the pulse width is shorter than $750\,\mathrm{ns}$, such as $100\,\mathrm{ns}$, $250\,\mathrm{ns}$, and $500\,\mathrm{ns}$ in Fig. 6(f), the conductance slightly decreases as the pulse number increases, indicating the accumulation of heat between adjacent pulse training cycles^{8,22,42}. Furthermore, it is noticed that there is also an abrupt change of conductance at the beginning of pulse training when the pulse is $1000\,\mathrm{\mu s}$ (Fig. S5). This phenomenon is possibly due to more oxygen vacancy drift driven by electric field during the training with long pulse width, leading to a large conductance change. The phenomenon shown in Fig. 6(e,f) may be utilized to emulate some other brain behaviors, such as habituation or sensitization 14,17,18.

In addition, the energy consumption is regarded as the most important issue for the neuromorphic devices. The memristors are desired to consume energy as low as possible. In our experiments, we find that operational voltages and currents are closely relevant to the $I_{\rm comp}$. As shown in Fig. 2, the lower $I_{\rm comp}$ results in lower energy consumption and the lowest energy consumption exhibits at the lowest $I_{\rm comp}$ of 0.1 mA. However, this low $I_{\rm comp}$ may generate the pyramidal shape conductive filament, which is unstable and easy to be dissolved. Therefore, there exists a tradeoff between the energy consumption and the stability of the memory.

Conclusion

In this work, we investigated the effect of the compliance current of electroforming process on the analog behavior using FeO_x based memristor. It was found that small $I_{\rm comp}$ tends to form a pyramidal CF resulting in poor data stability and the overlap of analog I-V curves, while large $I_{\rm comp}$ tends to form a cylindrical CF resulting in good data stability but a loss of analog behavior. $I_{\rm comp}$ with a proper value tends to form a conical CF leading to a large conductance window, good stability, and low voltage analog switching. A conductive filament model is introduced to explain the effect of $I_{\rm comp}$ on the formation of different CFs. The conduction mechanism is further investigated, which shows that ohmic conduction dominates the electron movement at low electric field and Poole-Frenkel emission accounts for its electron transport at high electric field. The LTP and LTD behaviors of FeO_x based memristor were demonstrated, showing the potential application in bio-inspired neuromorphic systems. Also of importance is that, the study on the pulse amplitude/width-dependence shows there are three various analog behaviors, where the conductance may monotonically increase, become plateau after initial jump, and continuously decrease after a peak, due to the competition between joule heating-induced migration and electric field-induced drift. Such different analog behaviors may enhance the learning capabilities of memristor as an electronic synapse to emulate comprehensive biological learning rules. This work would provide an important guidance in developing memristive nanodevices and the application in bio-inspired neuromorphic systems.

Methods

Device Fabrication. To fabricate the Pt/FeO $_x$ /Pt memristor devices, silicon wafer with 1 µm SiO $_2$ was used as the substrate. A 100 nm thick metallic Titanium (Ti) serving as an adhesion layer was deposited on the substrate by radio frequency (RF) magnetic sputtering, then a 40 nm thick platinum (Pt) was deposited by e-beam evaporation as the bottom electrode. Subsequently, an 80-nm-thick SiO $_2$ layer serving as an insulating layer was also deposited by e-beam evaporation. The 30 nm FeO $_x$ switching layer was deposited by RF magnetic sputtering. Finally top electrode consisting of 40 nm Pt and 100 nm Ti was deposited by e-beam evaporation.

Electrical Measurement. All the electrical characteristics were measured by a four-probe system (Cascade S300) equipped with a semiconductor characterization system (Keithley 4200-SCS). The various pulse conditions utilized in the testing are generated by Keithley 4200. During the electrical measurements, the positive bias was defined by the current flowing from the top electrode to the bottom one. All measurements were performed at room temperature in the air.

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Author Contributions

C.H.W. conceived the idea. C.H.W., Y.T. and W.H. carried out the devices fabrication and electrical testing. C.H.W. and W.H. proposed the models. C.H.W. performed material characterizations. C.H.W., W.H, Y.T. and R.Z. analyzed the data and co-wrote the paper. R.Z. and Y.T. directed the projects and provided overall guidance throughout. All the authors discussed the results and commented on the manuscript.

Additional Information

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