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Physical Modeling of Gate-Controlled Schottky Barrier Lowering of Metal-Graphene Contacts in Top-Gated Graphene Field-Effect Transistors

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A new physical model of the gate controlled Schottky barrier height (SBH) lowering in top-gated graphene field-effect transistors (GFETs) under saturation bias condition is proposed based on the energy conservation equation with the balance assumption. The theoretical prediction of the SBH lowering agrees well with the experimental data reported in literatures. The reduction of the SBH increases with the increasing of gate voltage and relative dielectric constant of the gate oxide, while it decreases with the increasing of oxide thickness, channel length and acceptor density. The magnitude of the reduction is slightly enhanced under high drain voltage. Moreover, it is found that the gate oxide materials with large relative dielectric constant (>20) have a significant effect on the gate controlled SBH lowering, implying that the energy relaxation of channel electrons should be taken into account for modeling SBH in GFETs.

Zero band gap and linear energy-momentum relationship are the characteristic properties of the graphene, owing to its two-dimensional nature. Therefore the behavior of carriers in graphene is similar to massless Dirac fermions with speed of 10^6 m s^{-1}[1]. The effective electron mass in monolayer graphene has been obtained from experiments as $0.012m_0$ (m_0 is the free electron mass)[2]. Graphene exhibits a high carrier mobility in the order of 20 000–200 000 cm^2 V^{-1} s^{-1} at room temperature[3], 16 000–42 000 cm^2 V^{-1} s^{-1}[4], 10 000–15 000 cm^2 V^{-1} s^{-1} for exfoliated graphene on SiO$_2$ substrate, and over 100 000 cm^2 V^{-1} s^{-1} for suspended samples[5]. This makes graphene as a promising candidate in ultra-fast electronic devices. A Schottky barrier is formed at the interface of the doped graphene-semiconductor junction[6,7]. In comparison with Si-based Schottky junction, experimental results showed that the SBH of grapheme transistor is strongly dependent on the gate voltage. It was observed that effective SBH decreases from 0.45 to 0.25 eV when the gate voltage increases from 0 to 5 V[7]. However, the explanation of the strong dependence of effective SBH on gate voltage is still not unclear. Yang *et al.*[7] thought that the SBH could be tuned by adjusting the work function of graphene due to the absence of Fermi-level at the interface. Kim *et al.*[8] believed that the image force also can lower SBH, which will result in some unreasonable conclusions shown in the following content. Chang *et al.*[25] experimentally reported that the SBH lowering is caused by hot electrons for Schottky barrier nanowire charge-trapping silicon–oxide–nitride–oxide–silicon devices. It implies that the physical origin of the SBH lowering in field-effect transistors caused by hot electrons should carefully be considered. In this paper, the effect of hot-electron is firstly introduced to successfully account for SBH lowering of GFETs.

Hot-electron phenomena are important in all semiconductor devices, which are governed by inelastic interactions between carriers and phonons. Elastic and inelastic collisions are the dominant mechanisms for momentum and energy relaxations, respectively. Hot-electron phenomena in semiconductor devices can be analyzed by using the continuity equation, momentum conservation equation, and energy conservation equation[9]. For transistors with the gate length less than micrometer, the non-equilibrium nature of electrons and phonons must

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Figure 1. Schematic cross section of a top-gated graphene transistor.

be considered[10]. The electron energy (electron temperature) can be much higher than lattice energy (lattice temperature) in semiconductor devices[9–11], while the energy difference between electrons and lattices is governed by the energy relaxation (ER) time[12]. Experimental results showed that the ER time in a graphene device is about 1 ps, and the electron gas temperature varies from 400 K to 700 K when the lattice temperature is 300 K in single-wall carbon nano-tubes[13]. Moreover, a larger difference between the electron temperature and the lattice temperature in graphene could be found[14].

Results

Theory. The aim of this study is to provide an explanation for gate-controlled Schottky barrier of a metal-graphene transistor on a silicon substrate reported in ref. 7. We thought that this modeling of the Schottky barrier height lowering effects could be used in any metal-semiconductor contact.

The device architecture of a top-gated graphene field-effect transistor can be simplified as the structure shown in Fig. 1, which is applicable for classical metal-graphene transistor or a metal-graphene transistor on a silicon substrate. The device architecture presented in ref. 7 could be equivalent to that in Fig. 1, when the gate-oxide-semiconductor structure can be treated as a parallel-plate capacitor (it implies that the electric field at the graphene/silicon interface perpendicular to the interface E_G equals to zero in Fig. 1). The channel in such a top-gated GFET (Fig. 1) is divided into the source region and the drain region. It is assumed that the electrons are widely spread over the graphene in the drain region and the channel electron, enclosed by the rectangle ABCD in Fig. 1, have the Gauss's surface. The saturation point is defined as $x = 0$, and the electric field outside the graphene layer is set as zero due to the screen effect by channel electrons. In other words, such a structure shown in Fig. 1 can be treated as a parallel-plate capacitor (the gate and the graphene can be regarded as parallel-plate terminals). The total of charge density (the charge density in the gate plus the charge density in the graphene) should be zero, therefore the electric field in the outside region of such a parallel-plate capacitor is zero according to the Gauss law, which is denoted as $E_G = 0$. Similar to the surface potential method for metal-oxide-semiconductor field effect transistor (MOSFET)[15], the Gauss law is applied to the sides of the rectangle ABCD shown in Fig. 1 under saturation bias conditions,

$$-\int_0^x \varepsilon_{ox} E_{ox}(x)\,dx - \int_0^{t_G} \varepsilon_G E_S\,dt + \int_0^{t_G} \varepsilon_G E(x)\,dt = -q \int_0^x \int_0^{t_G} \frac{(n - p + N_A - N_D)}{\varepsilon_G}\,dx\,dt \tag{1}$$

where $E_{ox}(x) = \frac{V_G - \psi_s(x) - V_{FB}}{t_{ox}}$, $\psi_s(x)$ is the surface potential at x, x is the coordinate along the channel (as shown in Fig. 1), V_G is the gate voltage, V_{FB} is the flat band voltage, t_G is the thickness of the graphene layer, t_{ox} is the thickness of the gate oxide, q is the electron charge, ε_G is the dielectric constant of the graphene, ε_{ox} is the dielectric constant of the gate oxide, N_D and N_A are the donor and acceptor concentrations, respectively, n is the electron density, p is the hole densities. The surface potential in the channel can be expressed as[16]:

$$\psi_s(x) = V(x) + V_{BI} \tag{2}$$

where $V(x)$ is the channel surface potential at x, qV_{BI} is the built-in potential energy from Fermi level of the source to the Fermi Level of the channel. Similar to the method in[16], for p-type graphene, one obtains

$$qV_{BI} = q\phi_{B0} - \left(\frac{E_{gg}}{2} - k_B T \, \ln\left(\frac{n_A}{n_{ig}} \right) \right) \tag{3}$$

where E_{gg} is the band gap of the graphene and $E_{gg} = 0$ for monolayer graphene, $q\phi_{B0}$ is the SBH (initial barrier height without lowering), n_A is the donor doping areal density in the graphene layer, k_B is the Boltzmann constant,

T is the temperature, and n_{ig} is the intrinsic carrier areal concentration of graphene. Thus the derivation of Eq. 1 for p-type graphene under depletion approximation can be written as[16]:

$$\frac{d^2 V(x)}{dx^2} - \frac{V(x)}{\varepsilon_G t_G t_{ox}/\varepsilon_{ox}} + \frac{(V_G - V_{BI} - V_{FB})}{\varepsilon_G t_G t_{ox}/\varepsilon_{ox}} = q\frac{N_A}{\varepsilon_G} \tag{4}$$

Using the boundary conditions $V(0) = V_{sat}$ (V_{sat}, the saturation voltage at onset of the saturation region, the position of $x = 0$ is the separating point between the source and drain regions), $V(\Delta L) = V_D$ (V_D is the drain voltage, ΔL is the length of the saturation region), $E(0) = E_{sat}$ (E_{sat} is the saturation channel electric field)[15], Eq. 4 can be solved to obtain V(x) as,

$$V(x) = -\frac{\varepsilon_G t_G t_{ox}}{\varepsilon_{ox}}C + \left(\frac{\varepsilon_G t_G t_{ox}}{\varepsilon_{ox}}C + V_{sat}\right)\cosh\left(\frac{x}{\sqrt{\frac{\varepsilon_G t_G t_{ox}}{\varepsilon_{ox}}}}\right) - \sqrt{\frac{\varepsilon_G t_G t_{ox}}{\varepsilon_{ox}}}E_{sat}\,\sinh\left(\frac{x}{\sqrt{\frac{\varepsilon_G t_G t_{ox}}{\varepsilon_{ox}}}}\right) \tag{5}$$

where $C = q\frac{N_A}{\varepsilon_G} - \frac{(V_G - V_{BI} - V_{FB})}{\varepsilon_G t_G t_{ox}/\varepsilon_{ox}}$. Thus the channel electric field distribution can be determined as:

$$E(x) = -\frac{dV(x)}{dx}$$

$$= -\left(\sqrt{\frac{\varepsilon_G t_G t_{ox}}{\varepsilon_{ox}}}C + \frac{V_{sat}}{\sqrt{\frac{\varepsilon_G t_G t_{ox}}{\varepsilon_{ox}}}}\right)\sinh\left(\frac{x}{\sqrt{\frac{\varepsilon_G t_G t_{ox}}{\varepsilon_{ox}}}}\right) - E_{sat}\,\cosh\left(\frac{x}{\sqrt{\frac{\varepsilon_G t_G t_{ox}}{\varepsilon_{ox}}}}\right) \tag{6}$$

In order to determine the effective channel length L_E, the length of the saturation region ΔL is required, the channel potential can be solved at $x = \Delta L$,

$$V_D = -\frac{\varepsilon_G t_G t_{ox}}{\varepsilon_{ox}}C + \left(\frac{\varepsilon_G t_G t_{ox}}{\varepsilon_{ox}}C + V_{sat}\right)\cosh\left(\frac{\Delta L}{\sqrt{\frac{\varepsilon_G t_G t_{ox}}{\varepsilon_{ox}}}}\right) - \sqrt{\frac{\varepsilon_G t_G t_{ox}}{\varepsilon_{ox}}}E_{sat}\,\sinh\left(\frac{\Delta L}{\sqrt{\frac{\varepsilon_G t_G t_{ox}}{\varepsilon_{ox}}}}\right) \tag{7}$$

Note that the lateral electric field along the channel in the source region can be treated as the gradual channel approximation[17] and the source voltage is 0 V, thus $V_{sat} = -\int_{-(L-\Delta L)}^{0} E_{sat}dx = -E_{sat}(L - \Delta L)$ (here L is the channel length), Substituting $E_{sat} = -\frac{V_{sat}}{(L-\Delta L)}$ into the Eq. 7, and one obtains

$$\Delta L = L - \frac{V_{sat}\sqrt{\frac{\varepsilon_G t_G t_{ox}}{\varepsilon_{ox}}}\,\sinh\left(\frac{\Delta L}{\sqrt{\frac{\varepsilon_G t_G t_{ox}}{\varepsilon_{ox}}}}\right)}{\left(V_D + \frac{\varepsilon_G t_G t_{ox}}{\varepsilon_{ox}}C\right) - \left(\frac{\varepsilon_G t_G t_{ox}}{\varepsilon_{ox}}C + V_{sat}\right)\cosh\left(\frac{\Delta L}{\sqrt{\frac{\varepsilon_G t_G t_{ox}}{\varepsilon_{ox}}}}\right)} \tag{8}$$

For simplicity, the lateral electric field in the drain region along the channel can be treated to be linear[15]

$$\frac{d^2 V}{dx^2}\Big|_{x=0} = -\frac{E_{sat}}{L_E} \tag{9}$$

where $L_E = L - \Delta L$ is the effective channel length. Solving Eq.1 with the boundary condition (Eq. 9), one obtains

$$E_{sat} = \frac{L_E}{\frac{\varepsilon_G t_G t_{ox}}{\varepsilon_{ox}} - L_E^2}\left(-\frac{t_G t_{ox}}{\varepsilon_{ox}}qN_A + V_G - V_{BI} - V_{FB}\right) \tag{10}$$

Thus the following is obtained:

$$V_{sat} = -\frac{L_E^2}{\frac{\varepsilon_G t_G t_{ox}}{\varepsilon_{ox}} - L_E^2}\left(-\frac{t_G t_{ox}}{\varepsilon_{ox}}qN_A + V_G - V_{BI} - V_{FB}\right) \tag{11}$$

Assuming that $L_E \gg \sqrt{\frac{\varepsilon_G t_G t_{ox}}{\varepsilon_{ox}}} = 2.1\sqrt{t_{ox}(\text{nm})}$ (for example $t_{ox} = 100\,\text{nm}$, $\sqrt{\frac{\varepsilon_G t_G t_{ox}}{\varepsilon_{ox}}} = 21\,\text{nm}$, $t_{ox} = 1\text{nm}$, $\sqrt{\frac{\varepsilon_G t_G t_{ox}}{\varepsilon_{ox}}} = 2.1\,\text{nm}$, thus it is found that, for realistic GFETs, such a condition is satisfied in most cases. Eq. 10 and Eq. 11 can be simplified as

$$E_{sat} = -\frac{1}{L_E}\left(-\frac{t_G t_{ox}}{\varepsilon_{ox}}qN_A + V_G - V_{BI} - V_{FB}\right) \tag{12}$$

$$V_{sat} = -\frac{t_G t_{ox}}{\varepsilon_{ox}} q N_A + V_G - V_{BI} - V_{FB}$$

(13)

Furthermore, assuming that $\Delta L \gg \sqrt{\frac{\varepsilon_G t_G t_{ox}}{\varepsilon_{ox}}}$, thus one obtains that $\cosh\left(\frac{\Delta L}{\sqrt{\frac{\varepsilon_G t_G t_{ox}}{\varepsilon_{ox}}}}\right) \approx \sinh\left(\frac{\Delta L}{\sqrt{\frac{\varepsilon_G t_G t_{ox}}{\varepsilon_{ox}}}}\right) \approx 0.5 \exp\left(\frac{\Delta L}{\sqrt{\frac{\varepsilon_G t_G t_{ox}}{\varepsilon_{ox}}}}\right)$. Therefore, Eqs 5, 6, and 8 can be further simplified as

$$V(x) = -\frac{\varepsilon_G t_G t_{ox}}{\varepsilon_{ox}} C + 0.5\left(\frac{\varepsilon_G t_G t_{ox}}{\varepsilon_{ox}} C + V_{sat} + \sqrt{\frac{\varepsilon_G t_G t_{ox}}{\varepsilon_{ox}}} E_{sat}\right) \exp\left(\frac{x}{\sqrt{\frac{\varepsilon_G t_G t_{ox}}{\varepsilon_{ox}}}}\right)$$

(14)

$$E(x) = -0.5\left(\sqrt{\frac{\varepsilon_G t_G t_{ox}}{\varepsilon_{ox}}} C + \frac{V_{sat}}{\sqrt{\frac{\varepsilon_G t_G t_{ox}}{\varepsilon_{ox}}}} + E_{sat}\right)$$

(15)

$$L_E = L - \sqrt{\frac{\varepsilon_G t_G t_{ox}}{\varepsilon_{ox}}} \; \log\left(L_E \frac{(V_D - V_{sat})}{0.5 V_{sat} \sqrt{\frac{\varepsilon_G t_G t_{ox}}{\varepsilon_{ox}}}}\right)$$

(16)

In a field-effect transistor, a lateral electric field in the channel not only results in a drift motion of electrons in the channel, but also changes their disordered thermal motion (the electron energy or electron temperature). Thus, the correlation between the electron temperature and lattice temperature in the channel of a transistor under the saturation bias conditions is given as[16]

$$T_e = T_L + \frac{2}{3}\frac{q\tau_e v E_{ch}}{k_B} = T_L + \frac{2}{3}\frac{q\tau_e \mu_e}{k_B} E_s^2$$

(17)

where μ_e is the mobility of electrons, τ_e is the ER time of electrons, v is the electron velocity, T_L is the lattice temperature (device temperature), and E_{ch} is the lateral electric field along the channel. Based on the gradual channel approximation, the effective SBH seen by the channel electrons when they obtain energy from the ER process can be written as

$$q\phi_B = q\phi_{B0} - k_B(T_e - T_L) = q\phi_{B0} - \frac{2}{3}q\tau_e \mu_e (E_s)^2$$

$$= q\phi_{B0} - \frac{2}{3}q\tau_e \mu_e \left(\frac{L_E}{\frac{\varepsilon_G t_G t_{ox}}{\varepsilon_{ox}} - L_E^2}\left(-\frac{t_G t_{ox}}{\varepsilon_{ox}} q N_A + V_G - V_{BI} - V_{FB}\right)\right)^2$$

(18)

where $q\phi_B$ is the effective SBH. Eq. 18 clearly shows that the effective Schottky barrier height will be affected by the difference between the electron temperature and lattice temperature. Larger difference between the electron temperature and lattice temperature could cause the larger reduction in the Schottky barrier height. According to the electron energy relationship, electron temperature increases with the square of the lateral electric field, electron energy relaxation time, and electron mobility. A lateral electric field in the channel can be analytically determined according to Eqns. 1–16. Because $L_E \gg \sqrt{\frac{\varepsilon_G t_G t_{ox}}{\varepsilon_{ox}}}$ is usually satisfied, Eq. 18 can be simplified as

$$q\phi_B = q\phi_{B0} - \frac{2}{3}\frac{q\tau_e \mu_e}{L_E^2}\left(-\frac{t_G t_{ox}}{\varepsilon_{ox}} q N_A + V_G - V_{BI} - V_{FB}\right)^2$$

(19)

On the other hand, for n-type graphene, we just need to replace all (N_A) with $(-N_D)$ in above equations. Then the similar equations for n-type graphene can be obtained.

For the source-drain current, the following equation of Schottky diode current-voltage relationship[16] can be used

$$I_{DS} = S\frac{4\pi m^* k_B^2 q}{h^3} T^2 \exp\left(-\frac{q\phi_B}{k_B T}\right)\left(\exp\left(\frac{q V_D}{k_B T}\right) - 1\right)$$

(20)

where S is the contact area between the source (drain) electrode and the channel (graphene), h is the Planck constant, and m^* is the effective mass of graphene. Therefore the source-drain current with consideration of the channel electrons ER can be written as

$$I_{DS} = S\frac{4\pi m^* k_B^2 q}{h^3}T^2 \times \left(\exp\left(\frac{qV_D}{k_B T}\right) - 1\right)$$

$$\times \exp\left(-\frac{\left(q\varphi_{B0} - \frac{2}{3}\frac{q\tau_e \mu_e}{L_E^2}\left(-\frac{t_G t_{ox}}{\varepsilon_{ox}}qN_A + V_G - V_{BI} - V_{FB}\right)^2\right)}{k_B T}\right)$$

(21)

Discussion

In our simulation, main parameters are given as following. The dielectric constant of 2.4 is used for graphene[18]. The thickness of single layer graphene is 0.34 nm[19]. According to other reports that the work function of graphene is considered as 4.5 eV in[20] and 4.4 eV in[21], the work function of graphene is considered as 4.5 eV in this paper[21]. The band gap of 1.12 eV is used for Si[16]. The relative dielectric constant of SiO_2, Si, and the published electron affinity of SiO_2 and Si are 3.9, 11.9, 0.9 eV and 4.05 eV, respectively [e.g.[22,23], and references therein]. The ER time is 1 ps[2], and the mobility is in the range of 1000–200000 cm^2 V^{-1} s^{-1} [3–5, the supplementary materials of 7]. International units have been used in all calculations.

It was experimentally reported that the effective SBH between graphene and silicon in a graphene device strongly depends on the gate voltage[7]. Kim, T. G. *et al* thought that such a SBH lowering effect should originate from the image potential in silicon nanowire field effect transistors (FET), where as the experimentally extracted SBH of 0.5 eV is smaller than that of 0.55 eV from the simulation[8], and the effective SBH could be expressed as[8,24],

$$q\phi_{Bi} = q\phi_{B0} - q\sqrt{\frac{q|F_m|}{4\pi\varepsilon_s}} = q\phi_{B0} - q\sqrt{\frac{qC_1}{4\pi\varepsilon_s}V_D + \frac{qC_2}{4\pi\varepsilon_s}V_G + \frac{qC_3}{4\pi\varepsilon_s}}$$

(22)

where t_s is the thickness of the nanowire, ε_s is its dielectric constant of the graphene, $q\phi_{Bi}$ is the effective SBH with consideration of the image force, the C_1, C_2, and C_3 are fitting parameters. And the channel surface electric field is[24]

$$F(x) = \frac{-\left(V_D + V_{bi} - \left(V_G - V_{FB} - q\frac{t_G t_{ox}}{\varepsilon_{ox}}N_d\right)\right)\left(e^{\frac{x}{\lambda}} + e^{-\frac{x}{\lambda}}\right)}{\lambda\left(e^{\frac{L}{\lambda}} + e^{-\frac{L}{\lambda}}\right)}$$
$$+ \frac{\left(V_{bi} - \left(V_G - V_{FB} - q\frac{t_G t_{ox}}{\varepsilon_{ox}}N_d\right)\right)\left(e^{\frac{L-x}{\lambda}} + e^{-\frac{L-x}{\lambda}}\right)}{\lambda\left(e^{\frac{L}{\lambda}} + e^{-\frac{L}{\lambda}}\right)}$$

(23)

where $\lambda = \sqrt{\frac{\varepsilon_s t_s t_{ox}}{\varepsilon_{ox}}}$. Thus[24]

$$F_m = F(0) = \frac{-2\left(V_D + V_{bi} - \left(V_G - V_{FB} - q\frac{t_s t_{ox}}{\varepsilon_{ox}}N_d\right)\right)}{\lambda\left(e^{\frac{L}{\lambda}} + e^{-\frac{L}{\lambda}}\right)} + \frac{\left(V_{bi} - \left(V_G - V_{FB} - q\frac{t_s t_{ox}}{\varepsilon_{ox}}N_d\right)\right)}{\lambda}$$

(24)

and

$$C_1 = \left(-\frac{2}{\lambda\left(e^{\frac{L}{\lambda}} + e^{-\frac{L}{\lambda}}\right)}\right)$$

(25)

$$C_2 = \left(\frac{2}{\lambda\left(e^{\frac{L}{\lambda}} + e^{-\frac{L}{\lambda}}\right)} - \frac{1}{\lambda}\right)$$

(26)

Using the parameters in[24], for example $\frac{L}{\lambda} = \frac{5\ \mu m}{\sqrt{\frac{\varepsilon_s t_s t_{ox}}{\varepsilon_{ox}}} \approx \sqrt{\frac{11.9}{3.9}} \times (0.05\ \mu m) \times (5\ \mu m)} > 4$. Therefore, $\frac{2}{\lambda}e^{-\frac{L}{\lambda}} < \frac{0.03664}{\lambda}$ and $C_2 = \left(-\frac{1}{\lambda}\right)$ because $e^{-\frac{L}{\lambda}} < e^{-4} = 0.01832$, and

$$q\phi_{Bi} = q\phi_{B0} - q\sqrt{0.055V_D + 0.15V_G + \frac{qC_3}{4\pi\varepsilon_s}}$$

(27)

C_1, C_2, and C_3 are just fitting parameters in the former studies[8,24]. Solving Eqns. 25, 26, $C_1/C_2 = 2e^{-\frac{L}{\lambda}} < 0.03664$. However, extracted from experimental results, $C_1/C_2 = 0.02/0.00015 \approx 133$ for the positive V_D, significant larger that the above theoretically calculation value, which denotes that the image force can not give a good explanation on the experimental data of the gate controlled SBH.
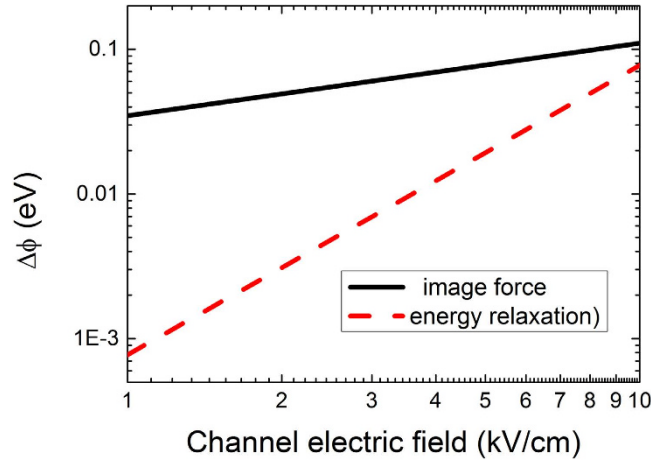
Figure 2. The SBH caused by the image force and the ER as a function of the channel electric field.
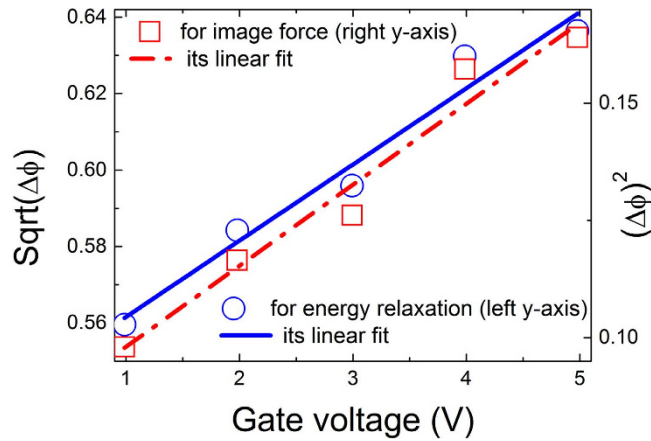

Figure 3. The experimental values $\sqrt{\Delta\phi}$ and $(\Delta\phi)^2$ as a function of the gate voltage, experimental data from ref. [7].

Therefore, the hot-electron effect is adopted to theoretically investigate the gate controlled SBH in graphene. In the following results, the different effects of the image potential and the ER of channel electrons on the SBH lowering are shown, and the comparison of simulation results with experimental results of silicon nano-wire FETs is given.

Figure 2 shows the reduction in the SBH (or the SBH lowering), $\Delta\phi = q\phi_{B0} - q\phi_B$, caused by the image force (Eq. 22) and the ER ((Eq. 18)), respectively, as a function of the lateral channel electric field. In Fig. 2, the ER time of 0.8 ps at 300 K[26] and the mobility of 1450 cm/V·s[16] for electrons in silicon have been used. For $V_G = 0$, it could be found that the $\Delta\phi$ between $V_D = 0$ V and $V_D = 1$ V is around 0.02 eV according to the experimental data from Fig. 7 of ref. 24. For simplicity, the lateral channel electric field could be simplified as $E_{ch} \approx \frac{V_D}{L} = 5$ (kV/cm) at $V_D = 1$ V and $V_G = 0$. It is easily found in Fig. 2 that the reduction of the SBH $\Delta\phi$ caused by the image force is around 0.078 eV at the channel electric field of 5 kV/cm, whereas the $\Delta\phi$ caused by the ER of channel electrons is around 0.019 eV. Fig. 2 proves the validity of the ER of channel electrons as the physical mechanism of the SBH lowering in field-effect transistor by comparing the difference of SBH lowering induced by the image force and ER of channel electrons with experimental results.

According to Eq.22, the SBH lowering ($\Delta\phi$) caused by the image force is proportional to the square root of the gate voltage, which denotes that $\Delta\phi \propto -\sqrt{V_G}$ or $V_G \propto -(\Delta\phi)^2$. While the SBH lowering caused by the ER of electrons is proportional to the square of the gate voltage according to Eq. 18, which denotes that $\Delta\phi \propto -(V_G)^2$ or $V_G \propto -\sqrt{\Delta\phi}$. The further comparison of the reductions in SBH calculated by the image potential (the ER of channel electrons) and extracted from experimental data in ref. 7 is given as following.

Figure 3 shows that the square of the SBH reduction $(\Delta\phi)^2$ and the square root of the SBH reduction $(\sqrt{\Delta\phi})$ as a function of the gate voltage (the symbols in Fig. 3 are the experimental data that come from Fig. 3 B in ref. [7], and the SBH value of 0.67 eV is used to estimate $\Delta\phi$). Although both methods for the SBH lowering using the image force and the ER of channel electrons could be used to explain the SBH lowering observed in the
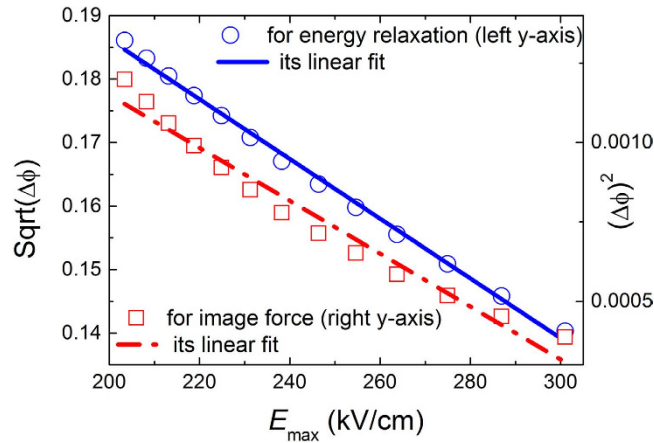
Figure 4. The experimental values $\sqrt{\Delta\phi}$ and $(\Delta\phi)^2$ as a function of the maximum electric field in the graphene/p-Si contact, according to ref. [27].

experimental results, which is shown in Fig. 3. Experimental extracted $\sqrt{\Delta\phi}$ ~ Vg has a slightly better linear fitting in comparison with the linearly fitting of $(\Delta\phi)^2$ ~ Vg. The adjusted R-Square is 0.95557 for linearly fitting of $\sqrt{\Delta\phi}$ to V_G, and the adjusted R-Square is 0.95308 for linearly fitting of $(\Delta\phi)^2$ to V_G, which demonstrates that the SBH lowering caused by the ER of channel electrons agrees better with the experimental results.

For the SBH lowering in the graphene/p-Si contacts, the maximum field graphene/p-Si contact under the abrupt approximation can be written as[16]

$$E_{\max} = \frac{\sqrt{qN/\varepsilon_s}}{\sqrt{2\left(\left(\frac{E_g}{2} - kT\ \ln\left(\frac{N}{n_i}\right)\right)/q - V - \frac{kT}{q}\right)}}$$

(28)

where $E_g = 1.12$ eV is the band gap of silicon. For a Schottky junction, the reduction in SBH caused by the ER of electrons is $\Delta\phi = \frac{2}{3}q\tau_e\mu_e(E_{\max})^2$ according to Eq.18 ($\sqrt{\Delta\phi}$ should be linearly dependent on $E_{\max}$), whereas the SBH caused by the image force is $\Delta\phi = q\sqrt{\frac{q|E_{\max}|}{4\pi\varepsilon_s}}$ according to Eq. 22 ($(\Delta\phi)^2$ should be linearly dependent on $E_{\max}$).

Figure 4 shows how experimental values of the $(\Delta\phi)^2$ and $\sqrt{\Delta\phi}$ change with the maximum electric field in the graphene/p-Si contact (the symbols in Fig. 4 are the experimental data and come from Fig. 2 C of ref. [27]). In Fig. 4, it is also clearly shown that there is a better linear fit between experimental extracted $\sqrt{\Delta\phi}$ and $E_{\max}$ in comparison with the curve of $(\Delta\phi)^2$ and $E_{\max}$. The adjusted R-Square is 0.99584 when we linearly fit $E_{\max}$ to $\sqrt{\Delta\phi}$, and the adjusted R-Square is 0.96622 when we linearly fit $E_{\max}$ to $(\Delta\phi)^2$. It indicates again that the SBH lowering caused by the ER is more in accord with the experimental results. All above results show that modeling the SBH lowering by using the ER of channel electrons in semiconductor devices is consistent with experimental results.

In the following, we will discuss the detailed influence of the ER of channel electrons on the gate controlled SBH lowering. It should be noted that the saturation density of n-type doping in monolayer graphene is around 1×10^{13} cm^{-2} [28] and the net p-type doping in bilayer and monolayer graphene is around 2×10^{13} cm^{-2} [29]. It was reported in[30] that the saturation characteristic of top-gated GFET degrades with the channel length shrinking from 5.6 μm down to 100 nm, and complete saturation can occur at the channel length of 5.6 μm. The source and drain material of p-type silicon is used in the following calculations. It should be noted that the electron velocity in a graphene can reach 1×10^6 m/s[1], thus the distance of electron transport in the graphene during 1 ps is 1 μm. For the energy balance conditions, all channel length used in the following calculations is larger than 1 μm. And $V_{FB} = 0$ is chosen in the all calculations of this work.

Figure 5 shows how the reduction of the SBH caused by the relaxation of channel electrons as a function of the gate voltage for different acceptor densities, where for larger acceptor doping in a GFET a larger gate controlled SBH lowering could be observed. From Fig. 5, it can be concluded that the effective SBH between graphene and electrode in a GFET decreases with the increasing of gate voltage, which clearly shows that the SBH lowering in a GFET can be modulated by applying different gate voltages due to the ER of channel electrons.

Figure 6 shows how the reduction of the SBH caused by ER of electrons changes with the gate voltage for different drain voltages. The inset of Fig. 6 shows that the reduction in the SBH caused by the ER of channel electrons slightly increases with the drain voltage. Because the saturation voltage is independent on the drain voltage according to Eq.13 and the relative small change in the effective channel length is caused by the drain voltage according to Eq. 16, the drain voltage could hardly reduce the SBH according to Eqs. 18 or 19.

Figure 7 shows that the reduction of the SBH caused by the ER of channel electrons as function of the relative dielectric constant and thickness of the gate oxide in a GFET. It is observed that the reduction of the SBH rapidly increases firstly with the relative dielectric constant of the gate oxide in a GFET, then approaches to a saturation
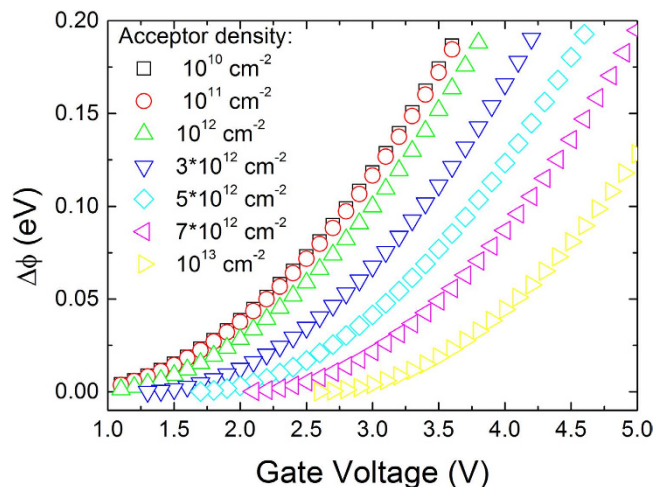
Figure 5. The reduction of the SBH as a function of the gate voltage with the HfO$_2$ layer thickness of 20 nm for different acceptor density. The channel length is 2 μm, the drain voltage is 3 V, the electronic mobility is 1300 cm^2 V^{-1} s^{-1}, the ER time is 1 ps and the device temperature is 300 K.
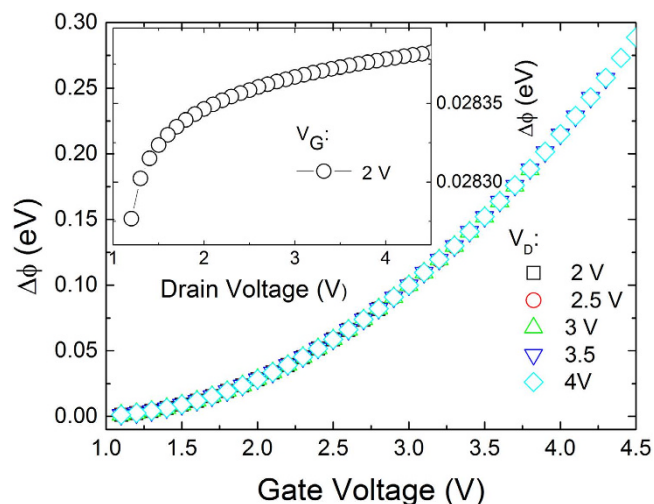

Figure 6. The reduction of the SBH as a function of the gate voltage with the HfO$_2$ layer thickness of 20 nm for different drain voltage. The inset figure shows the reduction of the SBH as a function of drain voltage when the gate voltage is 2 V. The channel length is 2 μm, the drain voltage is 3 V, the acceptor density in graphene is 1×10^{12} cm^{-2}, the electronic mobility is 1300 cm^2 V^{-1} s^{-1}, the ER time is 1 ps and the device temperature is 300 K.

value for the large relative dielectric constant (>20), which implies that gate insulator materials with high relative dielectric constant (>20) should be chosen for the best gate controlled SBH lowering effects in a GFET. Fig. 7 also shows the reduction of the SBH decreases with a thicker oxide since the saturation voltage and electric field decreases with the increasing of oxide thickness according to Eq. 13 and Eq. 12.

Figure 8 shows how the reduction of the SBH between the graphene and electrode in a GFET changes with the channel length for different gate voltages under a given drain voltage. The reduction in the SBH firstly rapidly decreases with increasing channel length, then saturates with further increasing of channel length. It is because the strength of saturation electric field along the channel is the reciprocal of the effective channel length according to Eq. 12, under the approximation assumption of gradual channel. It should be noted that the reduction of the SBH is a reciprocal function of the square of the effective channel length according to Eq. 18 or Eq. 19, thus the reduction of the SBH rapidly deceases with the increasing of channel length. Such a reduction is too small to be observed when the channel length is large enough. The inset figure in Fig. 8 illustrates that a change in doping density for small acceptor doping in graphene ($<1 \times 10^{11}$ cm^{-2}) have almost no effect on the effective SBH, but a change in doping density for larger acceptor doping in graphene ($>1 \times 10^{11}$ cm^{-2}) could significantly affect the effective SBH.

Though the models presented in the previous literature work[31,32] could describe the current-voltage characteristics of GFETs, it is difficult to analytically formulate Schottky barrier height lowering effects. In these models,
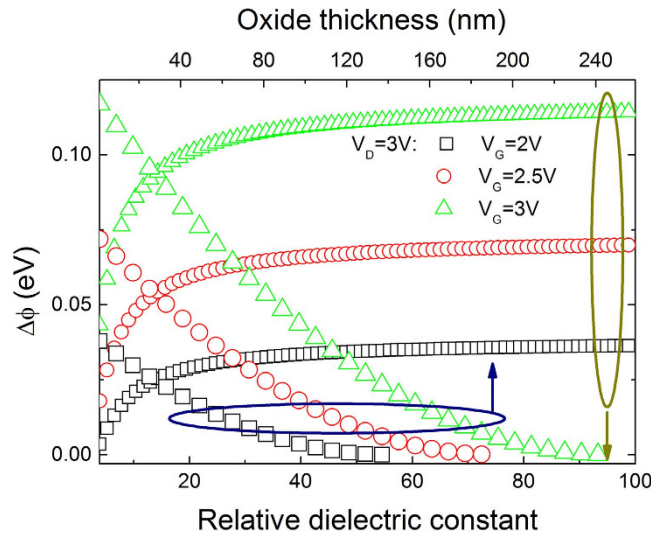
Figure 7. The reduction of the SBH as a function of the relative dielectric constant of the gate oxide with 20 nm thickness. The channel length is $2\,\mu$m, the acceptor density in graphene is $1 \times 10^{12}\,cm^{-2}$ the electronic mobility is $1300\,cm^2\,V^{-1}\,s^{-1}$, the ER time is 1 ps and the device temperature is 300 K.
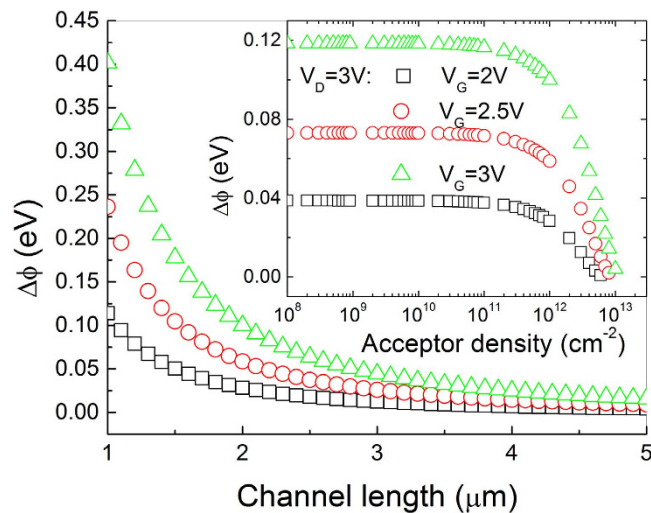

Figure 8. The reduction of the SBH as a function of the channel length when the acceptor density in graphene is $1 \times 10^{12}\,cm^{-2}$. The inset figure shows the reduction of the SBH in as a function of the acceptor density when the channel length is $2\,\mu$m. The HfO_2 layer thickness is 20 nm, the electronic mobility is $1300\,cm^2\,V^{-1}\,s^{-1}$, the ER time is 1 ps and the device temperature is 300 K.

many parameters have been used for Schottky barrier height lowering effect; where some fitting parameters have to be adopted to keep consistent with experimental results. Therefore, the lack of concise expression for the gate-controlled Schottky barrier height lowering effects limits the practical application of these methods. In our proposed model, main parameters still provide clear physical meanings, especially for the Schottky barrier height lowering effect, indicating that these model parameters could be expressed by device parameters, such as relative dielectric constant, channel density, doping density, and the energy relation time, which ensure device optimization design of the high-performance graphene field effect transistors. At the same time, due to general validity of electron transport of Eqs. 17 and 18 in various semiconductor materials, the proposed model could be extended to non-graphene materials and other device architectures only if the channel electric field is known. In others words, we can obtain similar conclusions by using the derivation of the channel electric field in other device architectures.

Conclusions
In conclusion, the effect of the ER (Energy Relaxation) of channel electrons on the SBH between graphene and electrode in a GFET has been theoretically investigated and physically modeled. The theoretical calculations agree well with experimental data reported in ref. [7,24,27]. The ER of channel electrons can result in a high electron temperature, thus causing a larger reduction in the SBH between graphene and electrode. Based on the energy

conservation equation with the balance assumption, a physical model is built in this work to describe the gate controlled SBH lowering effects in a GFET under the saturation mode. The increases in the electron mobility and the ER time of channel electron will result in a linear increase in the reduction in the SBH according to the proposed model (Eq. 19). And the effects of parameters such as oxide thickness, oxide relative dielectric constant, channel length, drain voltage, and acceptor density are analyzed in detail. The drain voltage has slightly effect on the reduction of the SBH. The increase of the gate oxide thickness, the acceptor density in the graphene, and the channel length result in the decrease of SBH reduction magnitude. Whereas, increase in the dielectric constant of the gate oxide and the gate voltage result in obvious SBH reduction. All these results indicate that the effect of electron ER on the reduction in SBH should be seriously taken into account in GFETs with nano-scale dimension.

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Author Contributions

L.F. conceived the idea and wrote the main manuscript text. H.Z.L. and J.Y. contributed for the editing of the manuscript. All authors discussed the results and reviewed the manuscript.

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