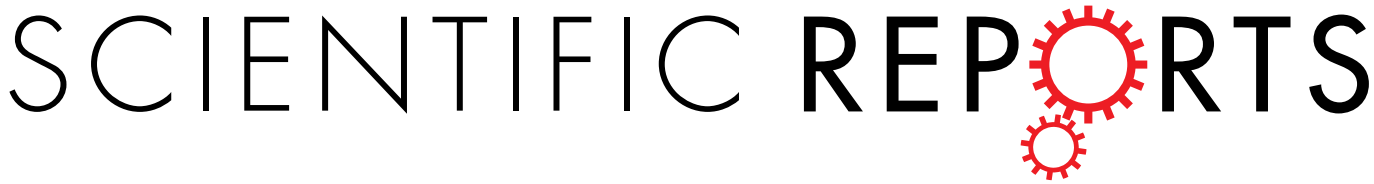

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Mechanically Flexible and High-Performance CMOS Logic Circuits

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Received: 20 July 2015
Accepted: 15 September 2015
Published: 13 October 2015

Low-power flexible logic circuits are key components required by the next generation of flexible electronic devices. For stable device operation, such components require a high degree of mechanical flexibility and reliability. Here, the mechanical properties of low-power flexible complementary metal–oxide–semiconductor (CMOS) logic circuits including inverter, NAND, and NOR are investigated. To fabricate CMOS circuits on flexible polyimide substrates, carbon nanotube (CNT) network films are used for p-type transistors, whereas amorphous InGaZnO films are used for the n-type transistors. The power consumption and voltage gain of CMOS inverters are $<$500 pW/mm at $V_{in}=0$ V ($<$7.5 nW/mm at $V_{in}=5$ V) and $>$45, respectively. Importantly, bending of the substrate is not found to cause significant changes in the device characteristics. This is also observed to be the case for more complex flexible NAND and NOR logic circuits for bending states with a curvature radius of 2.6 mm. The mechanical stability of these CMOS logic circuits makes them ideal candidates for use in flexible integrated devices.

The development of flexible electronic components such as transistors and integrated circuits is essential for the realization of flexible, stretchable, and wearable electronic devices that can be attached to a wide range of surfaces. Many different approaches for the fabrication of high-performance, flexible transistors have been reported previously using organic and/or inorganic materials[1–9]. Due to the processing challenges inherent in the fabrication of thin-film transistors (TFTs) on flexible substrates, most of these reports have focused on the fabrication of these devices, predominantly in deposition[10,11], solution-based processing[12–15], and printing methods[3,4,16]. For reports that do address the mechanical reliability of these devices, these have generally studied the characteristics of single flexible TFT devices (either n-type or p-type)[3,6,9,11,14,16–20]. However, in order to work towards the realization of low-power electrical devices, it is more appropriate to consider the performance of flexible circuit systems such as those based on complementary metal–oxide–semiconductor (CMOS) structures that integrate both n- and p-type TFTs, as opposed to simply measuring the performance of single devices. Several reports have been published that deal with the development of flexible CMOS circuitry, employing fabrication techniques including the film transfer method[1] or combinations of printing and deposition methods[2,21–24]: these reports present promising results for low-power logic circuits. However, the mechanical flexibility of integrated CMOS logic circuits have yet to be investigated in detail, although testing of standalone TFT devices has been widely reported[1,6,7,17,18]. In this study, we report the mechanical flexibility of CMOS logic circuits such as inverter, NAND, and NOR circuits to confirm that they exhibit near-identical electrical characteristics under both flat and bending test conditions. To demonstrate such behavior, flexible polyimide-based TFT devices using amorphous InGaZnO for n-type devices[10,24,25] and 99% semiconductor-enriched carbon nanotube (CNT) network films for p-type devices[12,24,26] were fabricated and incorporated into the aforementioned logic circuits. This study particularly focuses on the effects of bending on voltage gain and threshold voltage for the CMOS inverters, and the investigation of logic operations for CMOS NAND and NOR circuits.

Device Fabrication

Figure 1(a) depicts the fabrication process of the flexible InGaZnO–CNT CMOS logic circuits. To form the substrates, a polyimide (PI) solution (Sigma-Aldrich, USA) was spun on a handle wafer of Si/SiO_2

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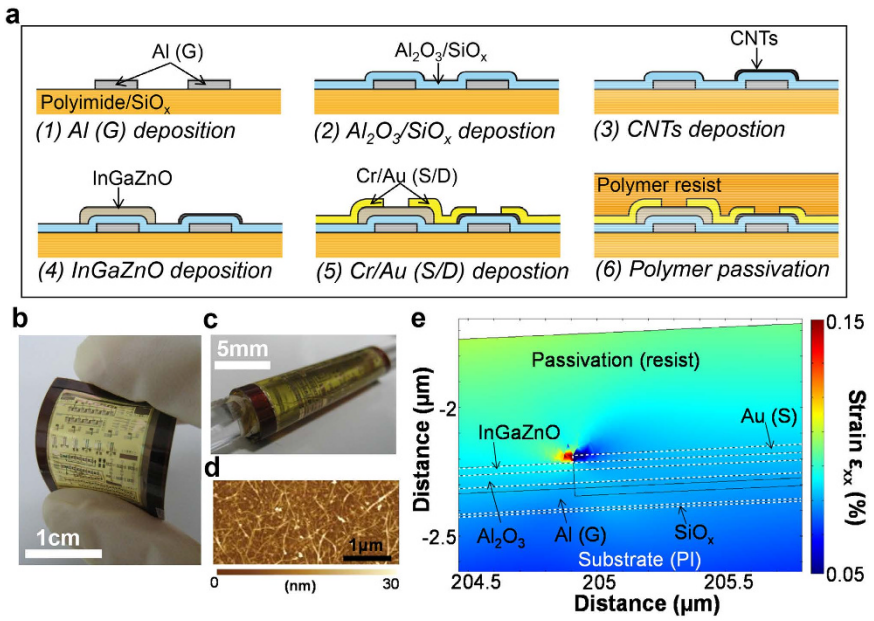

Figure 1. Process and strain distribution. (**a**) Fabrication process of flexible InGaZnO–CNT CMOS logic circuits. Photographs of flexible CMOS circuits under (**b**) bending by hand and (**c**) rolling over a glass bar (~2.6 mm radius). (**d**) AFM image of CNT network film for p-type TFT. (**e**) FEM simulation plot modeling the strain distribution in the InGaZnO channel region under bending ($r = 2.6$ mm).

and cured at 350 °C for 1 hour to form ~10 μm thick PI film. In order to improve the adhesion between the PI film and CMOS device components, a 10 nm thick SiO_x layer was deposited on the PI surface by electron beam (EB) evaporation. For the gate electrodes of both InGaZnO and CNT TFTs, an aluminum (Al) layer (100 nm thick) was deposited using a sputter tool (ULVAC, Japan), and subsequently patterned using a wet Al etchant. For the gate dielectric, a 50 nm thick layer of Al_2O_3 was deposited by atomic layer deposition (ALD) (Arradiance, USA) at 200 °C using the precursors of trimethylaluminium (TMA) and H_2O, followed by a SiO_x (10 nm thick) film formed by EB evaporation. We have observed that the presence of the SiO_x layer on top of Al_2O_3 serves to enhance the CNT network deposition, which allows for the realization of devices with high on-currents and mobilities. To further increase the density of the CNT networks[12], the surface of the SiO_x layer was cleaned using oxygen plasma and subsequently chemically treated with poly-L-lysine (Sigma-Aldrich) for 5 min. A commercially available 99% semiconductor-enriched CNT solution (Meijo Nano Carbon, Japan) was deposited for 20 min by soaking in the solution and rinsed with deionized (DI) water. CNT deposition and DI water rinse cycles were repeated up to 4 times to form relatively high-density CNT networks. The CNT network films were patterned by oxygen plasma (100 W) for 90 sec. Next, for the n-type channels, 30 nm thick amorphous InGaZnO films were deposited using a sputter tool under a chamber pressure of 13 Pa: this was achieved by controlling argon gas with oxygen gas of 6.4 sccm flow. InGaZnO films were patterned by a lift-off process. Via holes were etched in the Al_2O_3/SiO_x layers using a buffered hydrofluoric acid (BHF) solution, with subsequent deposition of source (S) and drain (D) electrodes (Cr/Au) carried out by EB evaporation and patterned using a lift-off process. Subsequently, a ~600 nm thick polymer resist (TSMR-V50EL; Tokyo Ohka Kogyo, Japan) layer was spun to passivate the InGaZnO–CNT CMOS circuit, in effect suppressing the strain effect under bending and preventing physical damage. Finally, the devices were detached from the handle wafer. Fig. 1(b,c) show photographs of the flexible CMOS logic circuit devices that were shown not to crack or delaminate under bending. Based on the surface morphology of atomic force microscopy (AFM) image in Fig. 1d, CNT network density is relatively low. By increasing the surface treatment and/or deposition time of CNTs, the density can be increased as the ones reported previously[12], resulting in that the field effect mobility may be increased more.

Results and Discussion

To understand the strain distribution under bending, a finite element method (FEM) simulation was conducted. The simulation was only carried out for the InGaZnO film as the mechanical properties of the CNT network film were not known. We speculate that the strain distribution values of the CNT network films under bending are similar to those of InGaZnO; however, further studies into the properties of CNT network films are required to verify this assumption. As shown in Fig. 1(e), under bending with a 2.5 mm curvature radius, the maximum strain in InGaZnO film is ~0.08% tensile strain: such a value may be small enough for the circuit to operate with no changes to its electrical properties. Further

reductions to the strain in the InGaZnO film may be attained by using a thicker passivation layer: as observed from Fig. 1(e), this would move the semiconducting layer towards the neutral strain region in the film stack.

The electrical properties of the InGaZnO–CNT CMOS inverter were measured prior to testing under bending conditions. The circuit diagram and a photograph of the fabricated CMOS inverter are shown in Fig. 2(a,b). The channel length and width of both InGaZnO and CNT TFTs are 100 μm and 400 μm, respectively, and each current value was normalized according to the channel width. Figure 2(c,d) present the switching and output characteristics of both InGaZnO and CNT TFTs. InGaZnO (CNT) TFTs exhibit a relatively good I_{on}/I_{off} ratio of $>10^5$ ($>10^4$) at $V_{DS} = 5$ V and a peak field effect mobility of ~5.5 cm^2/Vs (~2.2 cm^2/Vs) at $V_{DS} = 1$ V. The mobility was extracted from the parallel plate gate model using a measured gate capacitance (*i.e.* Al_2O_3/SiO_x) value of ~8.0×10^{-4} F/m^2. Next, the CMOS inverter was characterized as shown in Fig. 2(e,f): the device exhibited a high voltage gain of ~45 at a driving voltage, V_{DD}, of 5 V. Subsequently, the power consumption was calculated using the relation $I_{DD}/W \times V_{DD}$ ($= 5$ V) based on the results of Fig. 2(e): importantly, the power consumption at steady state was found to be <7.5 nW/mm at $V_{in} = 5$ V and <500 pW/mm at $V_{in} = 0$ V owing to the off-current of two TFT components, ~10^{-9} A/mm for the CNT and ~10^{-10} A/mm for the InGaZnO TFT, values that are comparable to those previously reported for low-power consumption circuits[27]. As the operating speed, Fig. 2g indicates that the rise time of a CMOS inverter is ~0.75 ms by observing the change of output voltage from 0 V to 5 V. The rise speed depends on the FET geometry, and it can be faster by fabricating smaller device if needed.

Mechanical flexibility of the CMOS inverters is characterized by measuring electrical properties as a function of bending radius, *r*, of the substrate (Fig. 3(a)). First, $V_{out} - V_{in}$ at $V_{DD} = 5$ V was measured as a function of *r*, up to 2.6 mm (Fig. 3(b,c)). Although there are small differences for electrical properties between each measurement, the peak gain and threshold voltage are relatively constant as shown in the compiled results in Fig. 3(d). This shows that the flexible CMOS inverter is not affected by the strain arising from substrate bending since there is no trend for changes in the electrical properties. This is in good agreement with the FEM simulation of strain distribution as discussed in Fig. 1(e), where the strain in the TFT channel was observed to be small (~0.08%). Since the strain does not significantly affect the performance of the flexible CMOS circuits, small fluctuations for voltage gain and threshold voltage might attribute to a hysteresis of CNT TFTs (Fig. S1). To prevent hysteresis in the characteristics of CNT TFTs, a more effective passivation layer is required, particularly one that can inhibit the diffusion of water molecules into the device[28]. To shed light further on the mechanical reliability of the flexible InGaZnO–CNT CMOS circuit, the device characteristics were measured whilst the circuit was subjected to up to 1000 bending cycles with a bending radius <6 mm: these results are shown in Fig. 3(e,f). Again, although small fluctuations in electrical properties were observed, all measured characteristics including voltage gain and threshold voltage were measured to be relatively stable. These results convey that the fabricated InGaZnO–CNT CMOS inverters are mechanically flexible and reliable given the lack of substantial changes in functional properties on bending.

Considering that more complex circuitry than the CMOS inverter (NOT circuit) is required in many practical applications, CMOS NAND and NOR circuits were also fabricated and characterized under the same bending conditions as used for the CMOS inverter ($r = 2.6$ mm). These two logic circuits are described in Fig. 4(a–d) and used the same channel dimensions (length = 100 μm, width = 400 μm) as the CMOS inverter discussed above. Two voltage input signals (0 V and 5 V) of $V_{A\text{-}IN}$ and $V_{B\text{-}IN}$ were used with different frequencies of square pulses with an amplitude of 5 V to create every digital input signal (*i.e.* 00, 01, 10, 11, shown in Fig. 4(e)): for this digital logic circuit, input voltages of 5 V and 0 V are "1" and "0" signals, respectively. Firstly, the flexible CMOS NAND and NOR circuits were confirmed to operate correctly as shown in Fig. 4(f,g). Furthermore, this also shows logic circuit operation under $r = 2.6$ mm bending conditions, showing that the flexible CMOS NAND and NOR circuits, as was the case for the CMOS inverter, possess the same functionality under both flat and bending conditions. From these results, it can be concluded that complex logic circuits can also possess mechanical flexibility with at least hundreds of input operations confirmed by the experiment based on Fig. 4(e–g).

In this study, we fabricated the TFTs with relatively large channel length (100 μm) and width (400 μm). TFTs should be designed for the application depending on how high operating on-current and speed are required. In this platform, if higher parameters are required, several micro meter size for channel length can be used without affecting another performance such as I_{on}/I_{off} based on previous studies[12,17]. However, smaller channel length may be challenge due to the purity of semiconductor CNTs in the solution (99% semiconductor and 1% metallic CNTs) that creates current paths through the metallic CNTs between S/D electrodes. By developing high purity CNT solution, it may be possible to scale down further in the future.

In summary, we fabricated and characterized flexible CMOS logic circuits by comparing the properties at flat and bending states (up to $r = 2.6$ mm). The results indicate that flexible InGaZnO–CNT CMOS inverter circuits are mechanically stable and function reliably, even after being subjected to multiple bending cycles. Furthermore, it was also confirmed that the more complex CMOS NAND and NOR circuits are mechanically flexible, with no device malfunction observed under bending conditions. Although characterization of standalone TFTs under bending conditions has been widely reported, this

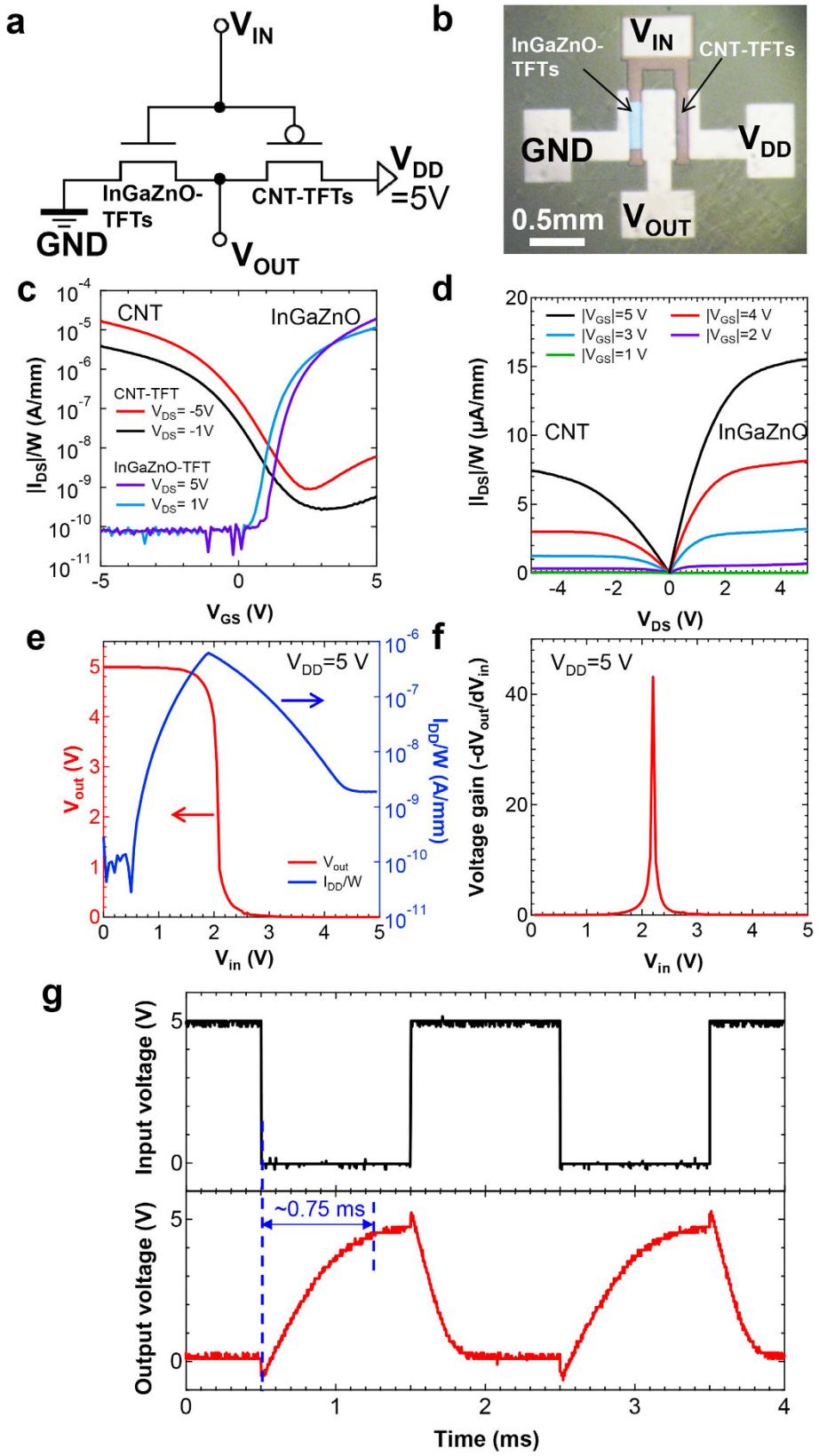

Figure 2. InGaZnO-CNT CMOS inverter. (a) Circuit diagram and (**b**) optical microscope image of a flexible InGaZnO–CNT CMOS inverter. (**c**) $I_{DS} - V_{GS}$ and (**d**) $I_{DS} - V_{DS}$ curves for n-type InGaZnO TFT and p-type CNT TFT devices. CMOS inverter characteristics: (**e**) output voltage, V_{out}, and drive current normalized with channel width (W), I_{DD}/W, and (**f**) voltage gain as a function of V_{in} at $V_{DD} = 5$ V. (**g**) Response time of a flexible CMOS inverter.

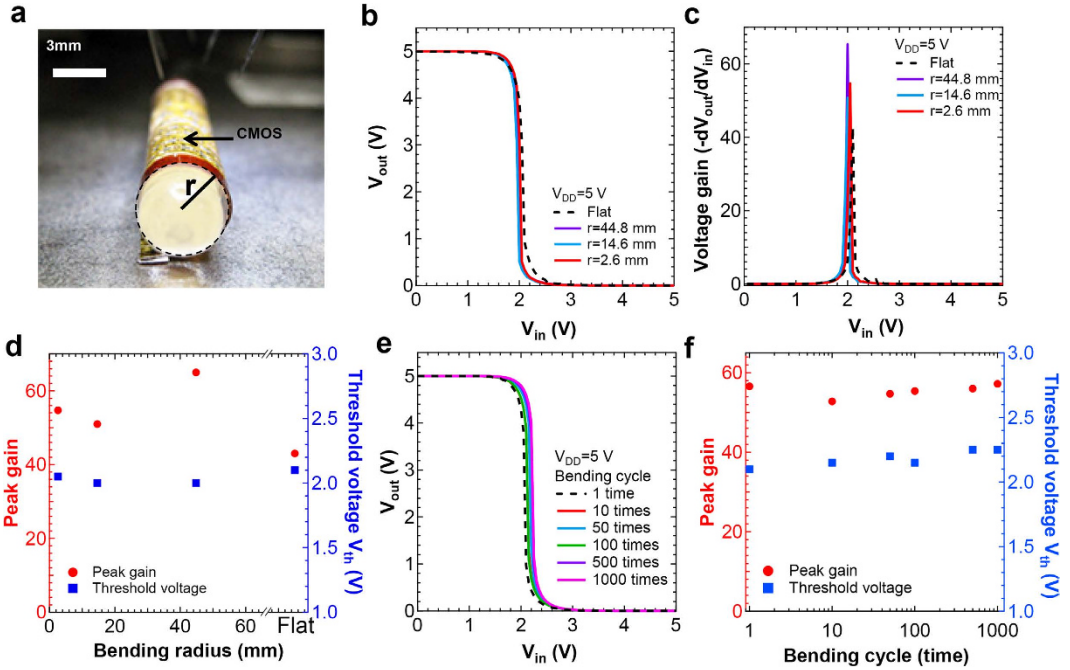

Figure 3. Mechanical properties of CMOS inverter. (**a**) Photograph of the measurement of flexible CMOS circuits and definition of bending radius, *r*. CMOS inverter characteristics of (**b**) $V_{out} - V_{in}$ and (**c**) voltage gain at flat and bending conditions (up to $r = 2.6$ mm). (**d**) Compiled peak gain and threshold voltage of the CMOS inverter as a function of bending radius extracted from (**b**,**c**). (**e**) $V_{out} - V_{in}$ properties and (f) compiled results of peak gain and threshold voltage for bending cycle tests at $r < 6$ mm for up to 1000 cycles.

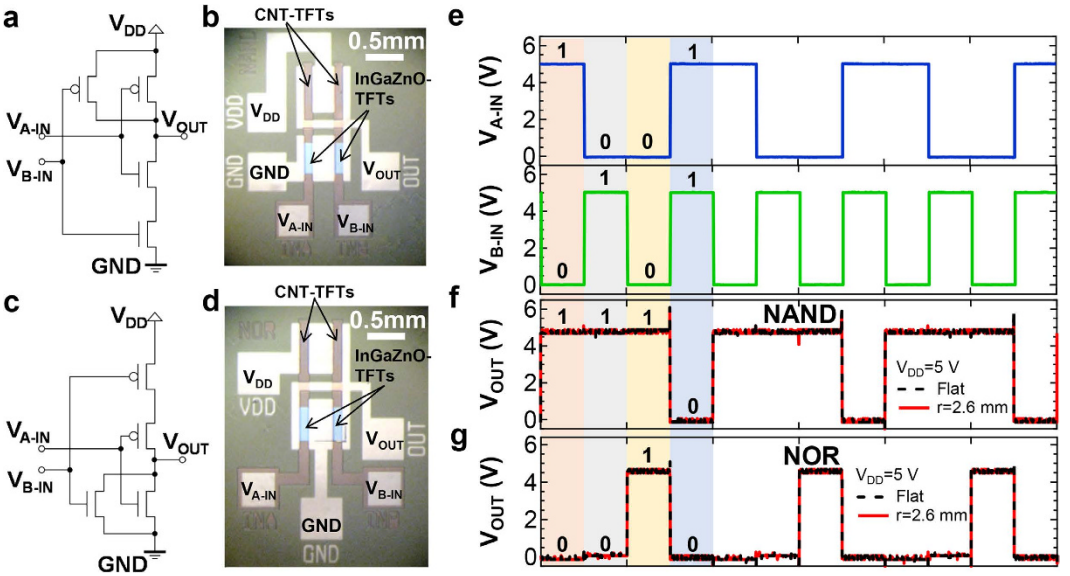

Figure 4. NAND and NOR logic circuits. (**a**) Circuit diagram and (**b**) microscope image of the flexible NAND circuit. (**c**) Circuit diagram and (**d**) microscope image of the flexible NOR circuit. (**e**) Input signal ($V_{A\text{-}IN}$ and $V_{B\text{-}IN}$) for NAND and NOR logic circuits. Represented output voltage of (**f**) NAND and (**g**) NOR circuits at the flat and bending ($r = 2.6$ mm) states when the digital input signals shown in (**e**) are applied.

is the first demonstration of the operation of flexible CMOS NAND and NOR circuits under such conditions, confirming that such components are insensitive to significant degrees of external stress. We believe that this demonstration of mechanically flexible CMOS logic circuits opens the door towards realizing low-power, high-speed, flexible CMOS systems that are likely to be key components in the next generation of portable electronic devices. Finally, next step for the practical use of flexible circuits should be the developments of both highly integrated circuits with high reliability and low-cost process.

Since the flexible devices target the macroscale electronics unlike Si-based electronics, the conventional Si-process infrastructure should not be used in terms of the fabrication cost. To address this issue, printing technique for the flexible CMOS circuits is an important role for the future flexible electronics.

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Acknowledgments

This work was partially supported by JSPS KAKENHI Grant (#26630164 & 26709026), the Mazda Foundation, Tateishi Science and Technology Foundation, and Japan Prize Foundation.

Author Contributions

K.T. conceived the idea and designed the project. W.H. conducted all device fabrication and characterization. All authors contributed to analyzing the data and discussed the results. W.H. and K.T. wrote the paper and all authors provided feedback.

Additional Information

Supplementary information accompanies this paper at http://www.nature.com/srep

Competing financial interests: The authors declare no competing financial interests.

How to cite this article: Honda, W. *et al.* Mechanically Flexible and High-Performance CMOS Logic Circuits. *Sci. Rep.* **5**, 15099; doi: 10.1038/srep15099 (2015).