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Mechanical Flip-Chip for Ultra-High Electron Mobility Devices

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Electrostatic gates are of paramount importance for the physics of devices based on high-mobility two-dimensional electron gas (2DEG) since they allow depletion of electrons in selected areas. This field-effect gating enables the fabrication of a wide range of devices such as, for example, quantum point contacts (QPC), electron interferometers and quantum dots. To fabricate these gates, processing is usually performed on the 2DEG material, which is in many cases detrimental to its electron mobility. Here we propose an alternative process which does not require any processing of the 2DEG material other than for the ohmic contacts. This approach relies on processing a separate wafer that is then mechanically mounted on the 2DEG material in a flip-chip fashion. This technique proved successful to fabricate quantum point contacts on both GaAs/AlGaAs materials with both moderate and ultra-high electron mobility.

Electrostatic gates fabricated on the sample surface are routinely used to locally deplete the two-dimensional electron gas (2DEG) in semiconductor heterostructures, in order to study the electronic behaviour in further confined geometries. The realization of the split gate in 1981¹ opened up the possibility to observe several new quantum effects in electron transport and as such generated a field of research on its own. Arguably the most famous use of split gates is the quantum point contact (QPC)², whereby a narrow constriction with a tuneable width comparable to the Fermi wavelength is fabricated on a 2DEG. This led to the observation of one-dimensional ballistic transport, a regime where the conductance g is quantized in even steps of $2e^2/h$ as a function of the constriction width. The use of QPCs has generated an enormous body of work regarding ballistic quantum transport³ and its impact on mesoscopic physics has been enormous. Nowadays, very similar fabrication techniques are used to fabricate devices tailored for the study of electronic transport in quantum dots⁴, electron interferometers⁵, and phase-coherent mesoscopic circuits⁶.

When the electron mobility in a 2DEG surpasses $\sim 10^5 \text{ cm}^2/\text{V} \cdot \text{s}$, drastic quantum effects can arise in a magnetic field, such as the Fractional Quantum Hall Effect (FQHE). This counter-intuitive phenomenon involves the two-dimensional system acquiring *fractional* effective charges, quantum statistics and quantum numbers, all driven by electron-electron interactions. This is in stark contrast with the Integer Quantum Hall Effect (IQHE) whose emergence does not involve any interactions and consequently is much more robust against disorder. While detrimental to the electronic mobility of its 2DEG, split gates fabricated on high-mobility GaAs/AlGaAs heterostructures have led to important insights. For instance, shot noise⁷ measurements were used to determine effective charges in FQHE circuits; electron interferometry with FQHE quasiparticles are now performed in Fabry-Perot⁸, and/or Mach-Zehnder⁹ interferometers which are electronic equivalent to those used in optics. A serious drawback, however, is the processing required to fabricate these gates, which results in unwanted degradation of the electron mobility. This is particularly damaging for delicate many-body quantum states such as the $5/2$ and $12/5$ FQH states. These states are unusual in that their quantum statistics is believed to emanate from a non-Abelian

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lineage¹⁰, but unfortunately their small energy many-body gaps of ~ 500 mK and 50 mK, respectively, is affected by disorder of any kind. As such, it has been difficult thus far to study these states in gated structures modulo a few *tour de force* experiments performed on the $5/2$ FQH state^{11,12}.

Methods

In order to circumvent the problem of degradation of the electronic mobility, we have developed a flip-chip technique where all processing steps required to fabricate the electrostatic gates are performed on a separate substrate that is then mounted on the surface of the 2DEG. This approach has previously been used to fabricate resonators on 2DEGs¹³ as well as for the coupling of high-frequency lines¹⁴; however, to our knowledge, split gates on high-mobility structures have never been reported using a flip-chip technique. This technique offers several advantages:

- *It avoids contamination by chemicals during the fabrication process.* Usually, the gate fabrication process uses several steps in which polymer resists are deposited on the surface of the 2DEG and chemicals are used to develop and remove these resists. Even when an appropriate solvent is used, these resist residues are hard to remove and doing so often involves a cleaning process that can damage the 2DEG (e.g. an oxygen plasma). Resist residues can also trap charges and generate undesirable fluctuations in the density of the 2DEG.
- *It avoids degradation of the electron mobility during lithography.* Radiation damage can arise from heating, electrostatic charging, ionization damages (radiolysis), displacement damage, sputtering and hydrocarbon contamination. In our approach, the 2DEG is never exposed to any electron beam or optical lithography.
- *It avoids additional strain induced by differential thermal contractions.* At room temperature, GaAs has a thermal expansion coefficient of $\alpha_L = 5.8 \times 10^{-6} \text{ K}^{-1}$. Electrostatic gates are typically made with a few nanometers of Ti ($\alpha_L = 8.6 \times 10^{-6} \text{ K}^{-1}$) and/or Cr ($\alpha_L = 4.9 \times 10^{-6} \text{ K}^{-1}$) adhesion layer, and most often with tens of nanometers of gold ($\alpha_L = 14 \times 10^{-6} \text{ K}^{-1}$) or aluminium ($\alpha_L = 23.1 \times 10^{-6} \text{ K}^{-1}$). These coefficients do not vary much from ~ 300 K down to 150 K and eventually become negligible at low temperatures. For a typical 2 mm wide gate made out of gold, the gate will shrink by approximately $4 \mu\text{m}$ during the first 150 K, whereas GaAs will shrink by less than $2 \mu\text{m}$. This is likely to induce strain in the material and to affect the electron mobility at low temperatures, particularly in the case of a narrow constriction with a width of only 500 nm.
- *It makes it possible to re-use the 2DEG material.* The technique is non-destructive and enables the re-use of the 2DEG material at will. In addition, for the highest mobility GaAs/AlGaAs 2DEGs with mobility in excess of $30 \times 10^6 \text{ cm}^2/\text{V} \cdot \text{s}$, it is known that different parts of the wafer may have different mobilities as well as fluctuations in the electron density. Since several types of gated devices have active areas of a few μm^2 only, should the need arise, our approach allows for the device to easily be remounted on a slightly different part of the wafer. This technique also allows one to swap gates so as to measure different devices (or designs) on the exact same piece of material. Finally, it avoids wasting precious material during low-yield processes, which is common when fabricating complex devices.

Results

In Fig. 1 we show the conventional (panels a–c) and flip-chip (panels d–h) fabrication processes of a QPC. In the traditional approach, the gates are fabricated directly on top of the 2DEG material using a combination of e-beam and optical lithography. In contrast, the flip-chip technique uses a sapphire plate where all the processing is performed through a conventional e-beam lithography process, with 50 nm of chromium first deposited to allow charge evacuation during the e-beam exposure followed by a spinning of MAA/PMMA resist. After exposure and development, 5/150 nm Ti/Au is deposited by e-beam evaporation followed by lift-off and chromium etching. Extreme care is taken to obtain a near perfect lift-off so as to prevent residual metal standing up along the edge, which could cause gate leakage or introduce an undesirable buffer space between the flip-chip gates and the 2DEG. A layer of aluminum oxide (30 to 100 nm thick) is then deposited to further prevent potential gate leakages. The ohmic contacts are fabricated directly on the GaAs/AlGaAs either by indium diffusion, or by evaporation of Ge/Au/Ni/Au using shadow mask to avoid lithography. The 2DEG wafer is placed on a sample holder and the ohmic contacts are connected to the contacts of the holder by indium-soldered gold wires. Then, the flip-chip is placed on top of the 2DEG together with an additional sapphire top plate, which is itself held in place by four BeCu springs that apply very gentle mechanical pressure. The optical interference fringes between the top plate and the flip-chip allow a fine tuning in the alignment of the flip-chip device. All fabrication and assembly steps are performed in a class-100 cleanroom to avoid contamination of the critical interfacing surfaces.

We have fabricated both $1 \mu\text{m}$ long QPC and Fabry-Pérot gates on sapphire and tested the technique on GaAs/AlGaAs wafers grown at Sandia National Laboratories (Sample A) as well as Princeton University (Sample B). We have chosen to compare the flip-chip devices with the best conventional QPC fabricated out of 20; in many cases, the conductance quantization were not as good as for the flip-chip devices. For the flip-chips mounted on sample A, several QPCs showed pinch-off with a success rate of

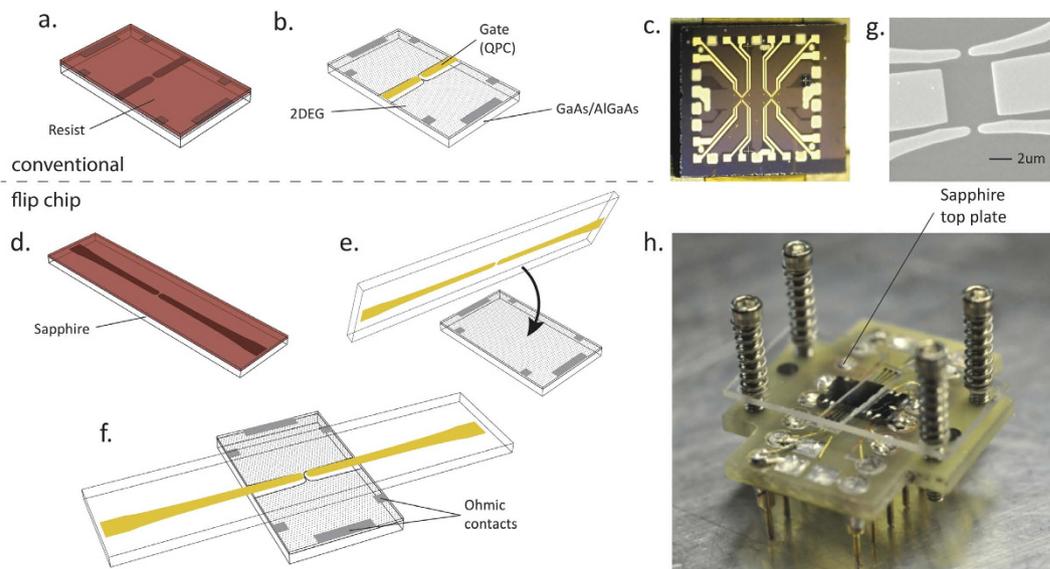


Figure 1. Top panels: conventional process. In (a,b) the lithography is performed directly on the 2DEG wafer. A photograph of a typical device is shown in (c). Bottom panels: the flip-chip process. (d) e-beam lithography is performed on a sapphire substrate and then (e) the metallic gates are brought into proximity of the 2DEG by a flip-chip process. The final assembly is shown in (f). Photographs of the central part of the gates as well as of the whole device are shown in (g) and (h), respectively.

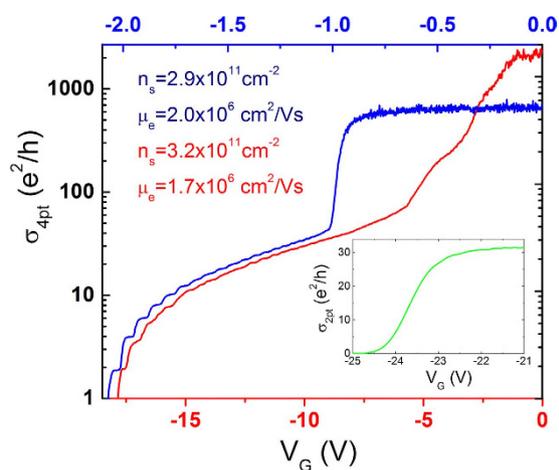


Figure 2. Conductivity across the 2DEG as a function of gate voltage (blue, top axis) applied on the conventional QPC, and on the FCQPC (red, bottom axis, sample A). The inset shows a pinch off of a FCQPC at 4 K fabricated on an ultra-high mobility 2DEG wafer (sample B).

~80%. In total, more than 20 devices were tested and a pinch-off voltage ranging from -6 V to -40 V was determined. For comparison, conventional QPCs (CQPCs) made on a similar wafer to sample A showed a pinch-off voltage ranging from -1.7 to -3 V , and thus had a superior gate efficiency by a factor ranging from ~ 3 to 13 . We attribute the lower gate efficiency of the Flip chip QPC (FCQPC) to the ‘air’ (vacuum) gap between the flip-chip and the 2DEG. A rough calculation that assumes a pinch-off voltage scaling linearly with the distance between gates and the 2DEGs estimates this gap to be in the range from 50 to 200 nm . This gap most likely occurs because the contact area between the 2DEG and the flip-chip gates is over $3.6 \times 2 \text{ mm}^2$ in area and not perfectly flat; this could easily be improved by reducing the contact area between the two mechanical parts of the device.

Figure 2 provides a typical example of the conductivity versus pinch-off gate voltage on a logarithmic scale for both a flip-chip QPC (red) and a conventional QPC (blue). The data were taken at 25 mK using a similar 2DEG GaAs/AlGaAs heterostructure with a moderate mobility of $2 \times 10^6 \text{ cm}^2/\text{V} \cdot \text{s}$ (although not coming from the exact same wafer). For both devices, the quantization of the conductance is clearly

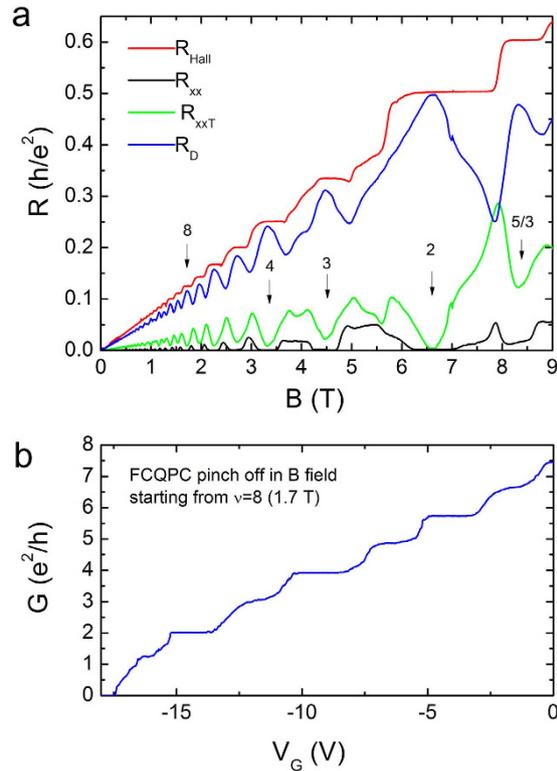


Figure 3. (a) Hall resistance (R_H), longitudinal resistance outside (R_{xx}) and through (R_{xxT}) the FCQPC, as well as the diagonal resistance R_D (mixing of R_H and R_{xxT}) versus the magnetic field measured on sample A. Clear QHE and FQHE features (such as the 5/3 FQH state) can be observed. (b) Diagonal conductance across the QPC at 1.7 T magnetic field versus gate voltage.

observed. While the CQPC shows better-defined and more precise conductance plateaus (ballistic behaviour), this likely arises from the shape of the QPCs that were not identical, and because of both the air gap present in the FCQPC and shallowness of the 2DEG modifying the gate-induced electric field profile. We also note that in the metallic regime at conductance below $\sim 50 e^2/h$, the slopes of the FCQPC and CQPC are strikingly similar. Importantly, we have not observed a pronounced hysteresis in the pinch-off curve of the FCQPC whereas this undesirable behaviour is often observed in conventional gated devices. Finally, in the inset of Fig. 2 the conductance of a FCQPC integrated with an ultra-high mobility ($\mu \sim 1.0 \times 10^7 \text{ cm}^2/\text{V} \cdot \text{s}$) GaAs/AlGaAs 2DEG and measured at 4 K is shown. Albeit with a lower gate efficiency, this data demonstrates that the flip-chip process can be integrated with the highest mobility 2DEG materials.

As further confirmation of the quality and efficiency of the flip-chip devices, they were characterized in the quantum Hall regime at very low temperatures in a magnetic field up to 9 T. Figure 3a shows the measured resistance in various configurations within sample A. The Hall resistance R_H measured outside of the interferometer (red trace) shows good quantization of the IQH plateaus and the 5/3 FQH plateau, as expected for a sample in this range of mobility. Due to the geometry of our design, it is not possible to directly measure R_H under the interferometer; rather, we measure the diagonal resistance R_D (blue trace), which includes a large longitudinal contribution. Also shown are R_{xx} outside of the interferometer and R_{xxT} through the interferometer; again geometry plays a role, since the contacts outside are much closer together and the measured voltage is correspondingly smaller. The fact that R_{xxT} does not reach zero in all of the states and that R_{xx} does may be due to the flip-chip blocking light from the LED used during the cooling process or to the non-ohmicity of particular contacts. Further investigation is required to clarify this. Finally, we note that in the quantum Hall regime the conductivity is related to the resistivity by the tensor relations $\sigma_{xx} = \rho_{xx}/(\rho_{xx}^2 + \rho_{Hall}^2)$ and $\sigma_{Hall} = \rho_{Hall}/(\rho_{xx}^2 + \rho_{Hall}^2)$. As a consequence, it is difficult to extract them in our case because they require the measurement of both R_{Hall} and R_{xx} in all regions of the sample in a well-controlled geometry, which is not the case here.

In Fig. 3b, the conductance is shown as a function of gate voltage at a magnetic field of 1.7 T, near filling factor $\nu=8$. Plateaus occur for each integer multiple of e^2/h , with the exception of the first plateau. The quantization for the lowest conductance plateaus (2, 3, 4) is excellent, but degrades for higher plateaus as the contribution of the longitudinal resistance in series with the QPC becomes significant. Along with the data in Fig. 3a, these results clearly show that the device can operate in a magnetic field and is mechanically stable up to 9 T at 20 mK.

In conclusion, we have demonstrated successful fabrication of split-gate devices on GaAs/AlGaAs 2DEG heterostructures using a flip-chip technique which avoids performing any potentially damaging fabrication steps directly on the ultra-high mobility wafer. This process has a yield on par with traditional fabrication techniques, and results in robust devices that can be measured at dilution refrigerator temperatures and in high magnetic fields. Benchmark measurements show that the samples perform as expected; we demonstrate pinch-off and quantized conductance both at zero field and in the quantum Hall regime. These devices have great potential for future studies of sensitive quantum Hall states such as interferometric measurements with the $5/2$ and $12/5$ FQHE that occur only in pristine ultra-high mobility devices.

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Author Contributions

G.G. provided the flip-chip conceptual idea. K.B. made the design, the implementation of the idea, and the fabrication. D.L. and S.G. assisted with the microfabrication. K.B., S.G. and B.S. performed the transport measurements and the analysis. S.G. made figure 1. M.L., J.R., K.W. and L.P. performed the growth of the wafer materials. K.B., B.S. and G.G. co-wrote the manuscript and all authors reviewed the manuscript.

Additional Information

Competing financial interests: The authors (K.B.) and (G.G.) disclose that there is potential competing interest since a patent has been filed regarding the work described in this manuscript. Should the commercialization be successful, these authors would receive a financial return. All other authors declare no competing financial interests.

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