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Vertical Bipolar Charge Plasma Transistor with Buried Metal Layer

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A self-aligned vertical Bipolar Charge Plasma Transistor (V-BCPT) with a buried metal layer between undoped silicon and buried oxide of the silicon-on-insulator substrate, is reported in this paper. Using two-dimensional device simulation, the electrical performance of the proposed device is evaluated in detail. Our simulation results demonstrate that the V-BCPT not only has very high current gain but also exhibits high $BV_{CEO} \cdot f_T$ product making it highly suitable for mixed signal high speed circuits. The proposed device structure is also suitable for realizing doping-less bipolar charge plasma transistor using compound semiconductors such as GaAs, SiC with low thermal budgets. The device is also immune to non-ideal current crowding effects cropping up at high current densities.

Bipolar transistors are widely used in the design of current mirrors, amplifiers and band-gap voltage reference in many high speed mixed signal circuits. Lateral bipolar transistors on SOI have been found to be of great interest with the advent of BiCMOS technologies[1–3]. However, lateral bipolar transistors on SOI suffer from lower cut-off frequency and lower current gain due to the difficulty in realizing a narrow base width. In vertical bipolar transistors, shallow junction depths can be easily realized by controlling the diffusion, ion implantation and epitaxial growth processes. A number of recent publications demonstrate great advancements in vertical complementary BiCMOS[4–5] as well. A highly scaled 3-D vertical n-p-n bipolar junction transistor (V-NPN BJT) resistive-switching random access memory cell[6] has been experimentally implemented for ultra-high density and low voltage applications. V-NPN BJT provided through a BiCMOS process has also been used for realizing a transducer design with large transconductance g_m, low-noise and high linearity[7] for applications in RF and analog circuits. Recently, the series collector resistance of the bipolar transistors has been considerably reduced by incorporating a highly conducting buried silicide layer[8–11] between the top silicon layer and the buried oxide layer (BOX) of silicon-on-insulator substrates.

A number of metal layers such as tungsten[8–10], cobalt[12], molybdenum[13] and others have been incorporated by bonding technology with low thermal budgets. However, in aggressively scaled devices, dopant fluctuation[14–15] and dopant activation[16] of the highly doped emitter and the base region of the BJT with high thermal budgets can be a bottleneck while integrating the bipolar process with the CMOS process on SOI incorporating a buried metal layer.

Recently, a lateral doping-less bipolar transistor (Bipolar Charge Plasma Transistor) based on the charge plasma concept has been reported[17] as shown in Fig. 1(a). In this transistor, n-type and p-type regions are created by inducing electron and hole plasma into the undoped silicon film using metal electrodes of appropriate work functions. For creating the emitter and the collector region, the work functions of the metal electrodes $\phi_{M,E}$ and $\phi_{M,C}$, respectively, should be less than the work function ϕ_{Si} of the Si film. For creating the p-base region, a metal electrode with a work function $\phi_{M,B} > \phi_{Si}$ is chosen. Neither ion implantation nor impurity atoms are diffused into the intrinsic silicon to form the emitter, base and the collector regions. The absence of the doped regions makes this device obviate the need for complicated thermal budgets required for the conventional bipolar transistors. As shown in Fig. 1 (b), the induced carrier concentration is maintained in the BCPT under thermal equilibrium as well as under forward active bias conditions. Since the BCPT is a lateral structure, it exhibits a low cut-off frequency as compared to its conventional counterpart, as shown in Fig. 1 (c). Further, in a lateral BJT, it is difficult to control the base width, whereas, thin base widths can be easily realized in vertical BJTs.

In this paper, we present a detailed study of a doping-less vertical bipolar charge plasma transistor (V-BCPT) with a buried metal layer on intrinsic silicon[17–28]. The novel feature of the proposed structure compared with the lateral bipolar transistor sturctures[17,20,22,23] is that it is a self-aligned vertical device with a buried metal layer. We demonstrate that the proposed V-BCPT exhibits a high current gain and a large $BV_{CEO} \cdot f_T$ product required in analog circuit applications. In the V-BCPT structure, without the need for dopant diffusion, the "n^+" emitter, "n"

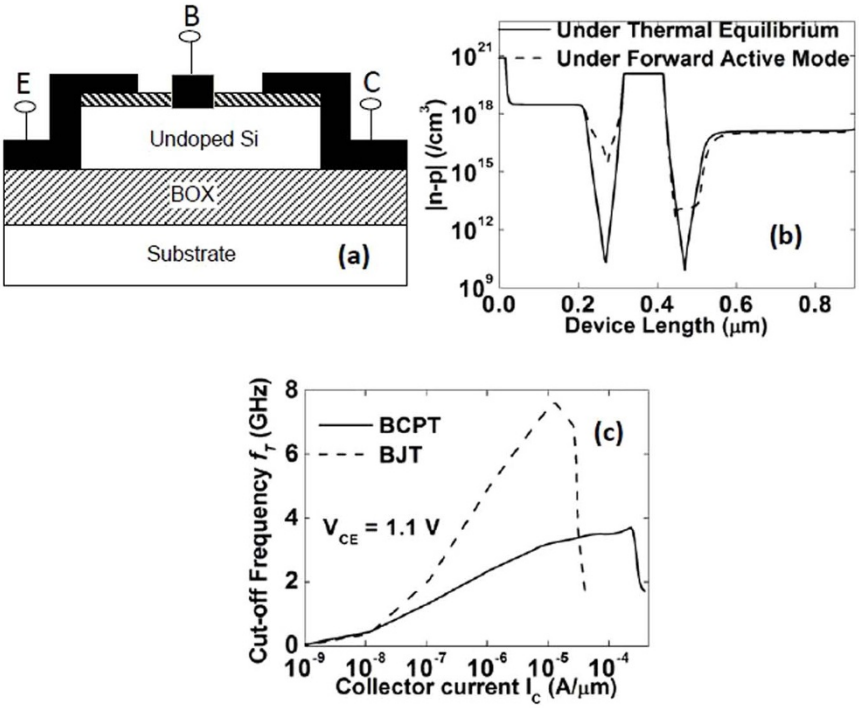

Figure 1 | (a) Schematic cross-section, (b) net carrier concentration and (c) cut-off frequency of the lateral BCPT.

collector and the "p" base are induced in the intrinsic silicon body by choosing the emitter, collector and the base metal electrodes with suitable work functions.

The proposed device structure can have potential applications in realizing BCPT using compound semiconductor materials such as GaAs and SiC. Using 2-D-simulations, we demonstrate that the V-BCPT not only exhibits a significantly higher current gain β and cut-off frequency f_T, but also is immune to current crowding effect arising at the emitter edges at high collector current densities.

Device Structure and Parameters

The cross-sectional view of the V-BCPT is shown in Fig. 2 along with the induced electron and hole distribution under thermal equilibrium conditions. In the V-BCPT, the electron plasma is induced in the undoped Si film to create the emitter region by employing Hafnium (work function $\varphi_{m,E}$ = 3.9 eV) as the emitter electrode metal. A stack of TiN/$HfSiO_x$/SOI doped with Fluorine (work function $\varphi_{m,B}$= 5.4 eV)[29] is used as the base electrode to induce hole plasma to create the base region with a non-uniform hole distribution. Substrate bias can be used during the emitter and base metal sputtering to avoid the possibility of silicide formation[30]. Since we need a lower electron concentration in the collector region compared to what is required in the emitter region of the transistor, Aluminum (work function $\varphi_{m,C}$ = 4.28 eV) is used as the collector electrode buried between the silicon and BOX of the SOI. This buried aluminum electrode (as described in section IV) can be formed using wafer bonding techniques[8–13]. Although the Si film is intrinsic, we have assumed it to be un-intentionally doped with $N_D = 1 \times 10^{14}/cm^3$. A gap ($L_S$) of 10 nm separates the emitter from the base metal electrodes on either side of the emitter electrode.

Simulations are performed with the ATLAS device simulation tool [ATLAS Device Simulation Software, Silvaco Int., Santa Clara, CA, 2014.] using the Fermi-Dirac distribution of carrier statistics with Philip's unified mobility model[31], all with default silicon parameters. The simulator uses a set of fundamental equations, which link together the electrostatic potential and the carrier densities. These equations are derived from Maxwell's laws and consist of Poisson's Equation, the continuity equations and the transport equations. The conventional drift-diffusion (DD) model is used for carrier transport. The standard thermionic emission model [*ATLAS Device Simulation Software*, Silvaco Int., Santa Clara, CA, 2014.] is invoked for the emitter contact of the V-BCPT with a surface recombination

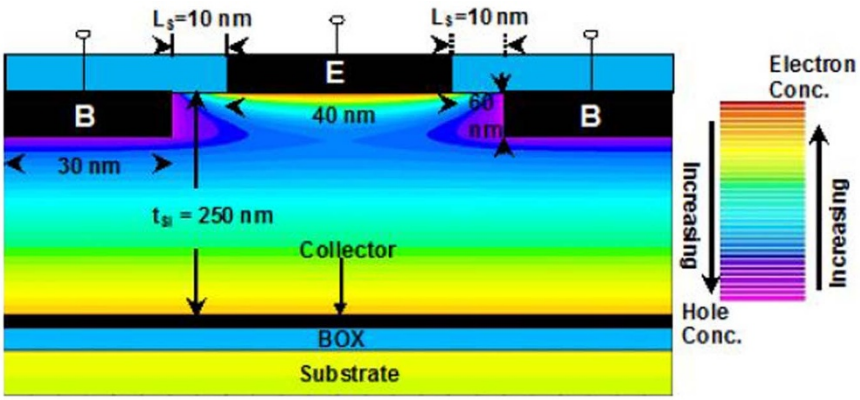

Figure 2 | **Schematic cross-sectional view of the V-BCPT.**

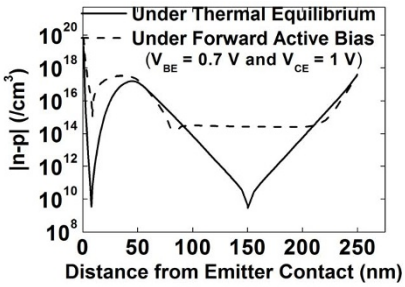

Figure 3 | Simulated net carrier concentrations in the V-BCPT for different bias conditions.

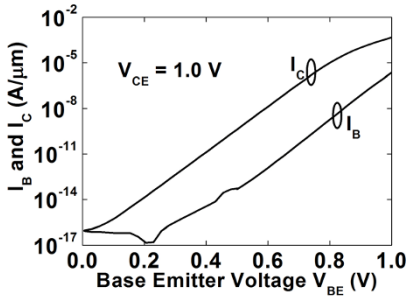

Figure 4 | Gummel plots of the V-BCPT.

velocity of 2.2×10^6 cm/s and 1.6×10^6 cm/s for electrons and holes, respectively. Similarly, ideal ohmic contacts have been assumed in the charge plasma diode[18] simulations. The results of the fabricated CP diode[19] indicate that the contact resistance does not seriously affect the device performance if appropriate care is taken during the electrode formation. It may be noted that we have not considered Fermi level pinning and the barrier lowering effects in our simulations. To account for the impact ionization, Selberherr's model[32] is invoked. For recombination, we have, enabled Klaassen's model for concentration-dependent lifetimes for Shockley-Read-Hall (SRH) recombination with intrinsic carrier lifetimes $n_{ie} = n_{ih} = 0.2\ \mu s$[33]. High electric-field velocity saturation is modelled through the field-dependent mobility model [ATLAS Device Simulation Software, Silvaco Int., Santa Clara, CA, 2014.]. The screening effects in the inversion layer are also considered by invoking the Shirahata mobility model[34].

Results

The electron and hole concentrations for the V-BCPT along the y-axis (cutline taken at the edge of the emitter electrode) under thermal equilibrium and forward active bias are shown in Fig. 3. The induced free carrier concentrations are maintained in the emitter, base and

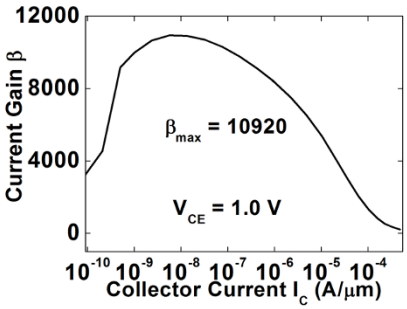

Figure 6 | Current gain variation of the V-BCPT.

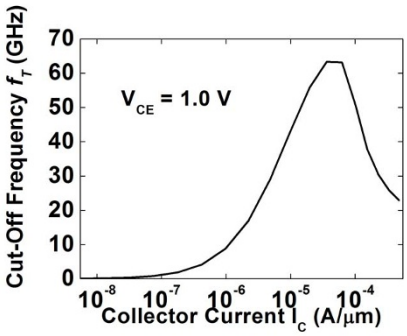

Figure 7 | Cut-off frequency of the V-BCPT.

collector regions either under thermal equilibrium ($V_{BE} = 0$ V and $V_{CE} = 0$ V) or the forward active bias condition ($V_{BE} = 0.7$ V and $V_{CE} = 1$ V). As can be seen in Fig. 3, for the given bias conditions, due to the direct metal-semiconductor contact, the net carrier concentration is higher near the metal-Si interface. Under thermal equilibrium conditions, the base-emitter and the base-collector junction are clearly well delineated. Under forward active bias conditions, the injected carrier concentration goes up at the base-emitter junction. Also, the net electron concentration in the base-collector depletion region increases due to the finite collector current flowing through the device. The Gummel plots in Fig. 4 indicate that the base current of the V-BCPT is almost two orders lower in magnitude compared to its collector current. The low base current of the V-BCPT structure is because of the accumulation of electrons at the metal-semiconductor interface of the emitter. Fig. 5(a) shows the accumulated electron concentration under the emitter contact along the Y-axis. As explained in literature[17,35,36] the electrons accumulate when a low work function metal is contacted to the n-type emitter. As shown Fig. 5(b), this accumulation of electrons results in an electric field, leading to the retardation of the holes injected from the base region. As a result the concentration gradient of the holes injected into the

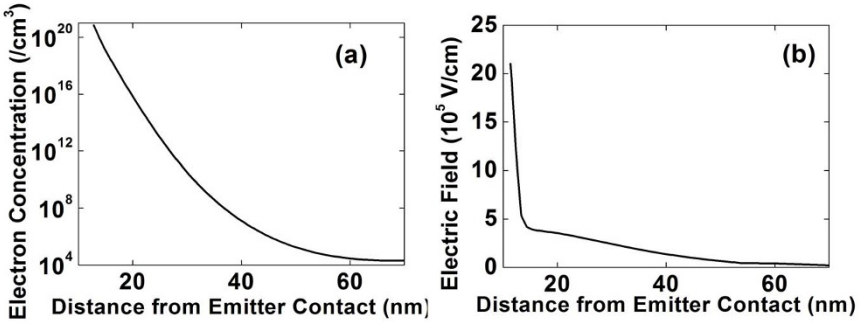

Figure 5 | (a) Electron Concentration and (b) electric field distribution in the emitter region of the V-BCPT.

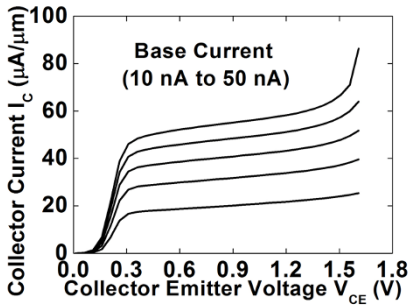

Figure 8 | **Output characteristics of the V-BCPT.**

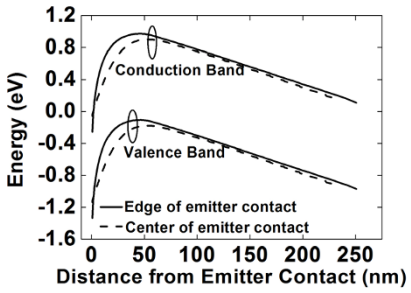

Figure 10 | **Energy band diagram of the V-BCPT taken along the Y-axis.**

emitter decreases and resulting in a low base current as shown in Fig. 4. Consequently, the current gain β of the V-BCPT is very high as shown in Fig. 6, with an approximate peak value of 10,000.

The cut-off frequency of the transistor is an important figure of merit to characterize the frequency response of the bipolar transistors. It is defined as $f_T = \sqrt{g_m/2\pi C}$ where, g_m is the transconductance and C is the sum of the emitter-base depletion capacitance, the base-collector depletion capacitance and the emitter-base diffusion capacitance. By performing the AC analysis, the simulator first calculates the electrode capacitances and the transconductance, and then gives the cut-off frequency of the device for the given bias conditions. The peak cut-off frequency of the V-BCPT (Fig. 7) is $\sim$ 63 GHz which makes it suitable for mixed signal circuits. This improvement in the cut-off frequency compared to that of the lateral BCPT[17] is due to 1) less transit time of the carriers due to a thinner base and 2) high transconductance[20]. The $BV_{CEO} \cdot f_T$ product is considered to be a figure of merit of the BJTs. The V-BCPT has a high $BV_{CEO} \cdot f_T$ product of 126.6 V-GHz (at $BV_{CEO} = 2$ V). The output characteristics of the V-BCPT are shown in Fig. 8. We observe from Fig. 8 that for different base currents, the collector current does not increase uniformly indicating that the gain of the device is varying with increasing base current. It is due to the high injection effects at high collector currents because of which the collector current does not increase at the same rate as it does for lower base currents. Therefore, the current gain of the device decreases similar to what happens in conventional BJTs. Our simulation results show that the breakdown voltage of the V-BCPT is lower than that of the conventional vertical BJTs and this is due to the high current gain exhibited by the V-BCPT[36].

When current crowding occurs, most of the emitter current flows through the emitter edges into the base region, leaving most of the central emitter area inactive. However, from the current contour plot of the total current density of the V-BCPT shown in Fig. 9, it is observed that in the V-BCPT, most of the current is flowing through the middle of the emitter region rather than at the edges. This is due to the non-uniform concentration of the induced holes along the X-axis away from the base electrodes. This leads to a lower built-in-potential barrier (Fig. 10) and hence an increase in the current flow at the middle of the emitter region as compared to the edges as can be observed in Fig. 9. Consequently, majority of the current passes through the middle of the device making it immune to current crowding at the emitter edges as observed in conventional BJTs at high current densities. One advantage of the V-BCPT structure is the realization of lateral variation in the concentration of the holes in the base region which is not possible to obtain in a conventional BJT.

One distinguishing feature of the V-BCPT compared to the conventional BJT is the presence of the metal-semiconductor junction at the emitter and the base contacts. Depending on the surface preparation and metal deposition methods, the possibility of having both donor and acceptor type of traps[37] at these metal-semiconductor junctions cannot be overruled. The trap concentration can be as large as $10^{11}/cm^2$ and their presence can affect the current gain as demonstrated in literature[17,35].

To simulate the influence of traps on the current gain, we have considered both the types of traps with the trap energy level (E.level) at 0.49 eV from the conduction (or valance) band[35]. The degeneracy factor (degen) is 12[35,38] and the capture cross sections for electrons (sign) and holes (sigp) are $2.85 \times 10^{-15}/cm^2$ and $2.85 \times 10^{-14}/cm^2$ [35], [ATLAS Device Simulation Software, Silvaco Int., Santa Clara, CA, 2014.] respectively.

With the increase in the trap density, the base current of the V–BCPT goes up and as a result, a decrease in the current gain of the V-BCPT is observed as seen in Fig. 11. However, the peak current gain of the V-BCPT is substantially high even for a trap density of $10^{11}/cm^2$. As is the practice in most advanced fabrication procedures, the surface preparation should be well regulated to control the

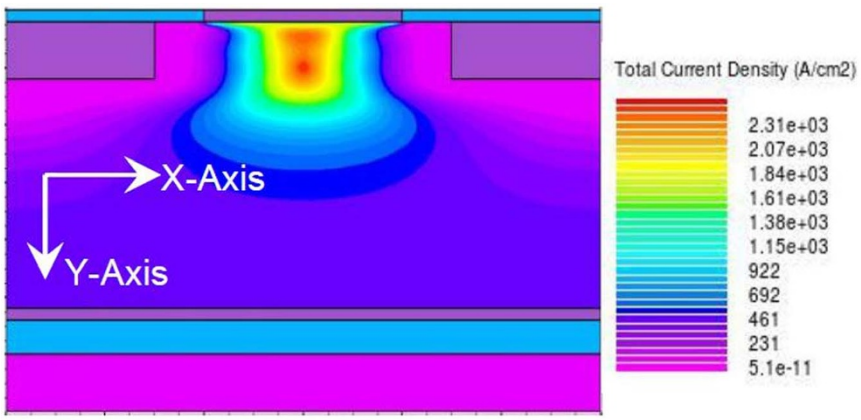

Figure 9 | **Contour plot of total current density of the V-BCPT for $V_{BE} = 0.7$ V and $V_{CE} = 1$ V.**

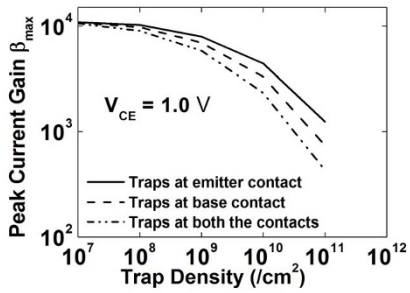

Figure 11 | **Peak current gain versus trap density for the V-BCPT.**

density of traps at the metal-semiconductor junction. The effect of surface traps will minimize[35,39] by inserting a native oxide ~10–15 Å between the metal-semiconductor contacts.

Discussion

In this paper, a doping-less vertical bipolar transistor with a buried metal layer on SOI is reported. The V-BCPT with Aluminum as the buried metal layer can be realized with low thermal budgets. 2-D simulation results of the V-BCPT indicate excellent electrical performance in terms of high current gain, cut-off frequency and $BV_{CEO} \cdot f_T$ product. It is also observed that the proposed device is immune to current crowding effect at the edges of the emitter at high collector current densities. Our results may provide the incentive for further experimental exploration of the V-BCPT concept.

Methods

Fabrication. The possible fabrication steps of the V-BCPT are schematically shown in Fig. 11. First, clean the starting device Si wafer and the handle Si wafer (Fig. 12 a) by a standard RCA process. Remove the native oxide on the Si surface by diluted HF solution and after that immediately sputter Al metal to form a 100 nm-thick layer on the Si substrate. Use plasma assisted room temperature bonding technology[13] to bond the device Si wafer against the handle Si wafer with a 50 nm thick top oxide layer (Fig. 12 b). Anneal the bonded wafers at 200°C for 2 hours to increase the bond strength. Thin down the top silicon layer to 250 nm thickness.

On top of this silicon film, sputter a 10 nm thick Hafnium metal layer followed by the deposition of an oxide layer (200 - 350°C) by plasma enhanced chemical vapour deposition (PECVD) (Fig. 12 c). Hf silicidation takes place in the 600–765°C temperature range[40]. Care must be taken so that the subsequent process temperature does not exceed the above temperature range. Form a 40 nm long emitter electrode by patterning and etching (Fig. 12 d). Following this step, deposit a good quality conformal low temperature oxide layer (Fig. 12 e) and use reactive ion etching to form a sidewall spacer oxide of 10 nm thickness on either side of the emitter electrode (Fig. 12 f). Etch the silicon to a depth of 60 nm on either side of the emitter electrode by RIE (Fig. 12 g). Next, sputter the base metal (Fig. 12 h) and pattern it (Fig. 12 i). By chemical mechanical polishing and followed by the deposition of a passivation oxide layer, the proposed structure as shown in Fig. 2 can be obtained. Collector electrode can be contacted by opening a trench in the silicon film and by sputtering Al metal as shown in Fig. 12 j. Using the suggested fabrication process, a self-aligned vertical bipolar charge plasma transistor with a buried metal layer can be realized.

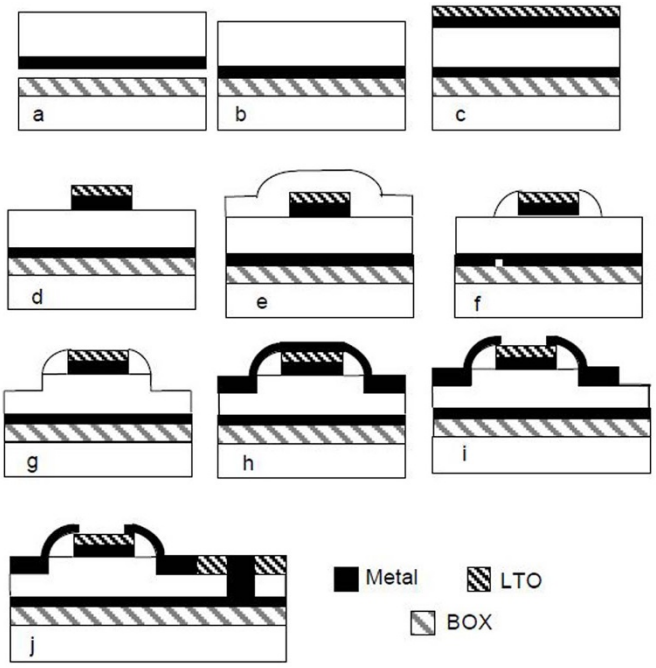

Figure 12 | **Possible fabrication process of the V-BCPT.**

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Author contributions

M.J.K. conceptualized and directed the project. K.N. carried out the simulations. All analyzed the data and co-authored.

Additional information

Competing financial interests: The authors declare no competing financial interests.

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