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## Roll-to-roll fabrication of large scale and regular arrays of three-dimensional nanospikes for high efficiency and flexible photovoltaics

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Three-dimensional (3-D) nanostructures have demonstrated enticing potency to boost performance of photovoltaic devices primarily owning to the improved photon capturing capability. Nevertheless, cost-effective and scalable fabrication of regular 3-D nanostructures with decent robustness and flexibility still remains as a challenging task. Meanwhile, establishing rational design guidelines for 3-D nanostructured solar cells with the balanced electrical and optical performance are of paramount importance and in urgent need. Herein, regular arrays of 3-D nanospikes (NSPs) were fabricated on flexible aluminum foil with a roll-to-roll compatible process. The NSPs have precisely controlled geometry and periodicity which allow systematic investigation on geometry dependent optical and electrical performance of the devices with experiments and modeling. Intriguingly, it has been discovered that the efficiency of an amorphous-Si (a-Si) photovoltaic device fabricated on NSPs can be improved by 43%, as compared to its planar counterpart, in an optimal case. Furthermore, large scale flexible NSP solar cell devices have been fabricated and demonstrated. These results not only have shed light on the design rules of high performance nanostructured solar cells, but also demonstrated a highly practical process to fabricate efficient solar panels with 3-D nanostructures, thus may have immediate impact on thin film photovoltaic industry.

hin film photovoltaics (PVs) are highly attractive for low cost solar energy conversion. In addition, potency of thin film solar cells to be made with remarkably light weight and excellent flexibility enables a wide range of applications in different scale from building-integrated photovoltaic generation to portable electronics. Nevertheless, due to utilization of ultra-thin material with limited light absorption capability and typically low crystalline quality, poor performance of thin film solar cells has placed them in a disadvantageous situation when competing with crystalline Si based solar cells. Meanwhile, the competition between light absorption and carrier collection in conventional type of planar thin film solar cells makes further performance boost a challenging and fundamentally intriguing research topic1-3. Recent studies have revealed that nanostructured substrates/templates can benefit performance of thin film solar cells, via introducing advanced light management schemes, such as photonic and/or plasmonic light trapping, and unique device design to improve minority carrier collection efficiency<sup>2-9</sup>. Although a number of different types of nanostructures, such as nanodome<sup>10</sup>, nanocoax<sup>11</sup>, nanorod<sup>12</sup> and nanopillars<sup>2,13</sup>, etc., have been proven effective in this regard, there is still a lack of fundamental understanding on how morphological and structural change will affect the trade-off between photon absorption and carrier collection in a thin film solar cell device. This is in fact crucial in order to develop rational design guidelines for high efficiency solar cell devices. Moreover, from a practical standpoint, a cost-effective and scalable scheme to fabricate desirable nanostructures on flexible substrates is of an urgent need. In this work, a low-cost process has been developed to fabricate perfectly ordered arrays of 3-D NSPs on flexible Al substrates. These 3-D NSPs were formed with a unique defect nanoengineering approach in conjunction with scalable Al anodization, and they have well controlled geometries, *i. e.* pitch and height. After Achieving NSP structures, *p-i-n* junction amorphous-Si (a-Si) thin films were used as model materials deposited on 3-D structures with different combinations of

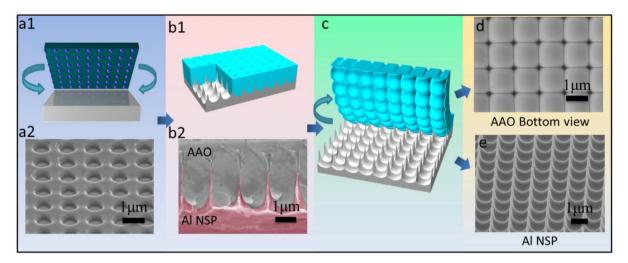


Figure 1 | Fabrciation process of 3-D nanospike. (a1–a2) Schematic diagram of nanoimprint process on flat Al foil with a silicon stamp and SEM image of a imprinted aluminum foil. (b1–b2) Schematic diagram and SEM image of NSP under squarely ordered AAO after anodization (Al NSP is indicated with red false color in b2). (c) Schematic of AAO removal to expose NSP underneath. (d) SEM of bottom view of squarely order AAO. (e) SEM of perfectly ordered Al NSP array.

height and pitch to implement 3-D solar cell devices. Then systematic characterizations on device optical absorption and electrical performance were carried out, assisted with optical and device simulations in order to gain further understanding. In brief, it has been discovered that 3-D architecture does improve light absorption in the active material, with the effectiveness monotonically depending on aspect ratio. However, high aspect ratio compromises uniformity of a-Si coating on the nanostructures which adversely affects building potential in the thin film thus hurts carrier collection eventually. Through systematic experiments and simulations, an optimal 3-D structure was identified to achieve a good balance between light absorption and carrier collection, yielding as high as 43% improvement on power conversion efficiency from a planar counterpart. Furthermore, a roll-to-roll compatible nanostructure fabrication process was successfully demonstrated and 3-D flexible thin film solar cells were fabricated in a relatively large scale with respectable efficiency. These investigations have not only exemplified the critical necessity of the coupled optical/electrical design for device performance optimization and shown a set of generic guidelines, but also demonstrated a highly practical and scalable technological platform to develop a new generation of high efficiency thin film solar cells based on various materials.

Fabrication of irregular 3-D NSP arrays on aluminum has been developed by us previously and the structures have demonstrated excellent photon capturing capability after coating with photovoltaic materials<sup>14</sup>. However, irregularity on periodicity and height of NSPs may introduce large variation on the coated film thickness. This may not significantly affect device optical absorption as it is typically measured in average, whereas it is detrimental for photovoltaic performance which is sensitive to local variation of junction depth<sup>15</sup>. In this regard, a facile approach has been developed to fabricate highly regular arrays of 3-D NSPs. Figure 1 demonstrates the schematics and the corresponding scanning electron microscopy (SEM) images of the process flow to fabricate a regular 3-D NSP array. It started with nanoimprint of squarely ordered nano-indentation on a clean and flat Al foil using a silicon nanoimprint master, as illustrated in Fig. 1a1 and 1a2. Then the imprinted Al chip was anodized in an acidic solution with desirable direct current (DC) voltage (see the Method section). Notably, solution based Al anodization process typically lead to formation of porous alumina films on Al substrates with local hexagonal pore ordering, due to the fact that the honeycomb structure is the most stable structure in nature<sup>16-18</sup>. However, in this work, squarely ordered nanoimprint was utilized to introduce periodic defects intentionally. As the square order is not naturally stable, voids were formed between unit cells during anodization. These voids were consequently filled up with the un-anodized Al material during the formation of porous alumina, as shown in Fig. 1b1 and 1b2. And Al NSPs were obtained after wet chemical etching away of alumina, as illustrated in Fig. 1c. The formation of NSPs by square pattern nanoimprint assisted anodization can be further evidenced by the bottom view of the anodic alumina shown in Fig. 1d, in which the periodic voids can be conspicuously resolved. In contrast, bottom surface of a hexagonally ordered porous alumina film is shown in supplementary Fig. S1a, and there is no void can be observed, leading to concave structure on the Al substrate without any NSP (Fig. S1b). Figure 1e demonstrates an SEM image of the resulting true three-dimensional Al NSP array with 1.2  $\mu$ m pitch and approximately 1.2  $\mu$ m height.

The existing research has shown that photon management capability of a nanostructure largely depends on its geometric factors, as well as the material intrinsic optical property<sup>13,19-22</sup>. Therefore, the ability to control geometries of nanostructures, i. e. pitch, height, shape, is the prerequisite for seeking the optimal device structure. In this work, the pitch of the 3-D NSPs is determined by the nanoimprint master design together with the DC anodization voltage (Method section). In experiments, pitches of 1 µm, 1.2 µm, 1.5 µm and 2 µm were chosen in order to achieve acceptable film coating uniformity during the solar cell fabrication with plasmaenhanced chemical vapor deposition (PECVD) and sputtering (Method section). Meanwhile, it was found that the height of the NSPs can be readily tuned via controlling anodization time (Fig. S2). However, it was also found that beyond certain time, the height of NSPs does not grow anymore, and the greatest height of NSPs is found to be approximately equal to the corresponding pitch (Fig. S2). Figure 2a shows the schematics of an NSP array before and after a-Si solar cell device fabrication with each layer clearly labeled. Figure 2b1, 2c1 and 2d1 show the 1.2 µm pitch nanostructures formed after anodization time of 30 mins, 3 hrs and 6 hrs, respectively. Interestingly, there can be seen a structural transformation from nanoconcave (NC) to NSP. Apparently NCs were formed with short time anodization. In this case the porous alumina film was too thin to support the growth of tall NSPs. Since their peak to valley height differences are 209 nm (Fig. 2b1), 614 nm (Fig. 2c1), and 1151 nm (Fig. 2d1), respectively, they are named as NC 200, NSP 600 and NSP 1200 correspondingly for the convenience. And the SEM images of NSP 400 and NSP 800 are shown in Fig. S3a and S3b.

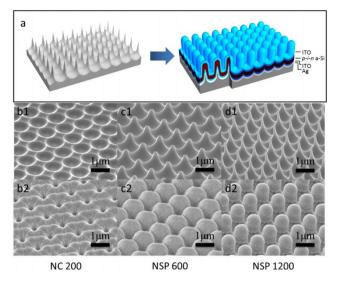
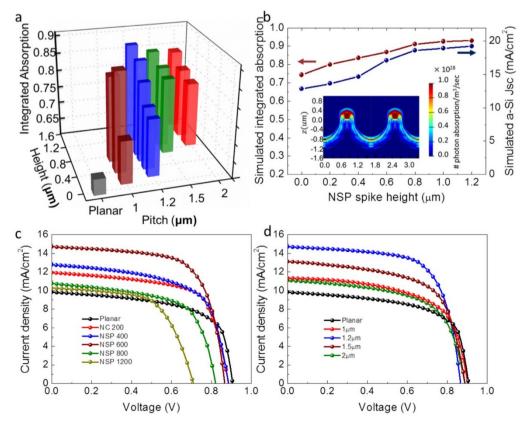


Figure 2 | SEM of Al NC, NSP and thin film a-Si solar cell based on them. (a) Schematic of multiple thin film layers deposited on NC and NSP for solar cell fabrication. SEM of (b1)NC 200, (c1)NSP 600, (d1) NSP 1200 and their corresponding a-Si solar cell at (b2), (c2) and (d2).

Note that all the NSP height mentioned here were obtained using atomic force microscopy (AFM) and the AFM images can be found in Fig. S6. Figure 2b2, S3c, 2c2, S3d and 2d2 show the SEM images of 3-D NSPs after depositing a-Si solar cell layers on NC 200, NSP 400, NSP 600, NSP 800, and NSP 1200, respectively. And the cross-section cut of these devices were obtained by focused ion beam (FIB) shown in Fig. S4a  $\sim$  S4e. Fig. S5a  $\sim$  S5f demonstrate SEM images of the NSP arrays before and after a-Si thin film device fabrication, with

pitches of 1 µm, 1.5 µm and 2 µm. It is clear that 5 different NSP heights can be retained after thin film deposition. It is worth pointing out that Al is known to have higher thermal expansion coefficient than Si, it may cause cracks of a-Si film and failure of device. To address this issue, we have converted 100 nm of the Al surface to Al oxide via low voltage DC anodization (Method Section). This layer of Al oxide can serve as a buffer layer to mitigate the thermal expansion coefficient mismatch. In addition, we have observed that the a-Si devices fabricated on flat and smooth Al substrates are prone to crack and peel off, however, a-Si device fabricated on NSPs are much more robust, as shown in Fig. S7 This observation can be simply explained as following. In a planar device, expansion of the bottom Al substrate leads to stretching of the a-Si PV device atop which can result in film cracking. However, when a-Si thin film PV device is uniformly deposited on the 3-D structure, the strain caused by thermal expansion can be effectively released three-dimensionally.

As mentioned above, optical absorption as well as photo-carrier dynamics are the key issues determining primary electrical performance of a solar cell device, *i. e.* short-circuit current density  $(I_{cc})$ , opencircuit voltage  $(V_{\alpha c})$  and fill factor (FF). These three parameters are in fact tightly coupled in reality. Therefore, coupled optical and electrical property investigation of nanostructured solar cells is of critical importance<sup>3,23</sup>. Herein, systematic optical and electrical characterizations on the fabricated 3-D NSP solar cells have been performed with experiments in conjunction with finite difference time domain (FDTD, Lumerical) optical simulation and semiconductor device simulation (Silvaco Atlas). Figure 3a shows the Air mass 1.5 global (AM 1.5 G) spectrum integrated above-band-gap solar cell device optical absorption acquired after measuring the absorption spectra shown in Fig. S8a and S8b. Obviously, the optical absorptions of all 3-D NSP cells are much higher than that of the planar cell which can only absorb about 64% of the solar spectrum. It can be also



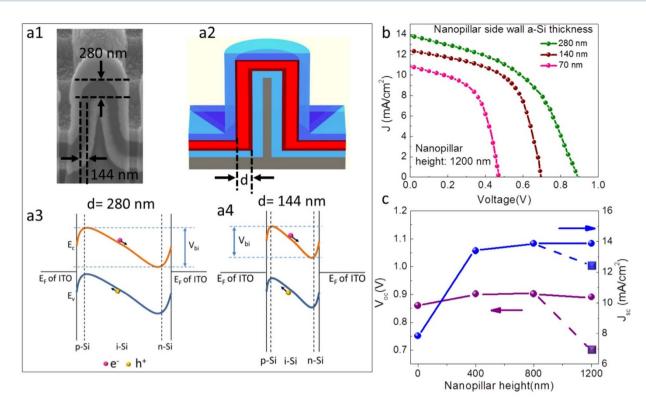
**Figure 3** | (a) AM 1.5 G spectrum integrated optical absorption of solar cell with different NSP heights and pitches. (b) Simulated AM 1.5 G spectrum integrated optical absorption and simulated  $J_{sc}$  in a-Si layer and inset shows the photon absorption profile in the 1.2 µm height device. *J*-*V* characteristics of best efficiency solar cells on (c) different NSP heights of 1200 nm pitch and on (d) optimal height for different pitches.

conspicuously seen that device optical absorption monotonically increases with the height of NSPs for pitches of 1.2 µm, 1.5 µm and 2  $\mu$ m, with the optimal absorption of 88.8% for 1.2  $\mu$ m pitch NSP device with 1.2 µm NSP height. This can be simply interpreted as the increased light trapping effect for higher aspect ratio structures. These results are further evidenced by FDTD optical simulation shown in Fig. 3b in which the simulated integrated absorption in the entire device and in a-Si layer only, represented as  $J_{sc}$ , increase monotonically with NSP height. Note that the inset of Fig. 3b shows the absorption profile in the 1.2 µm height device (other height device results are shown in Fig. S9), indicating that light absorption primarily occurs in the active a-Si laver, however, the absorption in the front and back indium tin oxide (ITO) is not negligible. Meanwhile, the fact that increasing pitch size for the same NSP height results in reduction of light absorption can be attributed to the reduced light scattering with large NSP to NSP distance at large pitch. However, device optical absorption for 1 µm pitch NSPs shows a maximal at 438 nm height. This is due to the excessively high material filling ratio for high aspect ratio NSP with 1 µm pitch, leading to high optical reflectance on the top surface of the structure, as shown in Fig. S5d.

The analysis on device optical absorption indicates that in general high aspect ratio structures with proper gap in between favor light trapping. However, this guideline may not be in harmony with the requirements for optimal device electrical performance. Figure 3c plots the current density - voltage (J-V) characteristics of the best efficiency solar cells under AM 1.5 G condition of different NSP heights in pitch of 1.2 µm, with Table 1a showing their detailed  $V_{oc}$  J<sub>sc</sub>, FF and efficiencies. And the efficiency statistical data is shown in Fig. S10a. In addition, external quantum efficiencies (EQE) of these devices were measured and shown in Fig. S11a. It can be seen that with the increase of the height of structures from NC 200 to NSP 600, the efficiencies of cells rise from 6.93% and reach the peak of 8.40% for NSP 600, which is 43% higher than that of the planar control device fabricated together. The same trend can be observed when comparing  $J_{sc}$ , which rises from 9.9 mAcm<sup>-2</sup> for the planar device to 14.72 mAcm<sup>-2</sup> for NSP 600 device. However, further increasing height of NSPs to NSP 800 and NSP 1200 leads to reduction of  $J_{sc}$  and  $V_{oc}$ , resulting in even lower efficiency than the planar control device. The initial rise of  $J_{sc}$  with height of NSP can be explained as the improved light trapping effect for 3-D structures. Nevertheless, loss on  $J_{sc}$  and  $V_{oc}$  for structures with higher aspect ratio indicates that optical absorption cannot solely determine the performance of the devices. And this intriguing effect will be further examined with simulations later. Meanwhile, the J-V characteristics of solar cells with best efficiencies among different NSP heights in other pitches are plotted in Fig. 3d, their detailed performance parameters, statistical data of efficiency and EQE are shown in Table 1b, Fig. S10b and Fig. S11b, respectively. It can be seen that the best performance for all four pitches can beat that of the planar control device, with the 1.2 µm pitch NSP solar cell demonstrating the greatest advantage mainly due to the enhancement on  $J_{sc}$ . And interestingly, it has been discovered that the best performance can be obtained when NSP height is  $\sim$ 50% of the pitch for pitch of 1.2 µm, 1.5 µm and 2.0 µm. However, the best performance for 1.0 µm pitch is from the device fabricated on 156 nm NSP height.

Overall, the electrical measurements have shown that the NSP devices with intermediate height have the optimal performance, and further increase the aspect ratio deteriorates device performance. In the past, it has been reported that excessive surface area for nanostructures may lead to performance degradation, especially for materials such as crystalline Si, GaAs, etc, which have rather low recombination rate in bulk but high recombination rate at surface<sup>24,25</sup>. However, since a-Si is defective in nature with high recombination rate in bulk, the surface recombination may not have dominant effect on device performance. In order to uncover this intriguing phenomenon, we have carefully examined the structures of NSP device with different NSP height. As shown in the device cross-sections in Fig. S4, it was discovered that for high aspect ratio structure, especially NSP 1200 device, a-Si film thickness on NSPs is rather un-uniform. Further observation from Fig. 4a1 shows that a-Si at the top of the NSP tip and at the bottom in between the NSPs is around 280 nm, which is close to that of the other low aspect ratio structures. However, the a-Si film on the side wall of the NSPs is only 144 nm, which is  $\sim$ 50% of the expected deposition thickness. This observation can be attributed to the directionality of PECVD deposition leading to un-uniform coverage on high aspect ratio nanostructures. In fact, similar effect has been observed previously, and it was found to be detrimental to photovoltaic performance<sup>5,26,27</sup>. However, there has no clear understanding on the mechanism yet. Therefore, device physics was analyzed and modeled to facilitate understanding here. In experiments, ITO has been used as the transparent conductive contact to a-Si solar cell device. However, as it has non-ideal work function matching with *p* and *n* type a-Si, Schottky contact can be formed at the front and back side of *p-i-n* a-Si layers<sup>28</sup>. Figure 4a3 depicted a schematic of the band alignment of the device based on ITO work function of 5.0 eV<sup>29</sup>. Due to the existence of the Schottky contact, p and n a-Si are partially depleted leading to a compromised building potential  $(V_{bi})$  as compared to an ideal contact situation. In this scenario, reduction of p and n a-Si thickness may lead to more severe depletion in them and significantly compromise V<sub>bi</sub> and eventually V<sub>oc</sub> and J<sub>sc</sub>. In addition, a-Si film thickness reduction on NSP side wall can also lead to loss of optical absorption which further hurts  $J_{sc}$ . Note that it has been reported previously on planar a-Si thin film solar cells that the thinner a-Si, especially p and n layers, can lead to drop of  $V_{oc}$  based on the similar rationale<sup>15,30</sup>. To confirm this effect on the NSP solar cells, device simulation with Silvaco Atlas was performed with the details described in Method section. Supplementary Fig. S12 demonstrates the modeled energy band bending across the side wall of 280 nm, 140 nm and 70 nm a-Si thickness, respectively. Note that in these cases the nanopillar structure shown in Fig. 4a2 was utilized for device modeling for simplicity, and the *p-i-n* thickness scaled down proportionally, with the top and bottom a-Si thickness remained unchanged at 280 nm. Furthermore, device J-V characteristics with 5.0 eV workfunction of ITO contact have been modeled and are shown in Fig. 4b. It can be clearly seen that with the reduction of a-Si thickness, both  $V_{oc}$  and  $J_{sc}$  decrease significantly, which is consistent with the above discussion. Beside, device performance with 4.8 eV and 5.2 eV work function of ITO contact were also modeled for comparison and the J-V characteristics (Fig. S13) showed the consistent trend. Figure 4c shows the device simulation results for the nanopillars with different height, and with 280 nm side wall a-Si film thickness (spherical symbols) and 140 nm side wall a-Si film thickness (square symbols). Note that the un-uniformity was only applied to nanopillar device with 1200 nm height. It can be found  $J_{sc}$ monotonically increases with the height due to the improved light trapping in the device when the a-Si film thickness is entirely uniform. However, when the side wall a-Si was decreased to 50% thickness (140 nm) for the 1200 nm height device, J<sub>sc</sub> drops from 13.9 mA/cm<sup>2</sup> to 12.4 mA/cm<sup>2</sup> accompanied with a more significant  $V_{oc}$  reduction from 0.89 V to 0.69 V, leading to a peak performance for 800 nm high nanopillar. This overall trend is consistent with the experimental results shown in Table 1.

The above results have demonstrated guidelines to design NSP solar cells with the optimal performance. The methodology can be also extended to rational design of other types of nanostructure photovoltaic devices, including nanopillar solar cells, nanocone solar cells, etc., which are being extensively explored<sup>4,5,31</sup>. Meanwhile, scalable fabrication for any type of nanostructure is of paramount importance for future cost-effective photovoltaic applications in large scale. As mentioned above, regular structures are preferred to



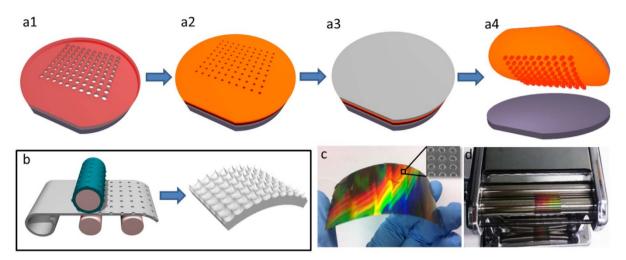
**Figure 4** | (a1) Cross-sectional SEM image of an NSP 1200 device showing thinner side wall a-Si thickness than the top a-Si thickness. (a2) Schematic of nanopillar a-Si solar cell for the simplified device simulation. (a3) Schematic band bending for 280 nm thick a-Si device. (a4) Schematic band bending for 140 nm thick a-Si device showing lowered building potential. (b) modeled *J*-*V* curves of the nanopillar a-Si solar cells with different side wall thickness. (c) Modeled  $V_{oc}$  and  $J_{sc}$  of the nanopillar solar cell versus different height. The spherical symbol data are from devices with 280 nm sidewall a-Si thickness, and the square symbol data are for the device with 140 nm sidewall a-Si thickness.

obtain uniform coating of photovoltaic materials on the structures. Up-until-now, the most commonly used fabrication approach involves batch lithography and RIE which poses a challenge for low cost fabrication in large scale<sup>5,7,10</sup>. In this work, a roll-to-roll compatible approach have been developed to fabricate the regular NSP arrays in large scale. Figure 5 demonstrates the schematic of the fabrication process. Specifically, roll-to-roll nanoimprint is implemented by imprinting aluminum foil with a thin metal (Ni/Cu) foil nanoimprint master mounted on a roller. The metal foil nanoimprint master was fabricated with photolithography in conjunction with electrodeposition, as schematically shown in Fig. 5a1  $\sim$  5a4. The detailed process can be found in the method section. Briefly, a squarely ordered nanohole array was defined on photoresist layers on a Si wafer by photolithography (Fig. 5a1). Then bilayer TiW/Cu

thin film was sputtered on the wafer (Fig. 5a2) followed by electrodeposition of 20  $\mu$ m Cu and 30  $\mu$ m Ni (Fig. 5a3). Finally, flexible nanoimprint master foil was released, as shown in Fig. 5a4. And Fig. 5b show a photo of the as-made flexible metal nanoimprint master. Such a flexible master was then mounted on a custom-made roller system primarily composed of two parallel cylinder rollers, as shown in Fig. 5c. Then an Al foil was fed in the rollers for imprint as schematically shown in Fig. 5d. This nanoimprint process is apparently roll-to-roll compatible with much higher scalability as compared with the stamp imprint process shown in Fig. 1. Meanwhile, it is worth pointing out that the solution based anodization and etching process have been demonstrated as roll-to-roll compatible as well<sup>32</sup>. Therefore low-cost fabrication of Al substrates with highly regular NSP arrays is feasible. To examine the effectiveness of this unique

Morphology	V <sub>oc</sub> (V)	J <sub>sc</sub> (mAcm <sup>-2</sup> )	Fill Factor (%)	Efficiency (%)
Planar	0.907	9.90	65.37	5.87
NC 200	0.886	11.93	65.55	6.93
NSP 400	0.885	12.78	64.43	7.29
NSP 600	0.866	14.72	65.88	8.40
NSP 800	0.820	10.76	62.70	5.53
NSP 1200	0.710	10.27	61.12	4.46
Pitch (µm)	V <sub>oc</sub> (V)	J <sub>sc</sub> (mAcm <sup>-2</sup> )	Fill Factor (%)	Efficiency (%)
Planar	0.907	9.90	65.37	5.87
1.0 μm (156 nm)	0.894	11.35	65.48	6.64
1.2 μm (NSP 600)	0.866	14.72	65.88	8.40
1.5 µm (766 nm)	0.889	13.13	62.80	7.33
2.0 µm (905 nm)	0.888	11.08	61.25	6.03

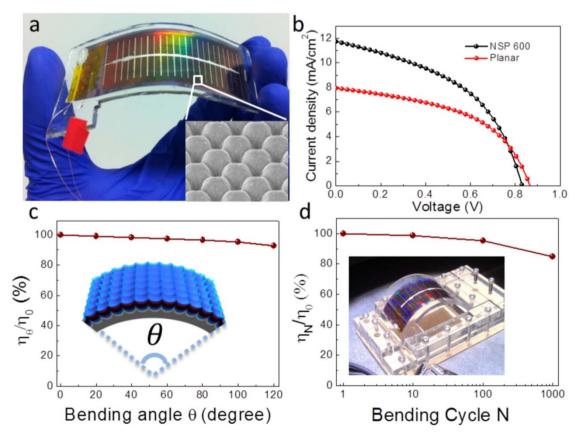
Table 1 | Electrical performance parameters of best efficiency solar cells on (a) different NSP heights of 1200 nm pitch and (b) devices with optimal height within different pitches



**Figure 5** | **Roll-to-roll fabrication of large scale NSP substrate.** (a1) Silicon wafer patterned with double layers photoresist hole array. (a2) Sputtered Ti/ W/Cu on photoresist for seed layer of the subsequent metal electrodeposition. (a3) Thick copper and nickel electrodeposited on the seed layer. (a4) Flexible nanoimprint master foil released in acetone. (b) Schematic of Roll-to-roll nanoimprint to fabricate large scale NSP on flexible Al foil. (c) Thin metal foil of nanoimprint master and inset shows SEM micrograph of its surface. (b) Roll-to-roll nanoimprint set-up with nanoimprint foil master mounted on.

fabrication process, *p-i-n* junction a-Si thin film solar cell devices were fabricated on top of the NSP arrays with 1.2  $\mu$ m pitch and ~600 nm NSP height, followed by encapsulation of the entire device into Polydimethylsiloxane (PDMS) for protection. Due to utilization of thin Al foil (0.2 mm) and flexible packaging material, the device showed appreciable flexibility. Figure 6a demonstrates a flexible

device with size of 2 cm by 7 cm. This device can be used to power up a toy wind turbine under the illumination of a table lamp (intensity: 25 mW/cm<sup>2</sup>), as shown in the supplementary video. Note that Al substrate has a number of advantages over plastic substrates for flexible photovoltaic application. Al substrate allows PECVD deposition temperature up to 600°C, which is significantly higher as



**Figure 6** | **Characterization of large scale NSP solar cell fabricated by roll-to-roll method.** (a) Large scale a-Si solar cell fabricated by roll-to-roll method and the inset shows the SEM micrograph of the surface. (b) *J-V* characteristic of large scale NSP and planar device. (c) Relative efficiency variation at different bending angle and the inset shows the schematic of defining bending angle. (d) Relative efficiency variation after bending cycle N to the initial efficiency and inset shows the measurement setup with bending.

compared to other plastic substrate. Such temperature allows deposition of not only a-Si film, but also other types of films such as Copper-Indium-Gallium-Selenide (CIGS), CdTe, etc. In the case of a-Si, low temperature (~100°C) PECVD a-Si deposition needs to be performed on plastic substrates due to their low glass transition temperature, which leads to poor a-Si material quality and inferior performance<sup>33</sup>. By using flexible Al substrates, the optimal a-Si deposition temperature on the rigid glass substrate ( $200 \sim 300^{\circ}$ C) can be applied, leading to better device performance. The electrical performance of the large flexible solar cell here was characterized under AM 1.5 condition and compared with a planar control device with the same size. Figure 6b plots the J-V characteristics of the two types of devices, showing 5.1% power conversion efficiency for the NSP solar cell and 3.7% efficiency for the planar device. This nearly 38% efficiency boost clearly demonstrates the improvement of performance with 3-D NSP structures at large scale. In order to evaluate the device performance variation during flexible operation, photovoltaic measurements were performed while bending the device with different angles using the set up shown in the inset of Fig. 6d. The curve in Fig. 6c shows the efficiencies of the NSP device normalized with projection area of simulated light source with respect to bending angles up to 120°. There can be seen a marginal efficiency drop upon bending with the maximal change up to 7.4% for 120°. Besides, the reliability of the nanospike cells with bending cycles of 10, 100 and 1000 have been investigated and the results are shown in Fig. 6d revealing that the efficiency can remain over 85% of the initial's value after 1000 bending cycles. These results have demonstrated that the 3-D NSP solar cells have excellent flexibility and mechanical robustness which is crucial for future practical applications.

In summary, we have demonstrated a roll-to-roll compatible approach to fabricate regular arrays of 3-D NSP arrays in large scale with the capability to precisely control the geometry of the nanostructures, including periodicity, height and aspect ratio. This type of nanostructured substrate is an appealing platform for development of a new type of thin film photovoltaic technology. In this work, a-Si was used as the model material to demonstrate the effectiveness of the 3-D NSP arrays for thin film photovoltaics. Systematic experiments and modeling have shown that in general the NSP solar cells can beat their planar counterparts. However, proper structural design is crucial in order to balance photon capturing capability and carrier collection associated with the nature of contact and film thickness uniformity. In the optimal case, a 3-D NSP solar cells can outperform a planar device by 43%, shown in this work. Meanwhile, large size flexible solar cell devices have also been fabricated and their respectable electrical performance has been systematically characterized with various bending conditions. Meanwhile, there is still room to further improve the performance of the devices, by optimizing a-Si deposition conditions, and quality of electrical contacts. It is worth pointing out that the technology developed here can be extended to other thin film photovoltaic material systems, including CdTe and Cu(In,Ga)Se, etc., to enable high performance flexible thin film photovoltaics.

#### Methods

Fabrication of three-dimensional nanospike (NSP) array substrate. Aluminum (Al) foil was cut into 1.7 cm by 3.5 cm pieces and cleaned in acetone and isopropyl alcohol. The foils were then electrochemically polished in a 1:3 (v:v) mixture of perchloric acid and ethanol for 2 min at 12 V and 10°C. The polished Al foils were then imprinted by 7 mm by 7 mm home-made silicon master (Squarely ordered pillar array with height of 200 nm and pitches of 1 µm, 1.2 µm, 1.5 µm and 2 µm) with a pressure of  $\sim 2 \times 10^4$  N cm<sup>-2</sup> to initiate the perfectly ordered AAO growth. After that Al foils were anodized with a home-built anodization setup with voltage equal to pitch (nm)/2.5. The detail anodization conditions are listed in supplementary table S1. The anodized AAO film was then etched in a mixture of chromic acid (1.5 wt%) and phosphoric acid (6 wt%) solutions at 100°C for 15 mins to expose the NSP. After etching, the 3-D Al NSP array chips were cleaned with DI-water and blown dry with compressed air.

**FDTD and Silvaco simulations.** Finite-Difference Time-Domain (FDTD) method was conducted to study the absorption properties of different structures. Simulation structures were constructed based on the AFM data obtained from experimental measurements. Plane wave light source with wavelength from 300 nm to 800 nm was illuminated normally down to the simulated structures. Periodic boundary condition was imposed at vertical boundaries and only one unit cell was simulated to reduce the computational demand<sup>19</sup>. The optical constants for a-Si and ITO were taken from online database<sup>34</sup>. The optical constants for Ag were taken from Lorentz-Drude fit to values contained in the Lumerical FDTD simulation package. We calculated the

generation rate profile,  $G_{opt}(\vec{r}, \lambda)$  using  $G_{opt}(\vec{r}, \lambda) = \frac{\epsilon'' |E(\vec{r}, \lambda)|^2}{2\hbar}$  where  $\epsilon''$  is the imaginary part of the permittivity and  $E(\vec{r}, \lambda)$  is the (optical) electric field<sup>3,23</sup>. We also calculated absorption in different materials by inserting material refractive index filters and then integrated the absorption spectrum with AM1.5 G solar spectrum to obtain the integrated broadband absorption and ideal  $J_{sc}$  in a-Si with 100% carrier collection efficiency<sup>6,35</sup>.

The device structure simulated was built by Silvaco Devedit(V.2.8.7.R) and run on Silvaco Atlas(V.5.18.3.R). The density of states of amorphous Silicon is considered as a combination of two exponentially decaying band tail states and two Gaussian distributions of mid-gap state<sup>36,37</sup>. To further accurately model the device performance, light induced defects model was also utilized here. The TCO contact of device used in simulation was ITO with workfunction of 4.8 eV, 5 eV and 5.2 eV<sup>19</sup>. Both thermionic emission and tunneling were considered for the transport of carriers through the schottky diode. The detailed parameters can be found in Supplementary Table S2.

Fabrication of a-Si solar cell on NSP array substrate. 100 nm on the Al NSP surface was converted to Al<sub>2</sub>O<sub>3</sub> by low voltage anodization (20 V, in 1.7 wt% H<sub>2</sub>SO<sub>4</sub>) which serves buffer layer to mitigate the thermal expansion coefficient mismatch between Al substrate and the thin film device. After that, 200 nm silver was deposited on Al NSP for passivation to avoid aluminum contamination. Afterward, multiple layers of ITO and a-Si were deposited in the order of ITO-n-i-p-ITO with thickness of 100-20-240-20-200 (in nanometers). ITO was deposited with ULVAC sputtering system will DC 300W at gases flow of Ar: 20 sccm and Oxygen: 0.6 sccm. a-Si were deposited with Sopower dual chamber PECVD system using SiH<sub>4</sub> with H<sub>2</sub> dilution and B<sub>2</sub>H<sub>6</sub> and PH<sub>3</sub> as P-type and N-type dopant.

**Roll-to-roll fabrication of flexible NSP array.** Fabrication process of thin metal nanoimprint master is described as following and illustrate in Fig. 5a. A silicon wafer was spin-coated at 4000 rpm with double layer photoresist with the lower releasing layer of 100 nm PMMA and upper layer of 200 nm AZ7908 photoresist diluted with AZ® EL Thinner in 1: 1 ratio. The upper layer of photoresist is then patterned with hole array with pitch equal to the nanoimprint master. The patterned wafer was then sputtered with 50 nm/200 nm of TiW/Cu as a seed layer for the subsequent electroplating. After sputtering, 20  $\mu$ m of copper was electroplated in electrolyte consist of 225 g/L CuSO<sub>4</sub>, 50 g/L H<sub>2</sub>SO<sub>4</sub> and 50 ppm HCl at 0.2 amperes per square decimeter (ASD). After that, 30  $\mu$ m nickel was electroplated in electrolyte of 1:4 nickel sulfate at 0.5 ASD and resulted in total 50  $\mu$ m thick foil deposited. Finally, flexible nanoimprint master foil was released by soaking and dissolving the PMMA layer in acetone for 1 hour.

Roll-to-roll nanoimprint was achieved by home-made manual roll-to-roll nanoimprint machine consist of two rollers with one of them was mounted with nanoimprint master metal foil which are illustrated in supplementary Fig. 5d. The imprinted aluminum foil was undergone anodization and etching processes with conditions described in the previous section to fabricate large scale flexible NSP substrate.

Morphology characterization, optical reflectance and device performance characterization of solar cell. Morphologies of the NSP and thin film were examined by SEM using a JEOL6700F at an accelerating voltage of 5 kV and Digital Instruments Dimension 3000 Atomic Force Microscope. The *I*-V characteristic of all the solar cell are characterized by Oriel solar simulator, 450 W Xe lamp, AM 1.5 global illumination with output calibrated to 1 sun (100 mW cm<sup>-2</sup>) with mono-crystalline reference cell (Newport corporation, 91150V) and Keithley 2400 source meter. EQE measurement was carried out by Oriel QE-PV-SI, Newport Corporation. Diffused reflectance spectra were carried out on the solar cell surface using a Perkin-Elmer UV/ vis spectrophotometer (model Lambda 20).

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S.-F.L., K.-H.T., J.-M.S., C.-H.S., D. Li and Z.F. designed the experiments. S.-F.L., K.-H.T., T.-H.H., C.-H.H., L.L., D.L., Q.L. and Z.F. carried out experiments. L.G. and Q.Z. carried out the simulations. S.-F.L., L.G., Q.Z., K.-H.T., J.-M.S., C.-H.S., T.-H.H., C.-H.H., L.L., D. Li, Q.L. and Z.F. contributed to the data analysis. S.-F. Leung and Z.F. wrote the paper and all the authors provided feedback.

#### Additional information

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