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Artificial semiconductor/insulator superlattice channel structure for high-performance oxide thin-film transistors

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High-performance thin-film transistors (TFTs) are the fundamental building blocks in realizing the potential applications of the next-generation displays. Atomically controlled superlattice structures are expected to induce advanced electric and optical performance due to two-dimensional electron gas system, resulting in high-electron mobility transistors. Here, we have utilized a semiconductor/insulator superlattice channel structure comprising of ZnO/Al_2O_3 layers to realize high-performance TFTs. The TFT with ZnO (5 nm)/Al_2O_3 (3.6 nm) superlattice channel structure exhibited high field effect mobility of 27.8 cm^2/Vs, and threshold voltage shift of only < 0.5 V under positive/negative gate bias stress test during 2 hours. These properties showed extremely improved TFT performance, compared to ZnO TFTs. The enhanced field effect mobility and stability obtained for the superlattice TFT devices were explained on the basis of layer-by-layer growth mode, improved crystalline nature of the channel layers, and passivation effect of Al_2O_3 layers.

Transparent electronics has gained special attention in recent years due to their wide range of device applications for information display and information storage[1]. Especially, high-mobility thin-film transistors (TFTs) have been receiving strong attention, because of their importance as a backplane for next-generation displays, such as large-size, high-resolution, transparent, and three-dimensional displays. Unfortunately, the commercially used amorphous Si (a-Si) TFTs have reached technical limits as backplane devices, because of insufficient mobility and long-term instability of the channel layers under electrical bias stress[2,3]. In addition, because of their narrow band-gap, Si-based TFTs cannot be applied to new-industry markets, such as smart windows and transparent displays.

In order to achieve transparent TFTs with high mobility and high stability, oxide-based semiconductors are the most feasible material as a channel layer. In particular, high-performance TFTs have been fabricated at low process temperatures compared with those necessary for *a*-Si TFTs, using polycrystalline binary zinc oxide (*poly*-Zn-O)[4,5], amorphous ternary indium-zinc-oxide (*a*-In-Zn-O)[6] or zinc-tin-oxide (*a*-Zn-Sn-O)[7], and amorphous quaternary indium-gallium-zinc-oxide (*a*-In-Ga-Zn-O)[3,8,9]. Many prototype displays, such as active-matrix liquid crystal displays (AM-LCDs), active-matrix organic-emitting-diode displays (AM-OLEDs), and e-paper, have been demonstrated with oxide-based TFT arrays[9]. However, the long-term instability of oxide-based TFTs, regarding the bias[10,11], temperature[12] and illumination stress[13,14], is currently one of the most critical issues that must be solved. Many studies have reported the deterioration of device performance due to instability problems of the oxide TFTs with high mobility. It was suggested that the origins of the instability inducing V_{th} shift in oxide TFTs are attributed to i) the charge injection/trapping in the gate-interface (between the dielectric and the channel) or within the bulk of the channel[10–12], ii) photo-generated carriers[13–18], and iii) the back channel effect by molecular adsorption or desorption[16,18,19]. Highly stable oxide TFTs were obtained by passivation layers[19], and the addition of stabilizer elements such as Ga, Hf, and Ti in the oxide channels[8,20,21]. Unfortunately, the TFTs with stabilizer exhibited reduced field effect mobility. In order to obtain highly stable oxide TFTs with high mobility, several groups have attempted to develop robust channels using a bi-layers[22,23].

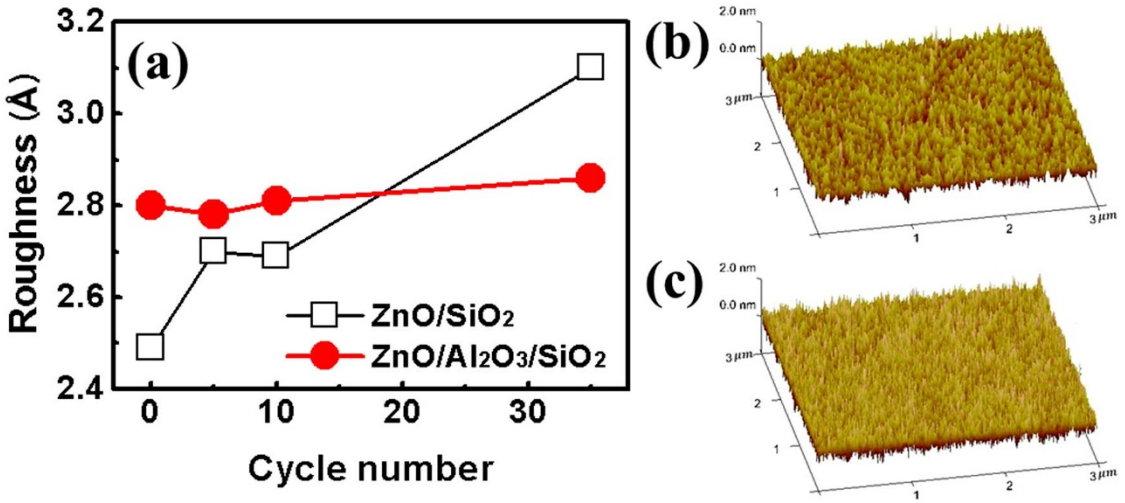


Figure 1 | AFM results for ZnO layers deposited on the SiO_2/Si and the Al_2O_3/SiO_2/Si. (a) RMS variation as a function of ALD cycles for Zn-O. Surface images of the ZnO layers deposited on (b) the SiO_2/Si and (c) the Al_2O_3/SiO_2/Si with 36 ALD cycles.

The fabrication of atomically controlled heterostructures such as multilayers and superlattice structure has shown new possibilities to generate novel electronic properties in the oxide materials. Recently, the formation of two-dimensional electron gas (2DEG) in the superlattice structure with periodic arrangement has been suggested, as well as oxide interfaces of epitaxial-grown heterostructures including $LaTiO_3/SrTiO_3$[24], $LaAlO_3/SrTiO_3$[25], and ZnO/MgZnO[26]. Also, Y. Chen *et al.*[27] reported that the 2DEG can occur even in amorphous $SrTiO_3$-based oxide heterostructures, which resulted from the formation of oxygen vacancies near the interface. Although the origin of 2DEG is still controversial, the researches on their exciting properties are expected to provide more advanced devices. For example, field-effect transistors and high-electron-mobility transistor consisting of ZnO/MgZnO[26], GaAs/AlGaAs[28] or AlGaN/GaN[29] heterostructures have shown extremely high electron mobility due to field-effect-modulated 2DEG at the interface of a heterojunction, while the charge scattering at the hetero-interface is not serious, due to the quantum 2D nature of the channel. Due to the large band discontinuities, it is expected that the electron concentration bound by 2DEG is quite high, and electronic devices show high mobility. Thus, the use of an oxide superlattice with band discontinuities is one method to increase the field effect mobility of TFT devices by the formation of 2DEG in the channels.

The ZnO TFTs with appropriate channel definition generally exhibited the mobility of 0.3 ~ 13 cm^2/Vs[5,30–33], but showed high instability, compared to the InGaZnO TFTs. It is well known that Al_2O_3 is often used as a dielectric layer in the TFT devices to achieve high mobility devices at low voltages due to its high dielectric constant (~9) and low leakage current with a wide band gap (~9 eV). The electrical parameters of TFT devices such as field effect mobility (μ_{FE}), threshold voltage (V_{th}), and subthreshold swing (*SS*) strongly depend on the device structure and fabrication process of TFT components. Atomic layer deposition (ALD) process has shown many unique advantages for the deposition of various oxides, nitrides, and sulfides with highly precise thickness/composition control, large area capability/uniformity, and high conformity at relatively low processing temperature. It was suggested that the oxide TFTs using AlO_x (fabricated by ALD) exhibit remarkably stable performance against gate stress-bias[5,32,33]. Until now, the field effect mobility of binary ZnO TFTs fabricated at low-process temperatures was not enough for the operation of large-size/high-resolution displays, where higher mobility is needed to improve switching speeds and obtain high current. In order to improve the field effect mobility and the stability of TFT devices, the crystallinity of channel layers and the interface state between channel/dielectric layers should be optimized for the reduction of the trap density. Based on the previously reported works of ZnO layer deposition by ALD process[5,32,33], the ZnO channel layers with reduced defects and atomically flat surface can be obtained under the optimum condition of the ALD process.

In the present work, we have proposed a novel channel structure for obtaining high mobility TFTs with high electrical stability fabricated by atomic layer deposition (ALD). The novel channel consists of the three-period ZnO and Al_2O_3 superlattice structure and it is expected that this structure provide high field effect mobility, because the ZnO/Al_2O_3 superlattice allows the formation of 2DEG and the electrons confined in conducting well layer effectively flow with quasi-two-dimensional nature. The suggested channels are superlattice structure with the periodic arrangement of ZnO and Al_2O_3 layer, and deposited by ALD on SiO_2/p^{++}-Si substrates at 200°C. The field effect mobility and device stability of superlattice channel TFTs were investigated and compared with single ZnO TFTs.

Results

Figure 1 shows the results of AFM analysis for ZnO layers deposited by ALD at 200°C on SiO_2/Si and ALD-grown Al_2O_3/SiO_2/Si substrates. As shown in Figure 1(a), with increasing frequency of ALD cycles (up to 36 cycles), the roughness of ZnO layers deposited on the SiO_2 surface was increased from 2.5 to 3.1 Å. The morphologies of ZnO layers on the SiO_2 surface did not show layer-by-layer growth behavior, even with 36 cycles [Figure 1(b)]. Alternatively, the ZnO layers deposited on the SiO_2 with an Al_2O_3 buffer layer (36 cycles) showed almost constant surface roughness (2.8 ~ 2.9 Å), as shown in Figures 1(a) and (c), despite the ZnO thickness. This means that the introduction of the ALD-grown Al_2O_3 buffer layer induces complete two-dimensional growth behavior, even in the initial growth stage.

In order to characterize the crystalline structure of ZnO thin films deposited by ALD and to investigate the effect of the introduction of the Al_2O_3 buffer, the microstructural properties were measured by X-ray diffraction (XRD) and transmission electron microscopy (TEM). Figures 2(a) and (b) show the θ-2θ XRD patterns of the ZnO thin films (~100 nm) grown with and without a 3.6-nm-thick Al_2O_3 buffer layer. The ZnO thin film directly deposited on the SiO_2 showed randomly rotated crystalline phases with diffraction peaks of hexagonal wurtzite structure at 31.7, 34.4, and 36.2° corresponding to the (100), (002), and (101) planes, respectively. However, the ZnO films grown on the Al_2O_3 buffer layer showed a slight c-axis preferred orientation with increased crystallinity, and a relatively intense (0002) diffraction was observed. Figures 2(c–e) show

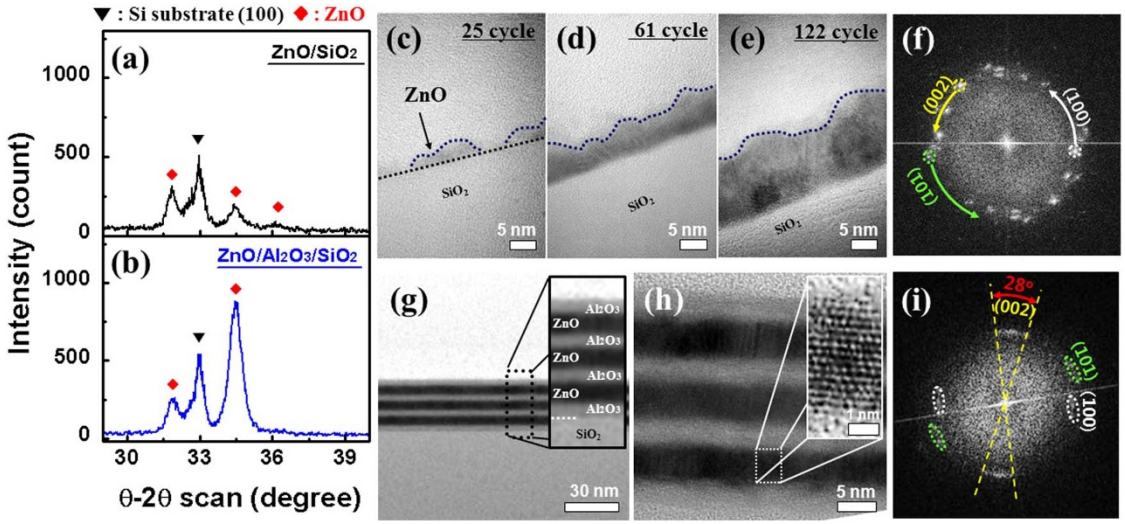
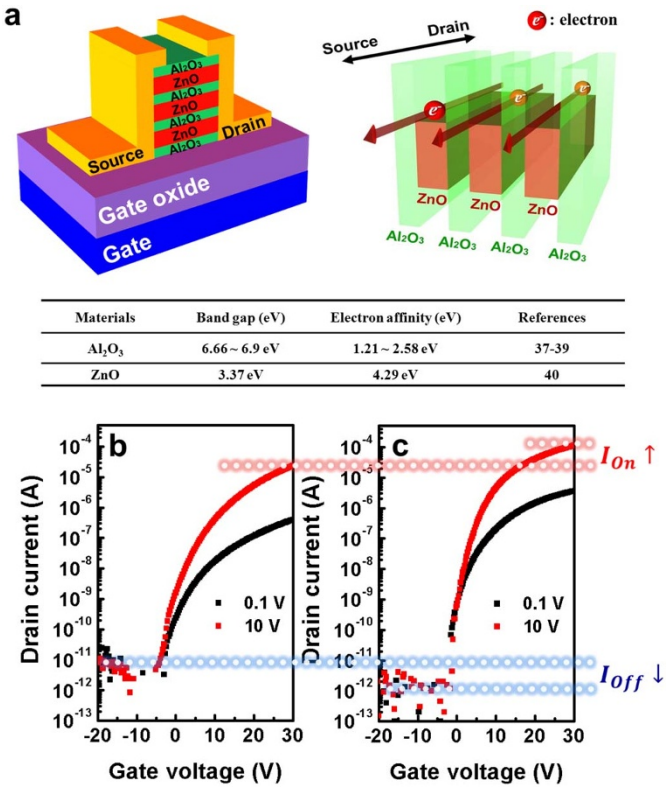


Figure 2 | θ-2θ XRD scans for ZnO films with 100 nm thickness deposited on different surface: (a) SiO_2 and (b) Al_2O_3 surfaces. HRTEM images for ZnO layers deposited on SiO_2 with (c) 10, (d) 61, and (e) 122 ALD cycles. (f) Selected area diffraction pattern for figure (e). (g) Bright-field TEM and (f) HRTEM images for ZnO/Al_2O_3 superlattice films. (i) Selected area diffraction pattern for figure (h).

high-resolution transmission electron microscopy (HRTEM) images of the ZnO layers deposited at 200°C as a function of ALD cycles. In the initial stages of the ZnO films, the ZnO layers have distinct island-like morphologies on the SiO_2. Further increases in the number of process cycles result in continuous films, which have randomly oriented polycrystallinity, as shown in the selected area diffraction pattern (SADP) of Figure 2(f). The increased surface roughness obtained with high ALD cycles can be understood by the coalescence of the ZnO islands with crystalline phase. In contrast, the ZnO/Al_2O_3 superlattice structure deposited by ALD shows very sharp interfaces between ZnO and Al_2O_3, which indicates the behavior of the layer-by-layer growth by the introduction of the Al_2O_3 layer. As shown in Figures 2(g) and (h), the ZnO layers have ~5-nm thickness and well-distinguished crystallinity with atomic arrangement, while the Al_2O_3 layers have 3.6-nm thickness and amorphous phase. Although the ALD process was expected to show a layer-by-layer growth mode by the self-limited reaction process of precursors, the growth of the oxide films was dependent on the surface status of substrates. In the initial states of the ALD process, layer-by-layer growth cannot be accomplished if the surface bonding obstructs the complete reaction, or has ligands of a chemisorbed precursor molecule. So, this may be related to the lack of chemical bonding sites such as O-H groups on the surface of SiO_2[34]. In previous study[35,36], it is reported that more ALD cycles are required for full coverage of the ZnO layer on SiO_2 surface, due to deficient O-H groups on the surface of the SiO_2. In general, it is well known that the surface of untreated Al_2O_3 is hydrophilic due to an abundance of hydroxyl (OH^-) groups. Thus, the ALD-grown ZnO layers are considered to show layer-by-layer growth on the Al_2O_3 surface, because the Al_2O_3 surface induces the formation of fully covered ZnO layer at even low ALD cycles. In addition, the ZnO layers in superlattice films are relatively well-arranged along the c-axis direction, as shown in Figures 2(h) and (i). As a result, the ZnO layers in the ZnO/Al_2O_3 superlattice show significantly improved crystallinity with the c-axis preferred orientation by the insertion of thin Al_2O_3 layers.

The ZnO/Al_2O_3 superlattice thin films are introduced as a channel layer in the oxide TFTs. Figure 3(a) shows a schematic of the oxide TFTs with single ZnO and ZnO/Al_2O_3 superlattice channel layers, which consist of an Al_2O_3/ZnO/Al_2O_3/ZnO/Al_2O_3/ZnO/Al_2O_3 superlattice. It is well known that the Al_2O_3 is an excellent dielectric material due to its high dielectric constant (~9), low leakage current, and wide band-gap (9 eV). Thus, it is often used as a dielectric layer in the TFT devices to achieve high-mobility devices at low gate voltages. Although the Al_2O_3 thin films theoretically have large band gap, it is reported that the Al_2O_3 dielectric films deposited by ALD showed the band gap of 6.66 ~ 6.9 eV[37–39]. The band gap and electron affinity of Al_2O_3[37–39] and ZnO[40] based on previous reports were given in Fig. 3(a). Assuming continuity of the vacuum level and neglecting the effects of dipole and interfacial states, the heterojunction band structure of the ZnO/Al_2O_3 can be constructed by the



Materials	Band gap (eV)	Electron affinity (eV)	References
Al_2O_3	6.66 ~ 6.9 eV	1.21 ~ 2.58 eV	37-39
ZnO	3.37 eV	4.29 eV	40

Figure 3 | (a) Schematic diagram showing the structure and band diagram of the ZnO/Al_2O_3 superlattice TFTs. And band gap and electron affinity of Al_2O_3 and ZnO based on referece 38–40. Transfer curves of oxide TFTs using (b) single ZnO channel and (c) ZnO/Al_2O_3 superlattice channel.

Anderson model in zero bias. The conduction band offset ($\Delta E_c = \chi_{ZnO} + \chi_{Al2O3}$) between ZnO and Al_2O_3 is estimated to show the value of 1.71–2.46 eV. In the ZnO/Al_2O_3 superlattice structures, the electrons can be confined in the potential well of ZnO, because of the high conduction band offset between ZnO and Al_2O_3. Thus, the ZnO/Al_2O_3 superlattice film is expected to induce high electron movement along the in-plane direction, due to the quasi-two-dimensional nature of the electrons confined in the ZnO well. In the bottom-gate TFT devices with top-contact, the current path of carriers between the source and drain was formed through both out-of-plane and in-plane relative to the superlattice channels. The current density along the out-of-plane of the superlattice films is strongly dependent on the thickness of the Al_2O_3 insulating barrier layers. The carriers can migrate along the vertical direction in superlattice structures through direct tunneling due to the ultrathin barrier layers (Al_2O_3). With increasing thickness of the Al_2O_3 layer, the current density in the superlattice film decreased, as shown in Figure S1. In particular, the barrier thickness of 7.2 nm significantly suppresses the flow of carriers. Therefore, in order to prevent the abrupt reduction of the out-of-plane current density, the ultra-thin Al_2O_3 layers for the effective carrier tunneling should be used as a barrier layer in the superlattice films.

Figures 3(b) and (c) show the transfer curves for the oxide TFTs with single ZnO and ZnO/Al_2O_3 superlattice channels. The threshold voltage (V_{th}), subthreshold swing (*SS*), and field effect mobility (μ_{FE}) values for the single ZnO TFT were 1.2 V, 0.7 V/dec., and 4.8 cm^2/Vs, respectively. In contrast, the ZnO/Al_2O_3 superlattice TFT shows considerably enhanced field effect mobility of 27.8 cm^2/Vs and low *SS* values of 0.3 V/dec. The μ_{FE} of the superlattice is rather high, even compared to the InGaZnO TFTs fabricated by the same method. In addition, the off-current of the ZnO/Al_2O_3 superlattice TFT has a value lower by about one order than that of the single ZnO TFT, which is due to the Al_2O_3 barrier layers inserted into the superlattice channels. As a result, the on-off current ratio (I_{on-off}) of the superlattice TFT measured at V_d = 10 V shows quite a higher value ($\sim 10^9$) than that of the single ZnO TFT ($\sim 10^7$). Although the out-of-plane current density for the superlattice channels decreased, the mobility of charge carriers for the in-plane direction in the superlattice channel can be improved by achieving high crystallinity of the ZnO and confining the electron transport to the ZnO well layers. If the thickness of the ZnO layers increases in the superlattice films, it is expected that the current density along the in-plane direction is significantly enhanced by increasing the mobile charge carriers, as shown in Figure S2(d). On the other hand, the current density along the out-of-plane direction shows an increase of only ~20%. This indicates that the out-of-plane current density is mostly dependent on the thickness of the Al_2O_3 barrier layer, because the current flow is generated by tunneling through the Al_2O_3 barrier layers. As a result, the superlattice channels induce high carrier mobility along the in-plane direction. However, with increasing thickness of the ZnO layers, high in-plane current density leads to high off-current in the superlattice TFTs (Figure S2) and the charge in the quantum effect. Consequently, the thickness of the ZnO layers should be optimized for the fabrication of the ZnO/Al_2O_3 superlattice TFTs with high performance.

The *SS* value is related to the total charge trap density in the bulk channel layer or at the interface between the channel and dielectric layers. As shown in the HRTEM and DP results of Figure 2, the crystallinity of the ZnO layers in the superlattice structure was improved by the insertion of the Al_2O_3 layers. In the photoluminescence analysis (Figure S3), we found that the intensity of the deep-level emission related to the defect density in ZnO[41] is decreased in the superlattice thin film compared to that of single ZnO. Also, the FWHM of the band-edge emission was reduced in the superlattice thin films [Figures S3(b) and (c)]. These results reveal that the superlattice film has reduced defect density, compared to single ZnO thin film. Therefore, the reduced *SS* value in the superlattice TFTs is ascribed to the improved crystallinity of the ZnO.

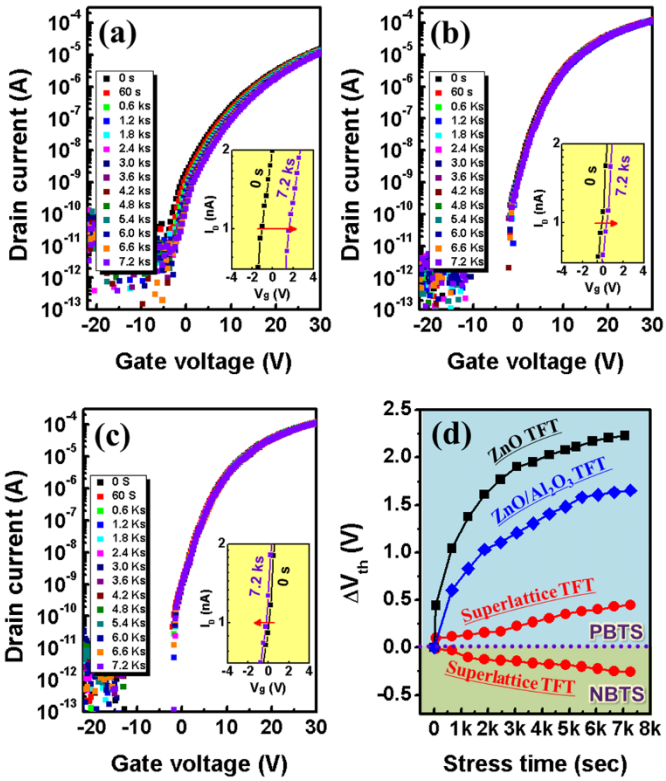


Figure 4 | Variation of transfer curves for the TFT devices measured as a function of gate bias stress time at fixed temperature (60°C). (a) positive gate bias stress (+30 V) for ZnO TFT, (b) positive gate bias stress (+30 V) for ZnO/Al_2O_3 superlattice TFT, and (c) negative gate bias stress (−30 V) for ZnO/Al_2O_3 superlattice TFT. (d) Summary on V_{th} shift of TFT devices induced by gate bias stress for the TFTs with single ZnO, bilayer ZnO/Al_2O_3, and superlattice channels.

The gate bias stress tests were conducted for comparative analysis of the device stability of the TFTs with ZnO and ZnO/Al_2O_3 superlattice channels. Constant positive gate bias (+30 V) was applied to the TFT devices at 60°C in dark condition for 2 hours. The variation of ΔV_{th} for single ZnO and ZnO/Al_2O_3 superlattice TFTs is shown as a function of stress time in Figure 4. The ZnO TFT shows a relatively large positive shift in V_{th} by the positive gate bias. However, the ZnO/Al_2O_3 superlattice TFT exhibits highly stable properties, with ΔV_{th} below 0.5 V for 2 hours. Generally, the charge trapping mechanism[10–12] and charge capture[16,18,19] by the adsorption of oxygen molecules in the back channel were responsible for the positive V_{th} shift of the oxide TFTs under positive gate bias stress. The ALD-grown Al_2O_3 layers are proposed as barrier films for gas diffusion, because they are excellent barrier layers for O_2 and water vapor permeation[42]. Moreover, multi-layer structures including Al_2O_3 are proposed for the application of barrier films with ultralow gas diffusion[43]. It is expected that the back channel effect can be reduced by the use of an Al_2O_3 gas diffusion barrier layer in the channels. In order to analyze the passivation effect of the thin ALD-grown Al_2O_3 layers in the devices, an oxide TFT with a channel comprising a bilayer of ZnO/Al_2O_3 (3.6 nm) was tested under the same stress conditions. The result shows improved device instability compared to a single ZnO channel, as shown in Figure 4(d), despite the thin passivation layer. However, the superlattice TFT provided much more stable electrical characteristics than single ZnO and bilayer ZnO/Al_2O_3. Also, the superlattice TFT showed high stability even

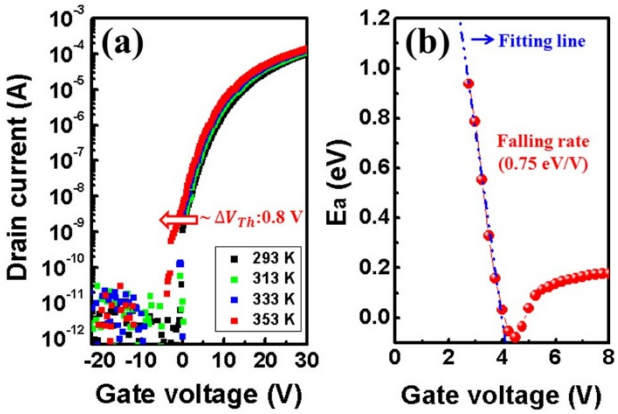


Figure 5 | (a) I-V curve showing the shift of transfer curves of ZnO/Al_2O_3 superlattice TFT as a function of temperature. (b) E_a as a function of V_g for the superlattice TFT, where blue dot-line is the fitting curve indicating falling rate.

in negative gate bias stress conditions (−30 V), as shown in Figure 4(c). As confirmed in the XRD, TEM, and PL results, improved crystallinity contributes to highly stable electrical properties of the ZnO/Al_2O_3 superlattice TFT, together with the passivation effect of the Al_2O_3 layer. As reported for polycrystalline TFT devices, the crystallinity of channel layers is very important for the field effect mobility and electrical stability of devices, because grain boundaries act as electrically active localized states, trapping centers, and adsorption sites for molecules such as oxygen. Thus, it is expected that the ZnO/Al_2O_3 superlattice films will have a lower trap density than single ZnO film, because the superlattice films have shown rather enhanced crystal quality compared with single ZnO films.

The charge trap density of oxide TFTs can be estimated from the variation of transfer curves as a function of temperatures. In the subthreshold region, the current of the devices was well described by the Arrhenius thermal activation model[44]:

$$I_{ds} \approx \alpha (V_g - V_{th}) \cdot \exp\left[-\frac{E_a(V_g)}{kT}\right] \quad (1)$$

where I_{ds}, E_a, and k are the drain current in the subthreshold region, the activation energy, and the Boltzmann constant, respectively. From this model, the E_a can be obtained as a function of gate voltage in the forbidden band-gap from the fitting of the logarithm plot of I_{ds} vs 1/T. Also, the rate of change in E_F with respect to V_g ($|\Delta E_F / V_g|$), defined as the falling rate, is inversely proportional to the magnitude of the total trap density, because all trap sites below E_F should be filled with electrons prior to the change in the E_F level. Figure 5(a) shows the variation of the transfer curves of the ZnO/Al_2O_3 superlattice TFT with increasing temperature from 293 to 353 K. The oxide TFT devices show a negative shift of V_{th} with increasing temperature, which was explained by the generation of thermally activated carriers from traps within the band-gap of the channel. The ZnO/Al_2O_3 superlattice TFT shows a V_{th} shift of only 0.8 V. In addition, as shown in Figure 5(b), the ZnO/Al_2O_3 superlattice TFT exhibits a large falling rate (0.75 eV/V) with a high activation energy of 0.93 eV, which means that the superlattice TFT has a low trap density. It is noted that the V_{th} instability of oxide TFTs using the ZnO channel showed inferior characteristics under bias stress conditions. It is generally accepted that the V_{th} instability of the ZnO TFTs induced by bias stress is due to a high trap site density as a result of oxygen vacancies and low crystallinity. Although superlattice channel structures have a lot of interfaces, the falling rate shows a high value of falling rate, compared with pure ZnO TFTs (falling rate: 0.24 eV/V). Also, The ZnO/Al_2O_3 superlattice TFT showed significantly higher stability and higher field effect mobility than the conventional single ZnO TFTs. As mentioned previously, the mobility enhancement in the ZnO/Al_2O_3 superlattice TFT with high stability was attributed to the charge transport of the electrons confined in the ZnO well layers and the improved ZnO crystallinity.

Discussion

We have introduced a novel channel structure for the realization of high-performance and high-stability in the oxide TFTs, which was based on the periodic superlattice structure of the ZnO/Al_2O_3. The superlattice channel layers consisting of semiconductive ZnO and dielectric Al_2O_3 were alternately deposited by ALD at 200°C. The microstructures of the ZnO/Al_2O_3 superlattice film were analyzed using AFM, XRD, and TEM, and compared with single ZnO thin film. In superlattice films, the ZnO and Al_2O_3 layers had crystalline and amorphous phase, respectively. The single ZnO films grown on the SiO_2/Si had randomly orientated polycrystallinity with island-like growth behavior in the initial stage. In contrast, the ZnO layers in the ZnO/Al_2O_3 superlattice showed improved crystalline phase with relatively c-axis preferred orientation by inserting thin Al_2O_3 layers, where the Al_2O_3 layers promoted layer-by-layer growth of the ZnO layers. As a result, the field effect mobility of the superlattice TFT exhibited higher value than that of the conventional single ZnO TFT, due to the high carrier mobility along the in-plane direction by the electrons confined in ZnO layers, as well as the high crystal quality. Also, the ZnO/Al_2O_3 superlattice channel including the ZnO with high crystallinity induced considerably high electrical stability, due to the low defect density in the superlattice channel and the passivation effect of Al_2O_3.

Therefore, we conclude that the ZnO/Al_2O_3 superlattice channel consisting of periodic semiconductor/insulator arrangement provides a creative route for producing more reliable TFTs, which are needed for the realization of acceptable driving transistors for next-generation displays. In addition, this study provide the feasibility of using chemical vapor deposition based process in the formation of novel channel structure for the high mobility and high stability oxide transistors, because the conventional sputtering system does not allow the delicate control for the nanoscale thickness and the abrupt interfaces.

Methods

Growth of channel layers by atomic layer deposition. The ZnO and ZnO/Al_2O_3 superlattice films were deposited on corning glass and SiO_2 (200 nm)/p^{++}-Si substrates by atomic layer deposition (ALD) at 200°C. The high-purity diethylzinc (DEZn), trimethylaluminium (TMA), and H_2O precursors were used as sources for zinc, aluminum, and oxygen, respectively. The temperatures of cooling circulators for DEZn, TMA, and H_2O were 10°C. These precursors were injected directly into the reaction chamber using nitrogen carrier gas with a flow rate of 100 sccm, which was also used as a purging gas. One cycle for film deposition consisted of exposure to DEZn (or TMA) (0.1 s), a 10 s purge, exposure to H_2O (0.1 s), and a 10 s purge.

Fabrication of TFT devices. Single ZnO and ZnO/Al_2O_3 superlattice channels deposited on SiO_2/Si substrate by ALD were defined by conventional lithography and a wet etching process using H_3PO_4. Then, the source and drain regions were formed by depositing Ti (30 nm)/Au (70 nm) bi-layer electrodes with e-beam evaporator. The width/length of the channel was 500 μm/50 μm. The TFT devices were annealed at 200°C for 2 hours with O_2 atmosphere.

Analysis of characterizations on active layers and TFT devices. The crystal structures of the films were characterized by atomic force microscopy (AFM), X-ray diffraction (XRD, RIGAKU, D/MAX-2500) in θ-2θ scan mode with a copper x-ray source, and transmission electron microscopy (TFM, JEOL JEM-2010). The electrical performance of the TFT devices was measured using an HP4145B semiconductor parameter analyzer. The field-effect mobility (μ_{FE}) in TFT devices was determined by the maximum transconductance at a drain voltage of 0.1 V. The sub-threshold-swing (SS) was extracted from the equation, $SS = (dV_g/dlogI_{DS})$, in the linear region. The threshold voltage (V_{th}) was determined by the gate voltage at a drain current of L/W × 10 nA.

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Author contributions

C.H.A. and H.K.C. designed this work. C.H.A. carried out the experiment and electrical/structural analysis. H.K.C., S.Y.L. and K.S. contributed to analysis and interpretation of results relevant to microstructural and electrical properties. All authors discussed the results and commented on the manuscript.

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