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Isolated nanographene crystals for nano-floating gate in charge trapping memory

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Graphene exhibits unique electronic properties, and its low dimensionality, structural robustness, and high work-function make it very promising as the charge storage media for memory applications. Along with the development of miniaturized and scaled up devices, nanostructured graphene emerges as an ideal material candidate. Here we proposed a novel non-volatile charge trapping memory utilizing isolate and uniformly distributed nanographene crystals as nano-floating gate with controllable capacity and excellent uniformity. Nanographene charge trapping memory shows large memory window (4.5 V) at low operation voltage (± 8 V), good retention (>10 years), chemical and thermal stability (1000 °C), as well as tunable memory performance employing with different tunneling layers. The fabrication of such memory structure is compatible with existing semiconductor processing thus has promise on low-cost integrated nanoscale memory applications.

With the advancement of semiconductor technology, tremendous efforts have been devoted to the development of high reliability, high-density, low power consumption and low-cost nonvolatile flash memory devices for use in consuming electronics products such as Pad, Smartphone, Digital cameras and Mobile Internet Devices^{1,2}. With the process technology further scaling down, conventional materials such as polysilicon used in a typical floating-gate memory structure have encountered great challenges to maintain the device performance and reliability with the miniaturized cell size and high density. Driven by this demand, considerable works have focused on searching candidate materials and structures as the storage mediums in memory devices, e.g. semiconductor/metal nanocrystals and high-k dielectric materials, for modified charge trapping memory (CTM) structure with isolated charge trapping layer³⁻¹¹.

Recently, Graphene has shown potentials to exceed the performance of current conducting floating gate flash memory technology by utilizing its exceptional intrinsic properties such as high work function, excellent chemical stability, and low dimensionality¹²⁻¹⁶. To date, graphene flash memory (GFM) with wide memory window at low voltages has been demonstrated¹³. Large-area CVD graphene transferred onto 5 nm-SiO₂ tunnel oxide layer was used as floating gate in these GFM devices. In principle, such floating gate flash memory is less efficient as a single pin-hole in a device would cause device failure. Indeed, insulating graphene oxide flakes is another option as storage nodes for charge trapping flash memory with large memory window¹⁴; however, the poor thermal stability and the incompatible device fabrication issues make graphene oxide less favorable for high performance devices. In this paper, we demonstrate the use of isolated nanographene crystals, for a first time, as the charge storage media for the charge trapping memory (CTM) applications.

Nanographene is disc-shaped graphene with nanoscale size/diameter and monolayer thickness. Isolated and uniformly distributed nanographene crystals show superior charge trapping capacity and excellent reliability. This novel nanographene charge-trapping layer offers several advantages: 1) High performance promising for superintegrated storage by miniaturization. Tunable memory performance can be achieved by control the size/density of nanographene crystals, as well as different high-k tunneling layers in the devices. Besides, abundant edges of nanographene provide additional charge-trapping sites thus largely increasing the charge storage density, which enables nanosized memory devices with low-voltage operation. 2) Chemical and thermal stability. Nanographene on various dielectric layers is very stable even upon high temperature annealing. 3) Low-cost and compatibility with CMOS technology. Nanographene can be directly grown on various high-k dielectric layers at

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low temperature with good uniformity in wafer scale by a simple and cheap gas-phase deposition system. Both the growth and device fabrication process are compatible with existing CMOS technology.

Results

Controlled growth of nanographene via remote plasma-enhanced chemical vapor deposition (RPECVD). Nanographene was grown by a remote plasma-enhanced chemical vapor deposition (RPECVD) approach as reported in our previous papers^{17,18}. The RPECVD growth of nanographene follows a van der Waals growth mode, as the surface of two-dimensional layered materials (such as graphene, MoS₂, BN) displays no dangling bonds and only weak van der Waals like interaction to the substrate^{19–21}. Compared with 3D materials grown via chemical vapor deposition, this van der Waals growth of layered 2D material allows precise control of growth from nucleation and formation of the first monolayer.

The substrate plays an important role during the growth of nanographene. Substrates used in our experiments are thermally oxidized silicon (heavily doped, n++) with SiO₂ layer thickness of 4 nm; the surface roughness is 0.2 nm. Therefore, nanographene crystals instead of graphene monocrystalline flakes were formed on these surfaces due to the large lattice mismatch. The density of nanographene is decided by the density of nuclei. During a thermal kinetic

growth process, the density of nuclei has a saturated maximum value when the density of metastable nuclei reaches to equilibrium within a certain time. The saturated density is independent on the growth rate while dependent on the growth temperature. Thus we can control the density and size by tune the growth time and growth temperature. Under optimized growth parameters, nanographene crystal arrays can be grown at high density while with good uniformity over a relatively large area (4 inch wafer).

Fig. 1a shows the atomic force microscopy (AFM) topography images of the nanographene samples (#1–5) with different growth conditions. From both height and phase images, we can see that these graphene nanocrystals are homogeneously distributed on the SiO₂ surface with sizes varied from several nanometers to hundreds of nanometers and densities varied from 10¹⁰/cm² to 10¹¹/cm². The height of as-grown nanographene is 0.4–0.7 nm, equivalent to a monolayer thickness. Fig. 1b shows Raman spectra of these samples and Fig. 1c plots the corresponding diameter and density of sample #1–5. The high D peaks and the appearance of D' edges (1620 cm⁻¹) reveal strong defect scattering at abundant edges of nanographene^{22,23}. The size dependence of effective area ratio and Raman $I_{D'}/I_G$ ratio as depicted in Fig. 1d are fingerprints for the edges in nanographene arrays²⁴. Small-sized nanographene with higher density shows larger $I_{D'}/I_G$ ratio and lower effective area ratio than

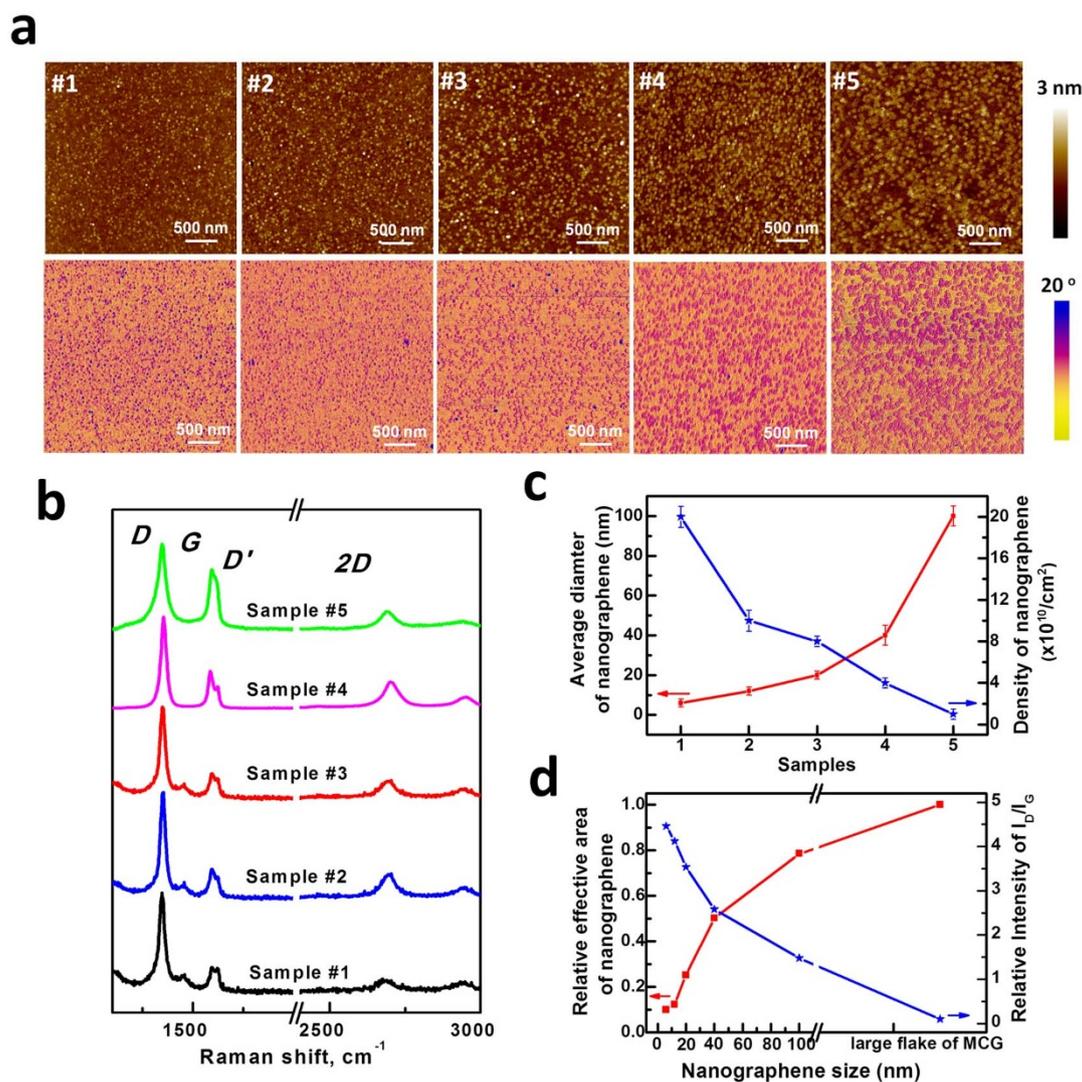


Figure 1 | Nanographene crystals with controlled sizes and densities. (a) and (b) AFM height/phase images and Raman spectra of nanographene samples #1–5 with controlled growth conditions. (c) The corresponding diameter and density of sample #1–5. (d) Size dependence of effective area ratio and Raman $I_{D'}/I_G$ ratio, which reveal the edge proportion in nanographene. Scale bars: 500 nm.



large-sized nanographene with lower density. Hence, the properties of nanographene can be modulated by these edges.

Charge trapping effect in nanographene. In order to investigate the feasibility of these isolated nanographene as charge trapping layer for memory applications, we employed the scanning Kelvin probe microscopy (SKPM) studies. SKPM is a probing technique capable of directly mapping the surface potential variations from the contact potential difference (CPD) between the sample surface and the metallic probe^{25–27}. Charges stored within nanographene can be detected from the change in the surface potential when the SKPM tip scans the surface of the blocking oxide layer above nanographene crystals⁷. Fig. 2a shows a schematic set-up of the SKPM measurements for the $\text{Al}_2\text{O}_3/\text{nanographene}/\text{SiO}_2$ structure. 4-nm SiO_2 was used for the charge tunneling layer and 4-nm Al_2O_3 deposited by atomic layer deposition (ALD) was used for the blocking layer. The zoom-in AFM image shows a typical as-grown sample with nanographene uniformly distributed on SiO_2 substrate with average size of ~ 8 nm and density of $\sim 1 \times 10^{11} \text{ cm}^{-2}$.

The SKPM measurements include two-steps: charges injection and CPD measurements. (Please see the Supplementary Information for details). Fig. 2b shows a typical real-space SKPM imaging of both programmed and erased states created on $\text{Al}_2\text{O}_3/\text{nanographene}/\text{SiO}_2$. The program operation was performed within an area of

$1 \times 1 \mu\text{m}^2$ with -3 V injection bias applied to the bottom Si substrate. Electrons were trapped in the nanographene by tunneling through the 4-nm SiO_2 . Note that, the bias polarity was reversed for device programming/erasing operations^{6,7}. In a following process, the center $500 \times 500 \text{ nm}^2$ area was erased by applying $+3$ V bias. During this process, originally trapped electrons were recombined with holes and then a trapped hole state was finally created. In order to exclude the possibility that the SKPM image contrast may originate from the induced charges trapped in the $\text{Al}_2\text{O}_3/\text{SiO}_2$ insulating layers other than in nanographene, $\text{Al}_2\text{O}_3/\text{SiO}_2$ structure without embedded nanographene was checked as a control sample. Same bias conditions were used and very weak charging was observed when applying programming or erasing bias. For more data, see supplementary Fig. S1. Thus we confirm that most of the contrast changes came from the charges stored in nanographene.

The cell distribution in nano-floating gate memory devices depends mostly on the homogeneous density distribution of nanocrystals^{9,10,28}. Following a similar process, we created a uniform pattern of trapped electron or hole arrays as demonstrated in Fig. 2c with 6×6 programmed (“1”) and erased (“0”) states. Here, the variation of nanographene number density in the defined area of 500 nm^2 is less than 5% as determined from the analysis of AFM phase image, and the result shows that the variation of erased and programmed cells distribution is also less than 5%. Therefore, these preliminary

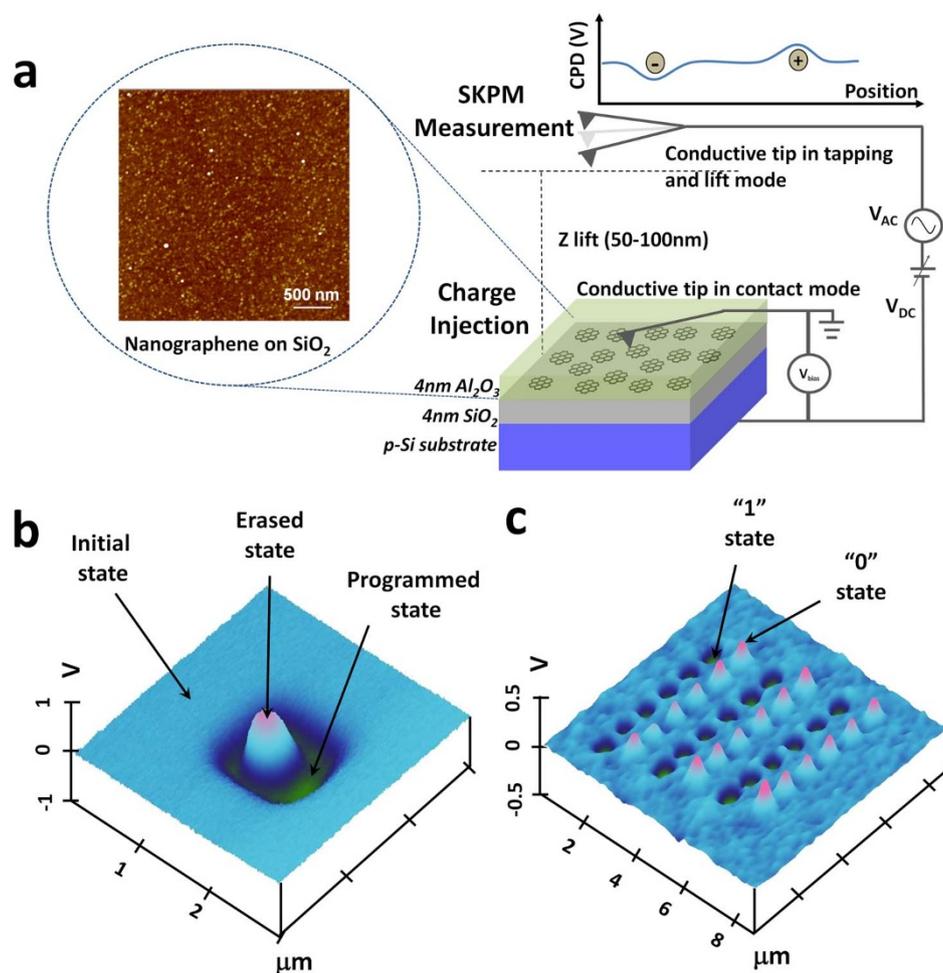


Figure 2 | SKPM characterization of charge trapping effect in nanographene. (a) Schematic diagram of the SKPM measurement process for the $\text{Al}_2\text{O}_3/\text{nanographene}/\text{SiO}_2$ structure. Inset: a typical AFM image of the as-grown nanographene. (b) and (c) 3D SKPM images of the $\text{Al}_2\text{O}_3/\text{nanographene}/\text{SiO}_2$ structure with programmed and erased states within a single cell and a uniform 6×6 array, respectively. The size of each cell is $500 \times 500 \text{ nm}^2$ with a spacing of 500 nm in the array. Charges were injected at room-temperature by 256 scan lines at $2 \mu\text{m}/\text{s}$ tip scan speed with sample bias of ± 3 V. The applied bias between the tip and the surface can form a vertical electrical field of $6 \text{ MV}/\text{cm}$. Note that, the bias polarity was reversed for device programming/erasing operations.



data clearly show that nanographene can yield charge trapping memory characteristics with localized charge storage for high-density storage at the nanoscale.

Size/Density-dependent charge trapping capacity of nanographene. Usually, the characteristics of nanocrystal memories are directly related to the nanocrystal size/or density, shape and configuration^{4–8}, thus it is important to investigate these structural effects. In order to study the structural effect on the charge trapping capacity of nanographene, we carried out SKPM measurements to quantify the charge trapping density in a local back-gated nanographene device as shown in the inset of Fig. 3. Without the blocking high-*k* oxide layer, the variation in surface potential is determined by the carrier concentration variation in nanographene. The change of carrier concentration is ascribed by the Fermi level shift due to the electric field effect induced charge doping, which is well quantified by the density of state (DOS) of graphene^{29–31}. The measured CPD values were used to estimate the charge trapping capacity of nanographene. Considering the test environment is lightly negatively charged, we use the electron injection to avoid the charge recombination of nanographene into the environment. Besides, the loss of some charge during the first tapping-mode scanning of the tip can also be ignored.

Fig. 3 presents the CPD values and corresponding calculated electron densities extracted from the SKPM measurements of samples #1–5 after low electrical field charging ($E: -5 \text{ MV/cm}$, charged area: $1 \times 1 \text{ } \mu\text{m}^2$), together with exfoliated large graphene flakes and silicon nanocrystals for comparison (See more details in the Supplementary Information). The total trapped electron density in smaller nanographene samples are obviously higher than that in bigger nanographene samples, indicating more available trapping sites in the smaller sized nanographene samples. The size dependent total charge trap density agrees well with the measured edge densities by Raman scattering. When the diameter decreases, the saturated density increases, and the available edge defect states in nanographene would increase and thus supply more trapping sites for charges. These results reveal that smaller nanographene is more favorable for higher trapping density than graphene flakes. We deduce that the edge defect states play an important role in contributing the charge trapping performance of nanographene¹⁴; hence, the stored charge densities in nanographene/SiO₂ structures can be tuned by changing the nanographene sizes and densities.

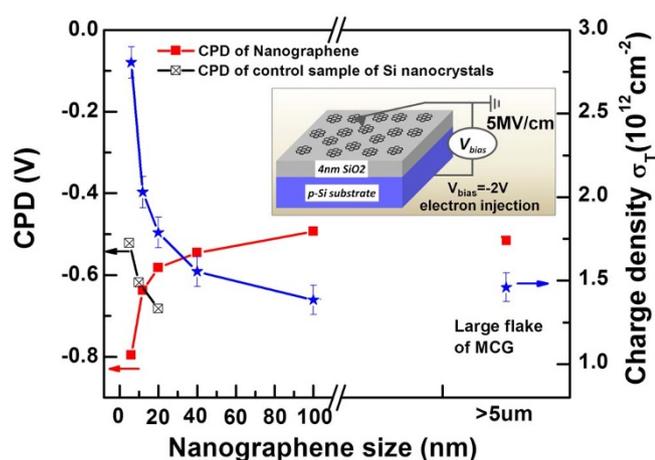


Figure 3 | Size/density depended charge trapping capacity in nanographene. The CPD values and corresponding electron densities extracted from the SKPM measurements of samples #1–5, together with exfoliated large graphene flakes and silicon nanocrystals for comparison. **Inset**, Sketch map of a local back-gated nanographene device for surface-potential measurement.

It is worthy of noting that the size-dependent charge trapping capacity of nanographene, as depicted in Fig. 3 with dotted marks, has an opposite trend as compared to that of silicon nanocrystals, which has been well explained by the size-related quantum effect resulted charge loss in semiconductor nanocrystal flash memories³². As the size of semiconductor nanocrystal decreases down to its Bohr radius (e.g. Si $\sim 11 \text{ nm}$), the total quantum confinement energy increases and available density of states decrease, leading to less charges being injected and stored. Unlike semiconductor nanocrystals, nanographene film is a zero band-gap semiconductor with a Bohr radius around 0.74 nm (which is comparable to noble metals, e.g. Au $\sim 0.5 \text{ nm}$) and shows an ambipolar conducting behavior with weak gate modulation^{17,18}. Even when the size of nanographene shrinks down to a few nm, there is only very small band-gap induced by the quantum size effect^{33,34}. Consequently, its high work function and small Bohr radius make it a favorable charge trapping material rivaling metals nanocrystals.

Device performance and compatibility. Based on the above SKPM analysis, nanographene shows highly controllable charge trapping capacity with large trapping density, ultra-thin thickness, and well uniformity. In order to further testing the compatibility of this structure with CMOS compatible process, we fabricated metal/Al₂O₃/Nanographene/SiO₂/Si (MANGOS) memory structure by standard atomic layer deposition (ALD), rapid thermal annealing (RTA), UV-lithography, e-beam evaporation and lift-off processes. The schematic cross-section of the device and its energy band diagrams before and after programming are shown in Fig. 4a. Typical Raman G-peak of nanographene before and after RTA at 1000°C are shown in Fig. 4b, confirming that the nanographene encapsulated in Al₂O₃ is stable even at high temperatures. From the broadened D-peak and 2D-peak, we may deduce that nanographene crystals were changed into oxygen-termination instead of hydrogen-termination after annealing. However, lattice inside nanographene keeps as evidenced from the Raman data shown in Fig. 4b. The edge of nanographene plays a very important role in the charge trapping, but we found that this trapping effect depends less on the termination types.

The high frequency (100 kHz) capacitance-voltage (CV) characteristics of MANGOS under different low sweep voltages are shown in Fig. 4c. The CV curves of MANGOS at high sweeping gate voltage are shown in Fig. S6. Compared with the control sample showing no memory window, CV curves of MANGOS reveal a large flat-band voltage (V_{fb}) shift under a dual-direction gate voltage sweeping ($V_{fb} = 4.52 \text{ V}$, at $\pm 8 \text{ V}$). The large memory window at low-voltage further proves that the nanographene dominate the charge storage capability. For previous nanocrystal memory devices, the estimated electrons stored in a single nanocrystal on average are usually less than 10. High-density charge storage and less fluctuation between individual cells can be achieved by increasing the density of nanocrystals. However, high density nanocrystal would also lead to highly charge leakage or directly tunnel through the surrounding oxide^{2,9,10}. Nanographene memory devices might have advance in overcoming this limitation as the single nanographene with size of $6\text{--}8 \text{ nm}$ can store over 15 electrons with sufficient spacing-gaps.

Fig. 4d depicts the noncycled retention characteristics of MANGOS at room temperature. The cycled retention characteristic of MANGOS at both room temperature and high temperature is shown in Fig. S7. Generally, retention-time more than 10 years is required before the device loses 50% of stored charge¹. The large barrier height ($\sim 3.85 \text{ eV}$) of nanographene/SiO₂ (as shown in Fig. 3a) and the low electric-field across the tunneling layer under retention state make direct tunneling the most probable charge loss mechanism^{2,13}. A $\sim 2.52 \text{ V}$ memory window shrinks to $\sim 2.23 \text{ V}$ after 10^4 s and a charge loss of 44% in MANGOS after 10 years' operation is predicted from the experimental data. However, due to some overlap of the

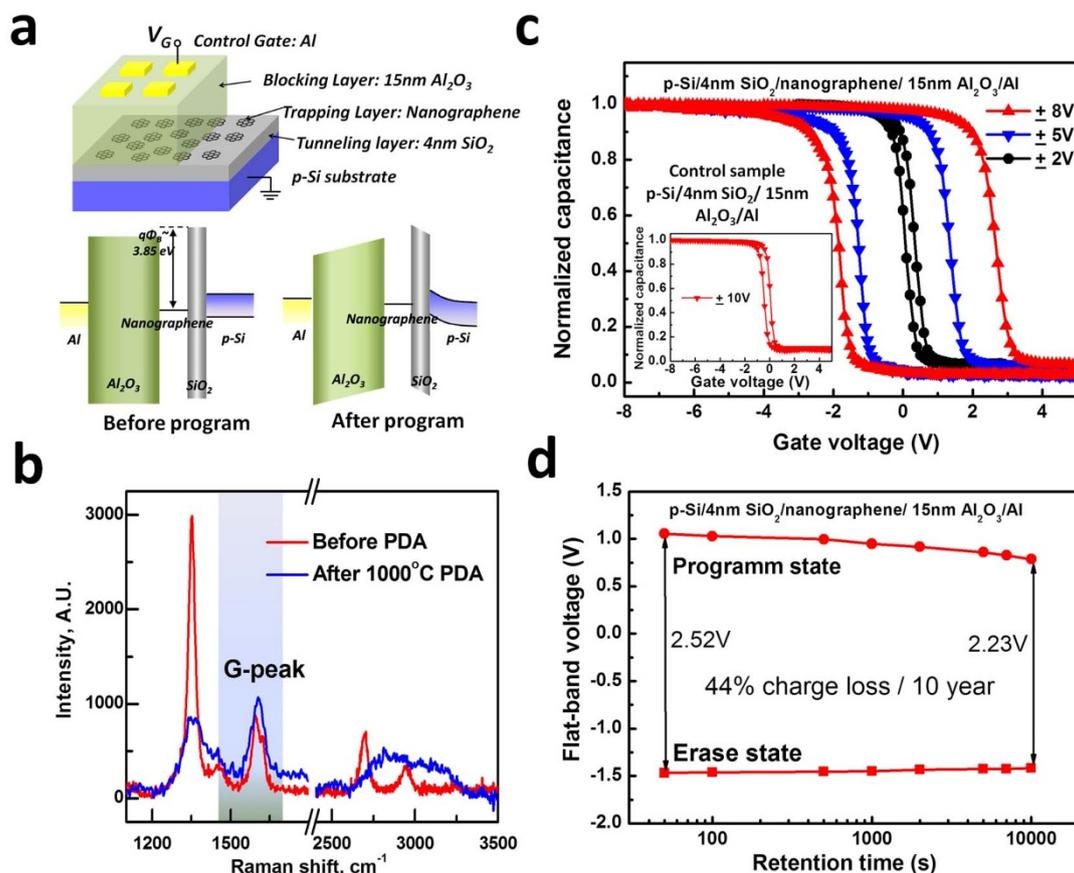


Figure 4 | CV measurements for the MANGOS structure. (a) Schematic cross-section of the MANGOS device structure (up) and the corresponding band diagram of the retention states before and after program operation (down). The blocking layer is 15-nm Al_2O_3 deposited by ALD. After the deposition of the blocking layer, RTA annealing at 1000°C for 1 min in N_2 ambient was carried out. 200-nm Al gate was used as the gate electrode. Control sample of metal/ Al_2O_3 / SiO_2 /Si (MAOS) structure was also prepared by the same process. (b) Raman spectra of nanographene before and after RTA. (c) High frequency CV characteristics of MANGOS under different gate voltage sweepings. (d) Data retention for MANGOS.

nanographene dots as well as the quality of blocking Al_2O_3 layer, the high-temperature retention after 1000 cycled operations shows a charge loss of 55%. In addition, the characteristics of program/erase speed and endurance for MANGOS device are illustrated in Fig. S8. The P/E curves shows 4.5 V V_{th} shift with ± 12 V operation voltage pulses at 10 ms. No obvious degradation in device performance after 1 K P/E cycles is observed. The device uniformity test is shown in Fig. S9. (Please see the Supplementary Information for details).

Discussion

Loss of storage is typically a result from charge tunneling through the tunneling oxide, and the tunneling rate depends on the thickness and the barrier height of the oxide^{9–11,28,35,36}. In order to decrease the charge loss, many high-k materials have been developed in charge trapping flash memory devices as tunneling layers to achieve larger memory windows along with low retention degradation. Here, we will show another significant advantage of nanographene as nano-floating gate by in cooperation with high-k material (Al_2O_3 , HfO_2 , etc.). The Raman spectra of as-grown nanographene on the Al_2O_3 and HfO_2 layer are shown in Fig. S10. Fig. 5a and 5b show the CV characteristics of the metal/ Al_2O_3 /NG/ Al_2O_3 /Si (MANGAS) and metal/ HfO_2 /NG/ HfO_2 /Si (MHNGHS) memory devices, respectively, together with corresponding control samples shown in their insets. Both the MANGAS and MHNGHS structures exhibited an improved flat-band voltage (V_{fb}) shift under low-voltage as compared with those for the control samples. As the programming energy barrier height is controlled by the tunneling oxide, the memory windows of nanographene with different tunneling layers are

different under the same sweeping voltage as depicted in Fig. 5c. Due to the high dielectric constant of the tunneling oxide, the MHNGHS structure shows obviously improved retention with a charge loss of 28% after 10 years as shown in Fig. 5d. It shows that the Nanographene structure is compatible with the high-k materials, which is very promising in further performance enhancement of the memory.

Comparing with existing semiconductor nanocrystals or metal nanoparticles based charge trapping memory devices^{9–11}, our nanographene charge trapping memory structures have advantages. Semiconductor nanocrystals are more favorable for industry in terms of the fabrication compatibility with CMOS technologies; however, their relatively large sizes limited their use for miniaturized device applications as very small semiconductor nanocrystals are not good for charge storage due to the quantum confinement effect. Metal nanoparticles, usually dealing with expensive cost and high-work-function metals such as Au and Pt, can be very small while keeping high charge storage capacity; however, the fabrication process is not compatible with CMOS technologies. Besides, it is also challenging to control the sizes, shapes, and thermostability of these metal nanoparticles, thus fluctuations of the device performance between individual devices become severe especially when reducing the devices' sizes to nanoscale. In contrast, nanographene not only possesses the advantages of metal nanocrystals, but also shows low cost, highly charge storage capacity, high temperature stability and wafer-scale homogeneity which can satisfy the nano-miniaturized requirement. Both the wafer-scale growth of nanographene and fabrication of the devices are compatible with modern semiconductor-based processing.

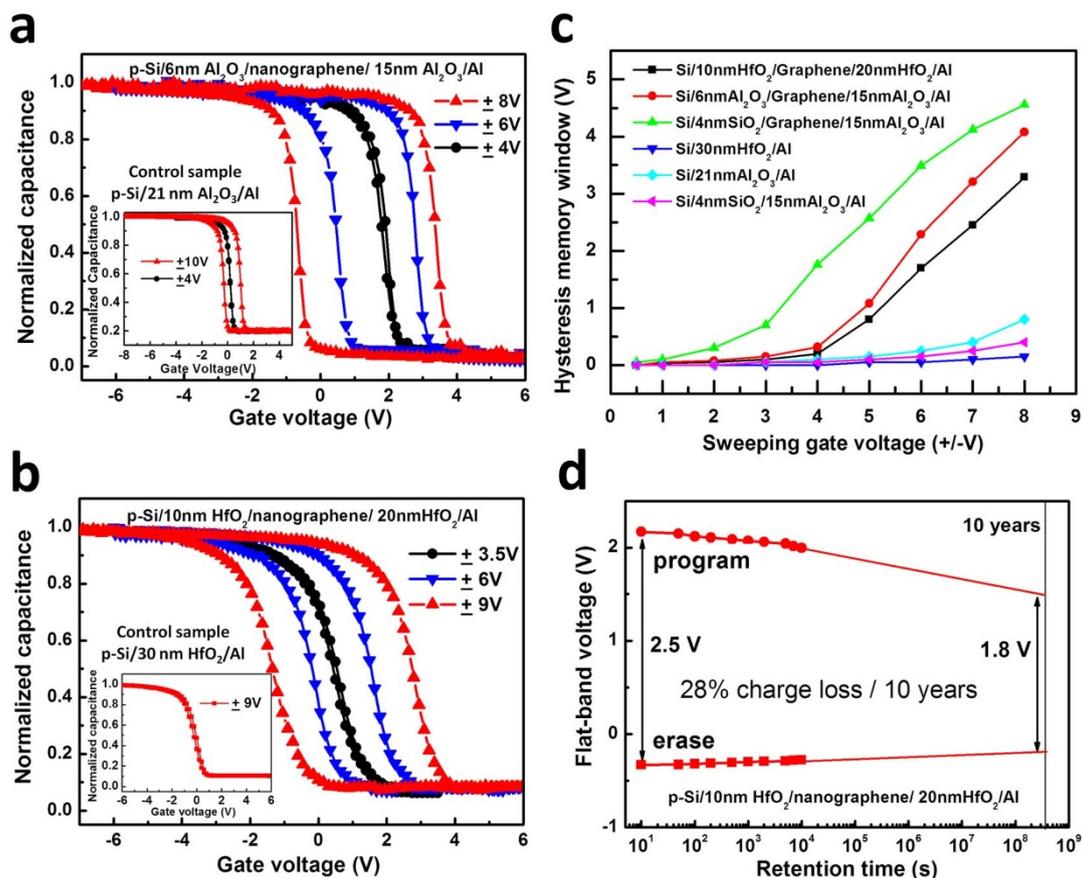


Figure 5 | Tunable memory performances with different high-k functional layer. (a) and (b) High frequency CV characteristics of MANGAS and MHNGHS memory devices under different gate voltage sweepings. (c) Tunable memory window of nanographene with different tunneling layers. (d) Data retention for MHNGHS with an improved charge loss.

We have demonstrated above that nanographene is a good candidate for charge trapping materials. For real applications, its size has to be reduced as small as possible at the technology node of ~ 30 nm and beyond. For example, assuming that a cell size is $20 \text{ nm} \times 20 \text{ nm}$, only ~ 4 nanographene can be accommodated when the average size is 8 nm, and then V_{th} distributions between cells might be oscillated. We have tried to reduce the average size of nanographene dots by simply reducing the growth time. Preliminary results show that it works but at the cost of sacrificing the density. Another alternative strategy to increase the nanographene density is to stack multilayer nanographene/high-k structures in which nanographene trapped in each layers can be separately prepared. In order to meet the requirement of miniaturized devices, further optimization of the growth parameters needs to be performed in the following research to achieve both small sizes and high densities of nanographene.

In summary, high performance nanographene charge trapping memory devices were developed with large memory window at low operation voltage, acceptable retention, high temperature tolerance (1000°C), and tunable memory performance. The RPECVD growth of nanographene is simple, highly controllable, cheap, and compatible with the current CMOS technology. Standard lithography and etching techniques can be easily used to pattern the nanographene crystals with desired arrays and shapes. Thus, the nanographene crystals are promising for nanoscale integrated high-performance and low-cost non-volatile charge trapping memory applications.

Methods

Preparation of silicon oxide and high-k dielectric layers. Heavily p-doped Si (100) wafers (Radio Corporation of America) were used as the substrates. The SiO₂ layer was thermally grown at 900°C in dry O₂ ambient; the Al₂O₃ layer was deposited by atomic layer deposition (ALD, Thin film system TFS 200 from Beneq) at 200°C with

Trinethylaluminum and H₂O as precursor; the HfO₂ layer was also deposited by ALD at 210°C with Tetrakisdiethylaminohafnium and H₂O as precursor.

Growth and characterization of nanographene. Growth of nanographene was performed by a direct growth process in remote plasma enhanced chemical vapor deposition system using pure methane as the precursor. This low-temperature and catalyst-free growth technique is applicable to various substrates. In this work, different dielectric oxide surface including 4 nm-SiO₂/Si, 6 nm-Al₂O₃/Si, and 10 nm-HfO₂/Si were used. Growth conditions of nanographene are listed below: samples #1–4 (on 4 nm-SiO₂/Si) were done at 100 W RF power, 30 sccm CH₄, 0.2 Torr gas pressure, 1.5 h with different growth temperature (525°C , 535°C , 550°C , 575°C). Larger nanographene samples (sample #10) were prepared by a two-step growth process (nucleation at 525°C for 30 mins then growth at 480°C for 3 hs). Samples on 4 nm-SiO₂/Si, 6 nm-Al₂O₃/Si and 10 nm-HfO₂/Si for devices were grown at 525°C for 1.5 hrs using 100 W RF power, 30 sccm CH₄, and 0.2 Torr gas pressure.

Atomic force microscopy (Nanoscope MultiMode IIIId from Veeco Instruments Inc.) was used for imaging and measuring the morphology, thickness, density and size of nanographene.

Raman spectroscopy (LabRAM HR-800 Raman microscope from Horiba Jobin Yvon) was carried out to characterize the size-dependent edge structures. The excitation laser wavelength is 532 nm. The laser spot size is $\sim 2 \mu\text{m}$ and the laser power is $\sim 1 \text{ mW}$.

SKPM measurement. SKPM was performed in the AFM system (Nanoscope MultiMode IIIId from Veeco Instruments Inc.) with metalized probes (PtIr coated silicon probe with a typical tip radius of $\sim 30 \text{ nm}$). The spring constant and resonant frequency of tip is $\sim 1.5 \text{ N/m}$ and 60 kHz, respectively. Potential imaging was realized under the lift-mode with a pre-defined lift height $\Delta Z = 50 \text{ nm}$. During the scanning, an AC bias V_{ac} at frequency close to the AFM tip resonance frequency is applied between the tip and the sample, in combination with a DC voltage V_{dc} . The force along the z axis is given by

$$F_z = F_{dc} + F_{1w} + F_{2w} = -\frac{1}{2} \frac{\partial C}{\partial Z} [(V_{dc} - V_{CPD})^2 + \frac{1}{2} V_{ac}^2] - \frac{\partial C}{\partial Z} (V_{dc} - V_{CPD}) V_{ac} \sin \omega t + -\frac{1}{2} \frac{\partial C}{\partial Z} V_{ac}^2 \cos 2\omega t'$$



where C is the entire capacity between the tip and the surface, $V_{CPD} = (\chi_{tip} - \chi_{sample})/e$ is the contact potential difference between the tip and the sample. If the applied bias V_{dc} is equal to V_{CPD} , the vacuum levels of the tip and the sample becomes the same, and the second term F_{1w} component signal becomes zero. Therefore, we can obtain the intended potential by adjusting dc offset bias V_{dc} to nullify the F_{1w} component signal.

Devices fabrication and measurement. For MANGOS device, the tunneling layer was a 4-nm SiO_2 and the blocking layer was a 15-nm Al_2O_3 . Before electrodes patterning, post annealing process for the above device structures was carried out in N_2 ambient at 1000°C for 1 min by rapid thermal annealing (RTA). The RTA process is necessary for improving the qualities of ALD films by removing possible impurities, which could lead to additional traps for charges. The Al electrodes with a gate area varied from $60 \times 60 \mu\text{m}^2$ to $500 \times 500 \mu\text{m}^2$ were fabricated by UV-lithography (MicroTec MA6 Mask Aligner from Karl Suss) followed by electron beam evaporation and lift-off process. Similar device structures were also fabricated, in which the nanographene was embedded in different high-k matrix. For MANGAS device, the tunneling layer was a 6-nm Al_2O_3 and the blocking layer was a 15 nm Al_2O_3 . For MHNGHS device, the tunneling layer was 10-nm HfO_2 and the blocking layer was a 20-nm HfO_2 . The corresponding control samples were simultaneously fabricated without nanographene.

Electrical measurements were performed using a Keithley 4200 semiconductor characterization system combined with an Agilent C-V 590, and a probe station. The holding time was 0.1 s during the C-V measurements.

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Author contributions

G.Z. designed the research; R.Y. performed the growth of nanographene and SKPM measurements; R.Y., C.Z. and J.M. performed the fabrication and CV measurements for the devices; M.C. helped on SKPM measurements; R.Y., C.Z., J.M., Z.H., M.C., D.L., W.Y., D.S., M.L. and G.Z. analyzed the data; R.Y. and G.Z. wrote the paper, and all authors commented on the manuscript.

Additional information

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