On the conference circuit

Technology breakthroughs at the 2018 IEEE International Electron Devices Meeting.

Conferences remain central to research communities across science and engineering. But the exact role they play in reporting peer-reviewed research can vary. For some, conferences are a place to discuss work that has been, or will shortly be, published in a journal; for others, they are, together with a conference proceedings paper, a place to report preliminary work that will later appear in a journal; and for others still, the conference, and related conference proceedings, are the only venue required.

At *Nature Electronics*, like the other Nature Research journals, we are happy to consider work that contains material previously published in a conference proceedings paper (our specific policy can be found here). But we would be looking for the submission to offer a substantial extension over the proceedings paper, be it in results, methodology, analysis, conclusions and/or implications. The proceedings paper should also be appropriately cited in the submitted manuscript.

A key conference for reporting developments in semiconductor and electronic device technology is the IEEE International Electron Devices Meeting (IEDM), which is now in its 64th year and took place in San Francisco in December. In this issue of *Nature Electronics*, we highlight some of the breakthroughs reported at the 2018 meeting.

To begin, we have an interview with Kirsten Moselund and Rihito Kuroda, publicity chairs of the 2018 IEDM. Reflecting on the history of the event, they note that Dennard scaling — principles for the scaling of metal–oxide–semiconductor field-effect transistors (MOSFETs) — was introduced at the 1972 meeting, and Moore's law — the prediction that the number of components in an integrated circuit would approximately double every two years — was reported at the 1975 meeting. Reflecting on this year's meeting, they note that neuromorphic devices have emerged as a central theme, and that developments in memory devices are also increasingly prominent.

Memory innovation is the focus of the first of our highlighted articles from the meeting. Magnetoresistive random access memory (MRAM) is an emerging non-volatile technology that stores information in magnetic elements known as magnetic tunnel junctions. At the 2018 IEDM, Intel report on integrating MRAM with their 22-nm fin field-effect transistor (FinFET) technology, work Arijit Raychowdhury of Georgia Institute of Technology discusses in a News & Views article. And the capabilities demonstrated by the Intel team are impressive: a 200 °C ten-year retention and endurance of more than 10^6 cycles.

Such embedded memory could be used to develop energy-efficient computing for use in applications such as the Internet of Things. With similar aims and applications in mind, Zhixin Alice Ye and colleagues at the University of California, Berkeley report at IEDM the development of digital integrated circuits using microelectromechanical relays, work we highlight with a News & Views article from Núria Barniol of Universitat Autonoma de Barcelona.

MOSFETs are the basic switching components of electronics, but the continued scaling of the devices has created increasingly pressing power consumption issues. As a result, a range of alternative devices are currently being explored. Mechanical relays could potentially offer zero off-state leakage current and sharp switch characteristics, and are thus of particular interest in the pursuit of low-power computing applications. Using self-assembled molecular coatings, which lower contact adhesion in the relays, Ye and colleagues have created integrated circuits that can reliably operate with very low supply voltages.

IEDM has a strong mix of academia and industry (around two thirds of the attendees are, in fact, from industry), and in our final two highlights from the conference, we cover work from both camps. From academia, there is a report from Kaustav Banerjee and colleagues at the University of California, Santa Barbara on developing interconnects made from graphene nanoribbons. Notably, the fabrication process they use is compatible with complementary metal–oxide–semiconductor (CMOS) technology. Then from industry, there is a report from Geumjong Bae and colleagues at Samsung Electronics on the fabrication of multibridge-channel field-effect transistors at the 3 nm technology node. In such transistors, the channels are made from multiple separated nanosheets that are encapsulated by the gate (the approach is thus often referred to as gate-all-around technology). The Samsung team show that with their gate-all-around technology, key device performance metrics are maintained or improved, compared to existing FinFET technology. The devices are also fabricated using 90% of the FinFET fabrication process, which suggests that it would be relatively straightforward to migrate to the new process. ❐

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