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Monolayer MoS_2 field-effect transistors patterned by photolithography for active matrix pixels in organic light-emitting diodes

Hyeokjae Kwon[1], Sourav Garg[2], Ji Hoon Park[1], Yeonsu Jeong[1], Sanghyuck Yu[1], Seongsin M. Kim[2], Patrick Kung[2] and Seongil Im[1]

Two-dimensional molybdenum disulfide (MoS_2) has substantial potential as a semiconducting material for devices. However, it is commonly prepared by mechanical exfoliation, which limits flake size to only a few micrometers, which is not sufficient for processes such as photolithography and circuit patterning. Chemical vapor deposition (CVD) has thus become a mainstream fabrication technique to achieve large-area MoS_2. However, reports of conventional photolithographic patterning of large-area 2D MoS_2-based devices with high mobilities and low switching voltages are rare. Here we fabricate CVD-grown large-area MoS_2 field-effect transistors (FETs) by photolithography and demonstrate their potential as switching and driving FETs for pixels in analog organic light-emitting diode (OLED) displays. We spin-coat an ultrathin hydrophobic polystyrene layer on an Al_2O_3 dielectric, so that the uniformity of threshold voltage (V_{th}) of the FETs might be improved. Our MoS_2 FETs show a high linear mobility of approximately 10 $cm^2 V^{-1} s^{-1}$, due to a large grain size around 60 µm, and a high ON/OFF current ratio of 10^8. Dynamic switching of blue and green OLED pixels is shown at ~5 V, demonstrating their application potential.

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INTRODUCTION

Molybdenum disulfide (MoS_2), a two-dimensional (2D) transition metal dichalcogenide (TMD) semiconductor has attracted much attention from many researchers owing to its interesting physical properties and potentials for future nanoscale electronics.[1–4] Like graphene, those 2D semiconductors are easily formed by mechanical exfoliation using scotch tapes in general, while it also displays high ON/OFF current ratio and good subthreshold swing in a field-effect transistor (FET) form with *n*-type conduction unlike graphene, which shows no bandgap.[5–14] Since 2D MoS_2 obtained by mechanical exfoliation limits the length scale only to a few micrometers, researchers have studied on how to fabricate such 2D MoS_2 in a large scale,[15–20] which would open the gate toward more practical applications enabling conventional photolithographic device/circuit patterning. Chemical vapor deposition (CVD) has thus become one of mainstream fabrication techniques to achieve large-scale MoS_2 2D sheets. Many of success on large-scale MoS_2 monolayer sheets have been reported.[21–23] Yet, reports on conventional photolithographic patterning for large-scale 2D MoS_2-based devices with decently high mobilities are still rare,[24–26] to the best of our limited knowledge. For instance, CVD-grown monolayer MoS_2 FETs might have never been used for both switch and driver of organic light-emitting diodes (two FETs in an OLED pixel for active matrix: see the circuit details in Supporting Information Figure S1), while exfoliated TMD-based FETs were barely used once with poor yield as a proof-of-concept-type demonstration.[27] According to previous works, low threshold voltage would be an important issue for OLED pixel switching.[26,27]

In the present work, we have fabricated CVD-grown large-scale MoS_2 FETs with patterned bottom gate and investigated their applications toward analog OLED pixel as low voltage switching and high current driving FETs. In particular, we successfully spin-coated an ultrathin hydrophobic polystyrene (PS) polymer layer on Al_2O_3 dielectric before the CVD MoS_2 monolayer was transferred onto the gate-patterned Al_2O_3 on glass, so that the uniformity of threshold voltage (V_{th}) of FETs might be improved. Our MoS_2 FET shows a linear mobility of ~10 $cm^2 V^{-1} s^{-1}$ and an ON/OFF current ratio of 10^8 as patterned by photolithography on glass, and those values are regarded quite high or comparable to those of previous CVD MoS_2 FETs[28–32] because a single grain of our CVD MoS_2 monolayer appears as large as ~60 µm in side dimension. Among 48 MoS_2-based FETs realized from the same CVD MoS_2 wafer, 38 devices successfully work (yield ~80%) operating at ~5 V with 50 nm-thick Al_2O_3 bottom gate dielectric. Dynamic/static switchings of blue and green OLED pixels were nicely demonstrated using the CVD monolayer MoS_2 FETs.

RESULTS AND DISCUSSION

According to scanning electron microscope (SEM) images of Fig. 1a–c, sufficiently large area and continuous MoS_2 monolayer film was achieved (Fig. 1b). For the CVD growth, we used a single precursor source consisting of MoS_2 powder at a high growth temperature ~800 °C with a temperature of 900 °C for the powder precursor,[33] instead of the combination of MoO_3 and S, which is more often reportedly used (see Methods section for more details).[15–17] From a more magnified view of the film region, a grain boundary is distinguished better as indicated by dashed

[1]Van der Waals Materials Research Center, Department of Physics and Applied Physics, Yonsei University, 50, Yonsei-ro, Seodaemun-gu, Seoul 03722, Korea and [2]Electrical and Computer Engineering, University of Alabama, Tuscaloosa, AL 35487, USA
Correspondence: Seongil Im (semicon@yonsei.ac.kr)

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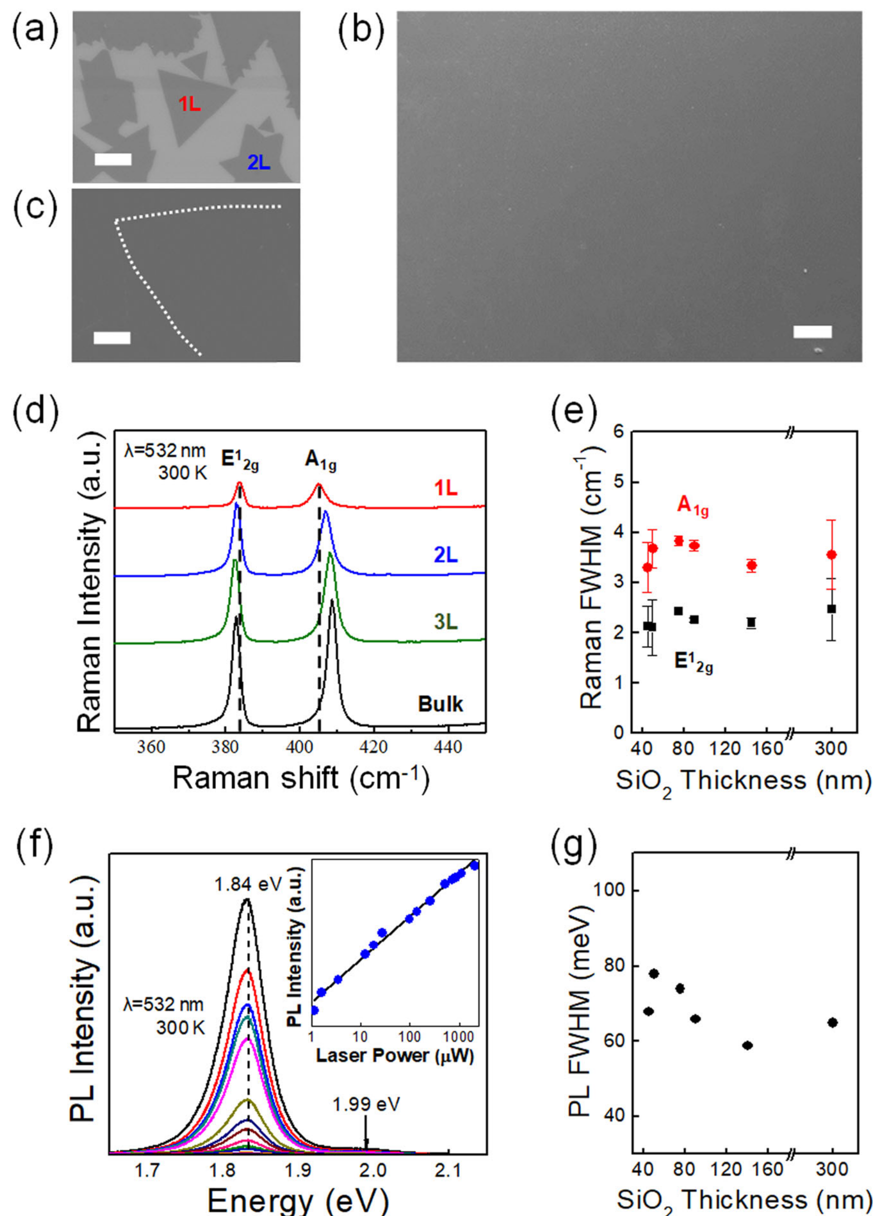

Fig. 1 Scanning electron microscope (SEM) image of chemical vapor deposition (CVD)-grown MoS_2. **a** Triangular shape MoS_2 located near periphery, **b** whole area-covering MoS_2 monolayer near central region. Each scale bar in **a** is 20 μm and in **b** is 200 μm. **c** Grain boundary is indicated by dashed line. Scale bar is 20 μm. **d** Raman spectra of 1L, 2L, and 3L CVD MoS_2, and bulk. **e** Raman peak full width at half maximum (FWHM) of 1L MoS_2 grown on differently thick SiO_2. **f** PL spectra of 1L CVD MoS_2 under varied laser power (inset). **g** Photoluminescence (PL) spectra FWHM plot obtained from varied SiO_2 thickness

outline in Fig. 1c. The average individual grain size is 2000 μm^2. At the periphery of the substrate, characteristic triangular-shaped monolayer MoS_2 with side dimensions from 30 to 60 μm were observed (Fig. 1a). In Fig. 1a we can also see how the monolayers start to join to ultimately form the continuous film. These results were obtained from all the thermally oxidized SiO_2/Si substrates we used. Continuous film area approaches to a few mm^2. Micro-Raman spectroscopy was used to confirm the monolayer nature of the MoS_2 grown as the separation between the E^1_{2g} and A_{1g} Raman peaks is known to be characteristic of the number of MoS_2 layers.[34–36] The spectra obtained over the film regions (Fig. 1b) are shown in the red “1L” curve of Fig. 1d, with a peak separation of 20.2 cm^{-1}. For further confirmation, we have put the spectra for bilayer (2L, blue, 23.2 cm^{-1} peak separation) and trilayer (3L, green, 24.2 cm^{-1} peak separation) MoS_2 spots that we could sometimes find at the very outer periphery of the substrates, where MoS_2 nucleation might not be so controllable resulting in more vertical growth (supporting photo image of the outer periphery is seen in Figure S2). We also included the Raman spectrum from bulk MoS_2 powder (black line), which exhibited a 25.1 cm^{-1} peak separation. To assess the quality of the MoS_2 monolayer films,[37–39] we plot in Fig. 1e the full width at half maximum (FWHM) of the E^1_{2g} and A_{1g} Raman peaks for the material grown on the various thicknesses of SiO_2. The FWHM was essentially independent of the oxide thickness, staying in the range of 2–2.5 and 3.5 cm^{-1} for the E^1_{2g} and A_{1g}, respectively. For comparison, FWHM values reported to date for the E^1_{2g} and A_{1g} peaks of CVD-grown monolayer have been in the ranges of 3.5–4.2 and of 5–7 cm^{-1} respectively.[35,40,41] Furthermore, MoS_2 monolayers exfoliated from geological materials exhibit a FWHM of 3.7 cm^{-1} for E^1_{2g} peak in report.[42] Therefore, the FWHM data we obtained may indicate that our CVD-grown monolayer MoS_2 is

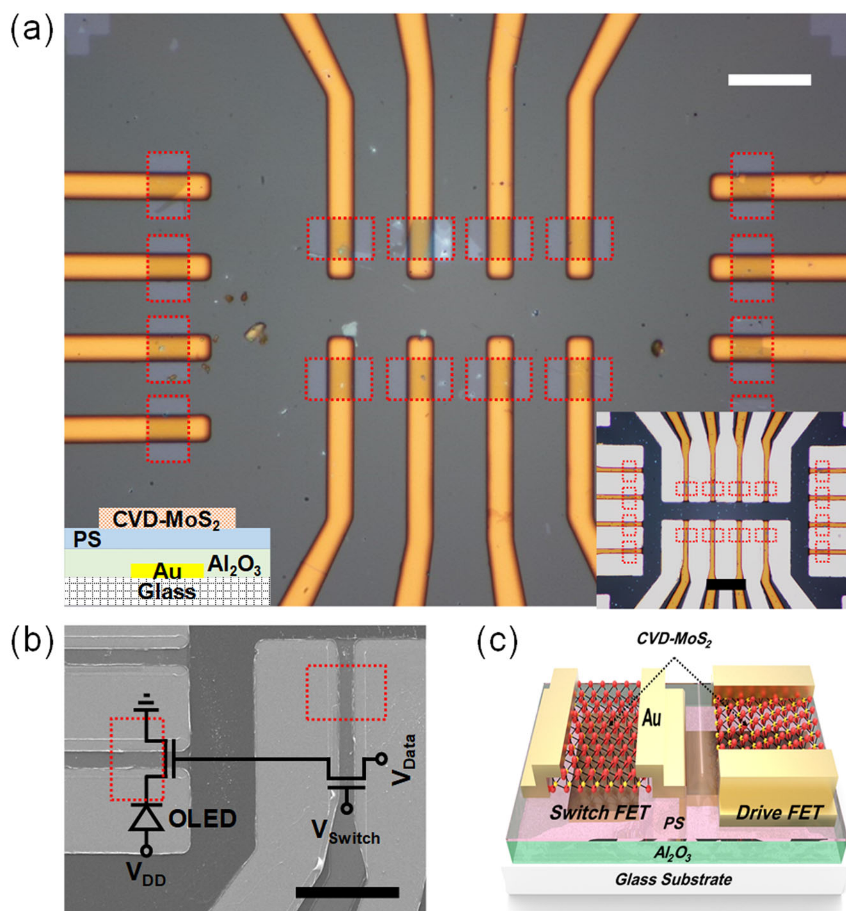

Fig. 2 **a** Optical microscope (OM) images of patterned chemical vapor deposition (CVD)-MoS_2 channels (red dotted rectangles) on patterned bottom gate (left inset for cross section) and OM images of field- effect transistors (FETs; right inset with patterned Au S/D electrode). **b** Scanning electron microscope (SEM) image of switching and driver FETs for an organic light-emitting diode (OLED) pixel. Circuit for an OLED pixel is overlaid on SEM image. **c** Schematic three-dimensional (3D) view of those FETs for the OLED pixel circuit. Hydrophobic polystyrene (PS) layer on oxide dielectric is worth to note in our FETs (schematic 3D and cross-sectional two-dimensional). All scale bars are 20 µm

comparable to or potentially better in crystalline quality than reported ones.[43] We might attribute such good crystalline quality along with large-scale continuous monolayer MoS_2 to a high growth temperature over ~800 °C with a temperature of 900 °C for the powder precursor, since the higher temperature enhances surface diffusion of adatoms and lateral crystal growth, and therefore smooth coalescence into a continuous film. The optical properties of our MoS_2 monolayer films were also characterized using power-dependent photoluminescence (PL) measurements at room temperature, as shown in Fig. 1f. A strong emission related to the A-exciton in MoS_2 was observed at 1.84 eV. The B-exciton-related peak could also be distinguished at 1.99 eV. The peak separation of 150 meV is due to the splitting of valence band.[2,42,44] The peak positions did not shift with exciton power. The inset of Fig. 1f shows that the luminescence emission intensity (I_{PL}) follows a power relationship with incident laser excitation power (I_L): $I_{PL} = nI_L^{\alpha}$.[45] The exponent α indicates the type of radiative recombination process the PL originates from, with an exponent of 1 corresponding to free exciton recombination. In our samples, a slope of 0.79 (as α) was obtained, which indicates the recombination is close to excitonic although there is some degree of defect-related recombination.[46,47] We have also compared the FWHM of the main luminescence peak for the MoS_2 films grown on the various thicknesses of SiO_2 as shown in Fig. 1g. The FWHM was found to range from 60 to 80 meV, which is close to the best reported value (60 meV) to date (50 meV is for the suspended MoS_2 monolayer[2]).[15]

The large-scale MoS_2 monolayer was transferred onto a 50 nm-thick Al_2O_3 dielectric, beneath which a patterned Au gate was located already. Our MoS_2 was then aligned and patterned on the gate as channels by conventional photolithography including O_2 plasma dry etching. Figure 2a displays such patterned MoS_2 channels (red dotted-line rectangles) and gates in optical microscope (OM) images along with a schematic cross section (left inset) while completed devices (16 FETs) with Au S/D electrodes are also shown in the right inset as another OM image. As stated in the introduction part, we particularly spin-coated an ultrathin hydrophobic PS layer on Al_2O_3 dielectric before the transfer of CVD MoS_2 monolayer, expecting and targeting a relatively uniform V_{th} distribution of MoS_2 FETs. But we also fabricated another set of MoS_2 FETs with bare Al_2O_3 without PS layer, so to compare the two types of FET devices with and without PS layer. Capacitance-voltage (*C-V*) measurements were thus conducted for two different dielectrics (see Figure S3 for the values of 8.46 nm PS/50 nm Al_2O_3 and 50 nm Al_2O_3). In addition, another PS layer was utilized as a technical sacrificial cover to transfer monolayer MoS_2 during these device fabrications, and this second PS layer is peeled-off from MoS_2 after transferring onto dielectric, while the ultrathin PS layer on Al_2O_3 stays firm because it covalently bonded on Al_2O_3 surface (see fabrication details in Methods section and Supporting Information, Figure S4.) According to the OM images of channels in Fig. 2a, most of the monolayer channels appear clean without any distinguishable specks except a few channels, which might contain nonuniform

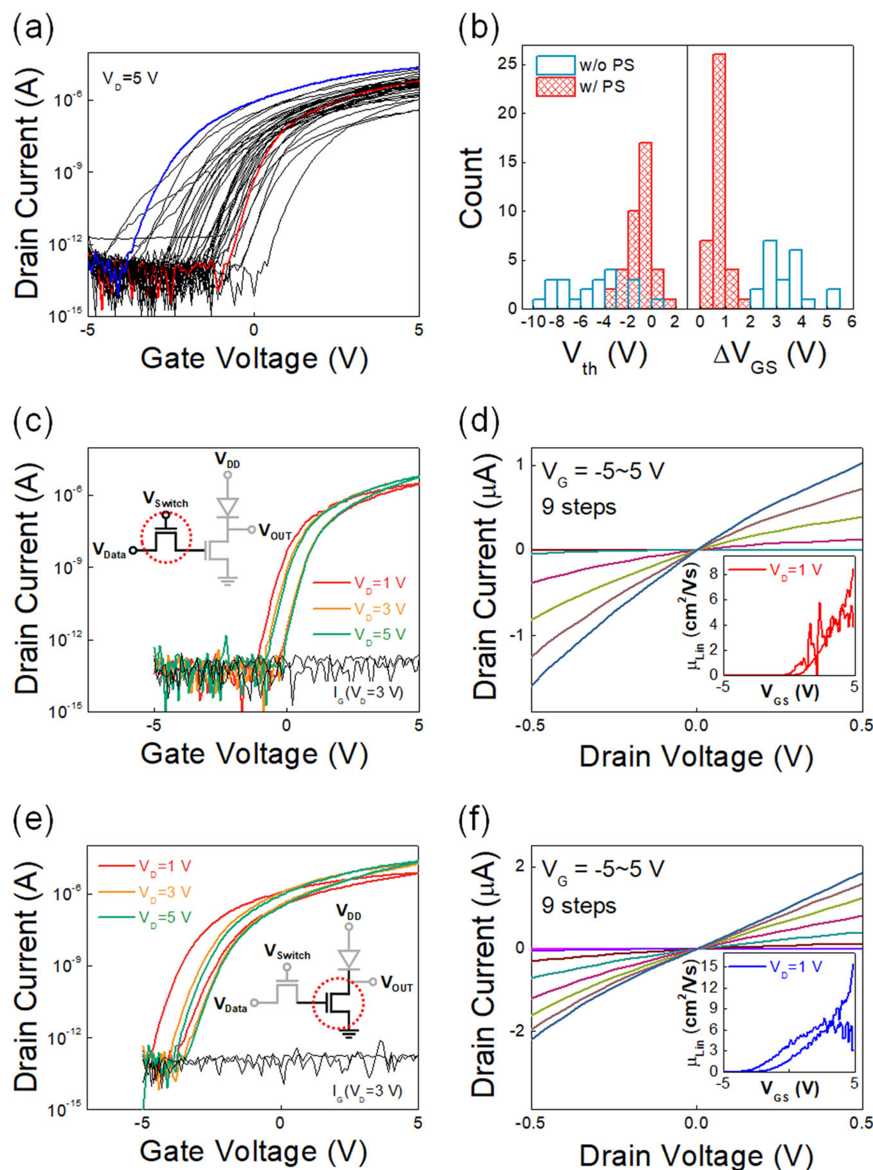

Fig. 3 **a** Transfer curves of total 38 chemical vapor deposition (CVD) MoS_2 field- effect transistors (FETs) with polystyrene (PS) layer obtained at $V_D = 5$ V (without including hysteresis). Blue and red curve FETs were selected for driver and switching devices in the pixel operation. **b** Histograms of the V_{th} and ΔV_{GS} from 38 FETs (w/ PS) and 22 FETs (w/o PS). **c** Transfer curves of switching driver FETs obtained at $V_D = 1$, 3, and 5 V (including hysteresis). Switching FET is indicated in the inset organic light-emitting diode pixel circuit by red dotted circle. **d** Output curve of switching FET and inset linear mobility plot. **e** Transfer curves of driver FET obtained at $V_D = 1$, 3, and 5 V (including hysteresis). Driver FET is indicated in the inset circuit by red dotted circle. **f** Output curve of driver FET and inset linear mobility plot

thickness (bilayer or trilayer) regions. Figure 2b is an SEM image from two MoS_2 FETs with S/D electrodes as example devices for switch and driver of an OLED pixel circuit (as described in the overlaid inset circuit). The red rectangles in Fig. 2b identify the channel area as partially covered by S/D region while Fig. 2c illustrates the same circuit as a three-dimensional drawing.

As we fabricated 48 MoS_2 FETs with PS layer (type 1, FET with PS/Al_2O_3 bilayer for gate dielectric) and 32 FETs without PS layer (type 2, FET with Al_2O_3 only), 38 FETs operated among total 48 while 22 FETs appeared alive among total 32 devices (~80% vs. ~70% in yield for type 1 vs. type 2). Figure 3a shows drain current-gate voltage (I_D-V_{GS}) transfer characteristics of such 38 FETs with PS layer (type 1), and the transfer curves from 22 FETs without PS (type 2) were put to Supporting Information, Figure S5a and b. We compare device uniformity between FETs with PS layer and without in Fig. 3b, where the histograms of V_{th} and gate hysteresis (ΔV_{GS}) are plotted as obtained from those two types of FETs. The V_{th} distribution of FETs with PS layer appears quite uniformly centered (near −1 V) while that of FETs without is relatively scattered, and the ΔV_{GS} of the former devices appears mostly smaller (as ~1 V in average) than that of the latter (approximately more than 3 V). Failed or low-performance FETs seem to originate from the transfer failure of MoS_2 monolayer, which includes tearing and possible wrinkling during transfer whether on PS/Al_2O_3 or bare Al_2O_3 surface. It is, however, regarded that the hydrophobic PS layer surface certainly improves the device uniformity and causes hysteresis reduction due to trap density reduction at the MoS_2 channel/dielectric interface. Among the 48 FETs of Fig. 3a, we selected two FETs for switch and driver, which have red and blue curves, respectively for active OLED pixel operation. Figure 3c shows transfer characteristics of switching MoS_2 FET (inset circuit), where ΔV_{GS} (~1 V) and V_{th} (~−1 V) of the device are displayed along with ON I_D current of a few μA and high ON/OFF I_D ratio of ~10^8 at a drain voltage (V_{DS}) of 1, 3, and 5 V. Gate leakage was <~100 fA only. Output (I_D-V_{DS})

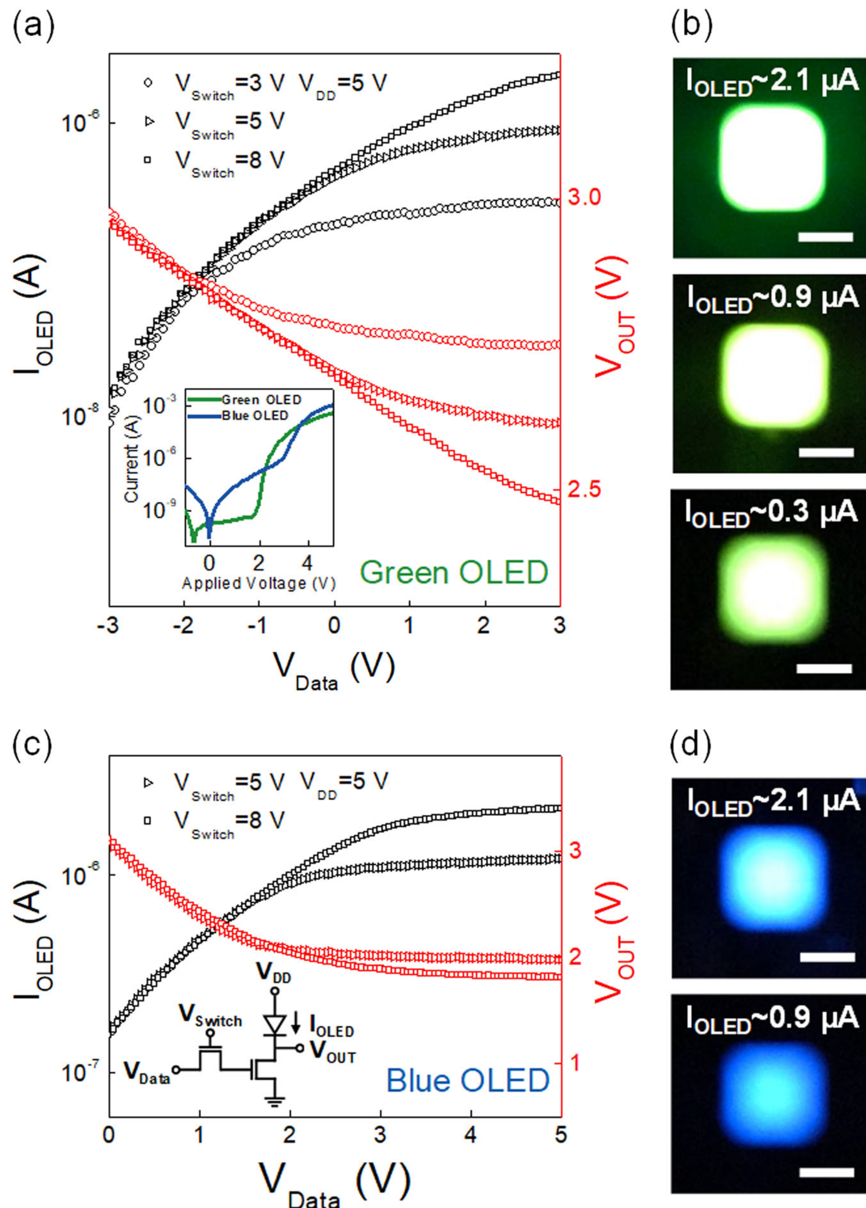

Fig. 4 **a** Organic light-emitting diode (OLED) current (left *y*-axis) and output voltage (right *y*-axis) plots obtained from the pixel circuit by V_{Data} sweep for green OLED (under $V_{Switch} = 3$, 5, and 8 V). Inset *I-V* curves were obtained from green and blue OLED diodes. **b** Each V_{Switch} condition causes different emission intensity and I_{OLED}. **c** I_{OLED} and V_{OUT} plots obtained from the pixel circuit by V_{Data} sweep for blue OLED ($V_{Switch} = 5$ and 8 V). Inset pixel circuit is seen for analog OLED pixel operation. **d** Each V_{Switch} condition causes different blue emission intensity and I_{OLED}. All scale bars are 50 μm

characteristics of the switching device are shown in Fig. 3d where ohmic behavior between Au and S/D is confirmed. Inset linear mobility plot of Fig. 3d shows that the average mobility of switching FET is as high as ~8 cm^2 V^{-1} s^{-1}. On the one hand, from the type 1 FET group in Fig. 3a we chose another device (blue transfer curve) for driving FET whose V_{th} is a little deviated to more (−) direction from central region. Our selection was according to a natural expectation that this FET would draw more current for OLED operation, although such V_{th} deviation may be undesirable in producing uniform devices. This deviation may come from bilayer- or trilayer-containing MoS_2 channel. Figure 3e displays the transfer characteristics of driving MoS_2 FET (inset circuit), where ΔV_{GS} (~1 V) and V_{th} (~−4 V) of the device are shown along with high I_D current of more than 5 μA at 5 V of V_{DS} and high ON/OFF I_D ratio of ~10^8 at 1, 3, and 5 V of V_{DS}. Output characteristics of the driver FET are quite similar to those of switching device as shown in Fig. 3f. Inset mobility plot of Fig. 3f shows the linear mobility of driving FET as ~15 cm^2 V^{-1} s^{-1}. In fact, maximum mobility of ~15 cm^2 V^{-1} s^{-1} and average of 8–10 cm^2 V^{-1} s^{-1} were achieved from our type 1 FETs. Those decently high mobility values might come from large MoS_2 grain size (~60 μm), which is relatively larger than channel length ($L = 4.5$ μm) and width ($W = 10$ μm).

Based on the device performances of the switching and driving FETs, an analog pixel operation for a single OLED was attempted with a circuit (the inset of Fig. 4c) under voltage conditions: a fixed supplied voltage (V_{DD}), varied switching voltages (V_{Switch}), and varied data voltages (V_{Data}). Figure 4a shows OLED current (I_{OLED}) and output voltage (V_{OUT}) with respect to V_{Data} sweep, which was taken to turn on a green OLED (inset displays *I-V* curve characteristics of green and blue OLED). It is no doubt that high V_{Switch} (=8 V) and V_{Data} (=3 V) cause (or drive) high I_{OLED} with most

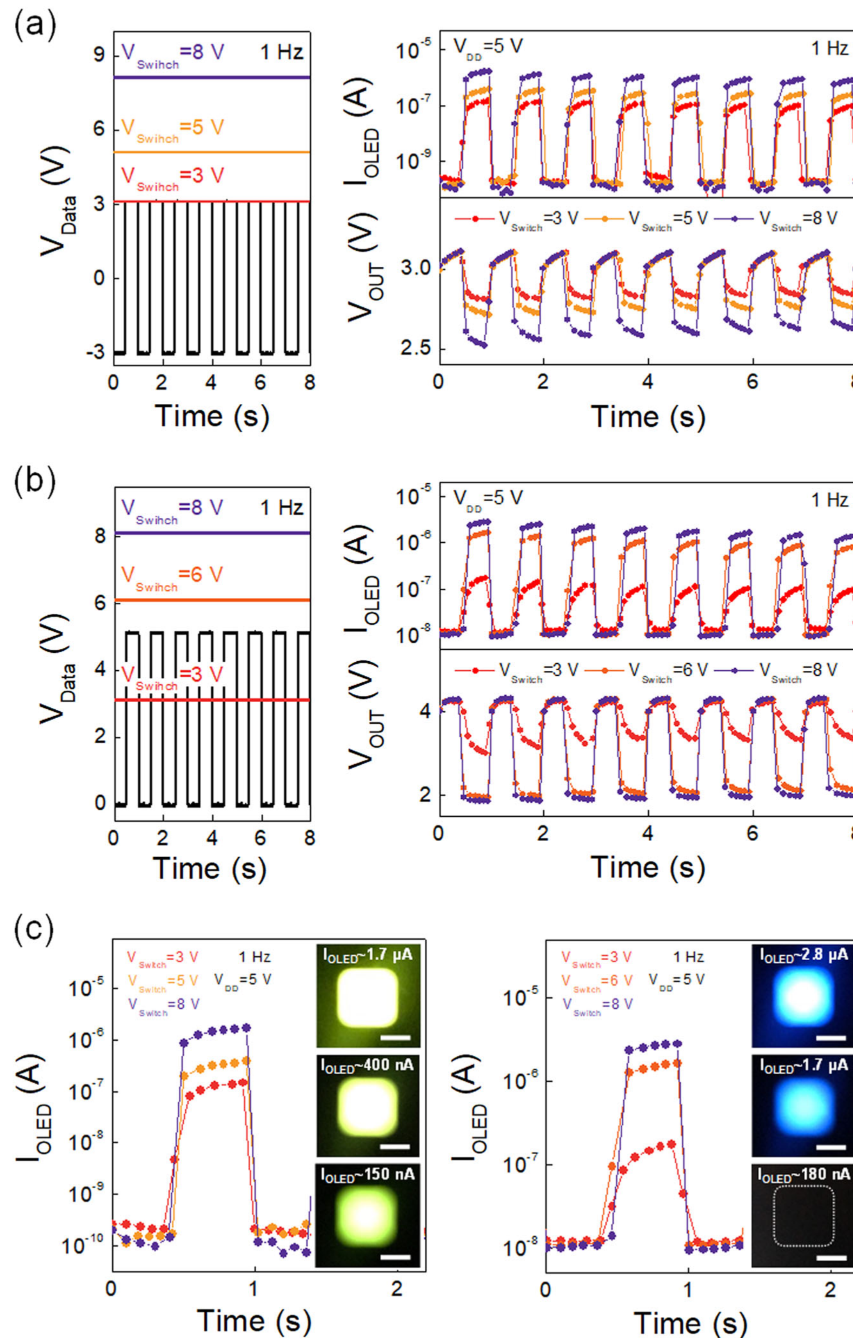

Fig. 5 Time domain plots of organic light-emitting diode (OLED) current and output voltage. **a** For ON (light) and OFF (dark) switching in the pixel circuit of green OLED, V_{Data} was modulated between −3 and 3 V at 1 Hz under three different V_{Switch} = conditions 3, 5, and 8 V. **b** For ON and OFF switching in the blue OLED pixel circuit, V_{Data} was modulated between 0 and 5 V at 1 Hz under three different V_{Switch} = conditions 3, 6, and 8 V. **c** Dynamic emission properties of green vs. blue OLED pixels. Even under smaller I_{OLED} current, green light appears brighter than blue emission. Under V_{Switch} = 3 V, blue OLED cannot be turned on. All scale bars are 50 μm

intense brightness among three different pixel displays of Fig. 4b. Medium and low I_{OLED} are also displayed with V_{Switch} of 5 and 3 V showing their respective brightness in Fig. 4b. The value of V_{DD}-V_{OUT} matches with the applied voltage to the OLED pixel itself. Similar behavior of analog pixel operation was observed from a single blue OLED with two different switching voltages of 5 and 8 V as shown in Fig. 4c, d. However, it is recognized from blue OLED pixel operation that we might need higher V_{Switch} to brighten up the blue light than that for the case of green OLED. According to Fig. 4d, I_{OLED} values of blue OLED are higher than those of green OLED for V_{Switch} (=8 and 5 V) while blue lights appear much dimmer than green lights.

Dynamic ON/OFF switching of OLED pixels was attempted as shown in Fig. 5a, b, which are according to their static light-emitting performances in Fig. 4a–d. Figure 5a shows the I_{OLED} and V_{OUT} dynamics in green OLED pixel circuit as obtained by temporally modulating V_{Data} (between −3 and 3 V at 1 Hz). ON and OFF switching was observed from all the switching voltages (=3, 5, and 8 V), and of course, the green emission intensity appears distinguishable according to each switching voltage. For blue OLED pixel operation of Fig. 5b, almost the same dynamics

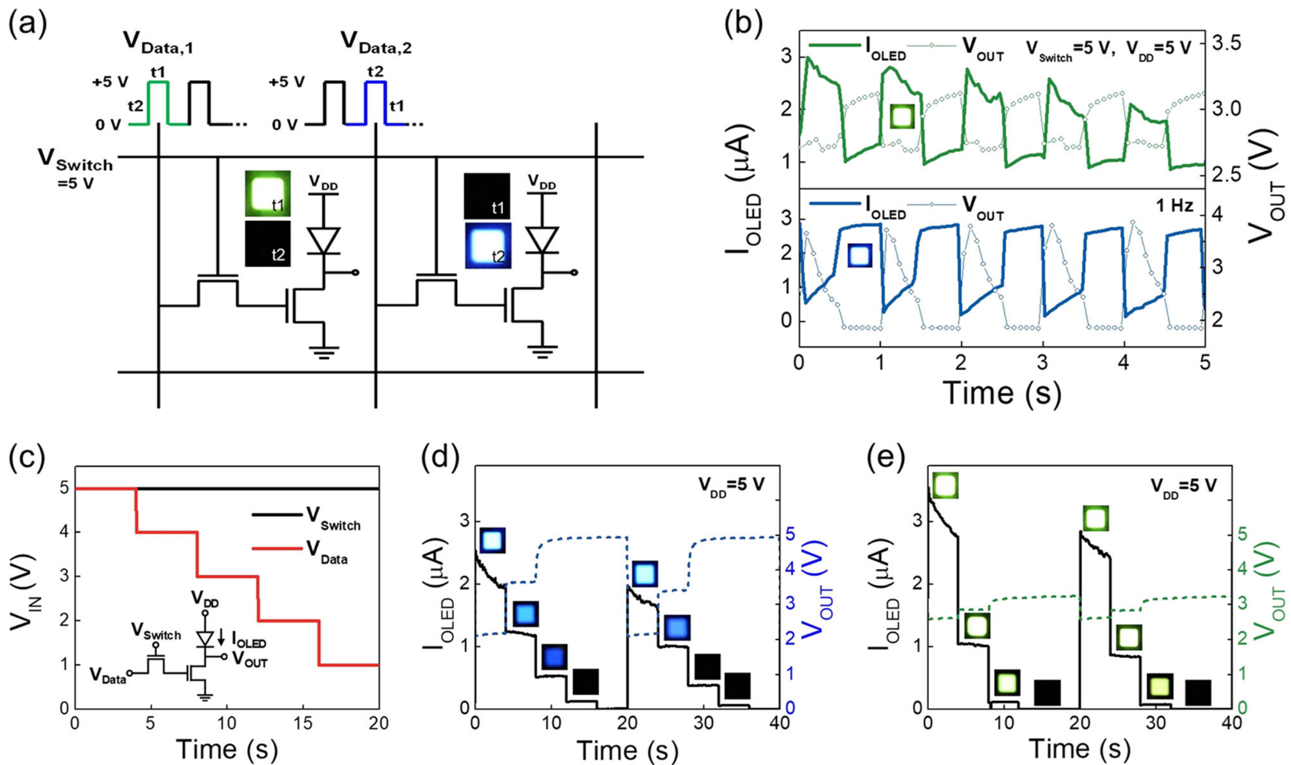

Fig. 6 **a** Circuitry for digital alternate switching of 2 × 1 two-color organic light-emitting diode (OLED) pixel array, and **b** I_{OLED}/V_{OUT} dynamics for each color OLED under constant $V_{DD} = V_{Switch} = 5$ V, periodic $V_{Data,1} = 5$ and 0 V ($V_{Data,2} = 0$ and 5 V, synchronously). **c** Time-V_{IN} design plot for grayscale analog pixel switching. **d**, **e** Time domain I_{OLED} and V_{OUT} results for grayscale analog OLED pixel (blue and green)

was expected and observed from the circuit, however, in fact a low V_{Switch} of 3 V could not turn on the blue light at its I_{OLED} (=~0.18 μA) while 6 and 8 V turn on the OLED without problem. Based on the I_{OLED} results of Fig. 5a, b, dynamic OLED emissions for green and blue lights are displayed in Fig. 5c for more detailed comparison between the two OLEDs. According to Fig. 5c, the blue light appears completely dark at I_{OLED} (=~0.18 μA) and 3 V switching voltage while the green emission is still very bright at the same voltage and even lower I_{OLED} (=~0.15 μA). Such emission difference in both dynamic and static operations comes from their respective emission efficiencies since green OLED emission displays a higher efficiency than blue ones in general. On the one hand, an obvious delay in V_{OUT} dynamics (Fig. 5b) for blue emission was observed under 3 V of V_{Switch}. It is probably because *I*-*V* curve characteristics of blue OLED is different from that of green OLED. According to the inset plots of Fig. 4a, blue OLED should have higher resistance (d*V*/d*I*) in the range of 1–3 V than green OLED device. Such higher resistance (*R*) might cause longer RC delay under the same parasitic capacitance (*C*) condition. Nevertheless, it is regarded that our CVD MoS_2 monolayer channel FETs overall show strong potentials to function as the gate switch and I_{OLED} driver for analog OLED pixel circuits.

Based on above switching dynamics results from Fig. 5a–c, we further conducted two types of more advanced dynamic switching: digital switching of 2 × 1 OLED pixel array and grayscale analog switching of single blue/green OLED pixel. These demonstrations were carried out under fixed V_{DD} and V_{Switch} ($V_{DD} = V_{Switch} = 5$ V), which appears to be a proper condition for pixel display in Fig. 5c when two alternating V_{Data} pulses are used between 0 and +5 V. Figure 6a shows 2 × 1 OLED pixel array operation employing four CVD MoS_2 FETs, where green OLED is ON with $V_{Data,1}$ of +5 V when blue one is OFF with $V_{Data,2}$ of 0 V at a certain time t_1, and vice versa at time t_2. Such alternating digital operations are displayed with I_{OLED} and V_{OUT} from each OLED pixel circuit (green and blue) as shown in Fig. 6b. Grayscale analog pixel operation was designed as plotted in time-V_{IN} (=V_{Data}), and in this case V_{IN} decreases with 1 volt step in 4 s. According to resultant time-I_{OLED} plots in Fig. 6d, e, grayscale pixel display appears quite clear in each step of I_{OLED}. For each color, four different intensities of OLED are obtained while green color is much brighter than blue one as expected. Another interesting to note is that V_{OUT} difference in analog green OLED driving is much minimal compared to that in analog blue driving. In other words, small V_{OUT} difference causes large difference in I_{OLED} for green OLED. Such difference between green and blue pixel would be again attributed to the *I*-*V* curve origins of green and blue OLED diode in the inset of Fig. 4a. Supporting Information, a video file (two MoS_2 OLED.avi) is also prepared to demonstrate the digital switching of 2 × 1 pixel array and grayscale analog switching of single blue/green OLED pixel.

In summary, we have fabricated CVD-grown a few mm large-scale MoS_2 FETs and investigated their low voltage OLED pixel circuit applications. In particular, when CVD MoS_2 monolayer was transferred onto gate-patterned Al_2O_3 dielectric on glass, an ultrathin hydrophobic PS layer was used as a moderating medium between MoS_2 and Al_2O_3, to improve the uniformity of V_{th} and reduce the gate hysteresis in FETs. Our MoS_2 FET shows its average linear mobility of 8–10 $cm^2 V^{-1} s^{-1}$ and a high ON/OFF I_D ratio of 10^8 as patterned by photolithography on glass, and those values are regarded quite high or comparable to previous reports for CVD MoS_2 FETs[28–32] because a single grain of our CVD MoS_2 monolayer appears as large as ~60 μm in side dimension. Among 48 MoS_2-based FETs, 38 devices successfully work (yield ~80%) operating at ~5 V. Dynamic switching of blue and green OLED pixels was nicely demonstrated using the CVD monolayer MoS_2 FETs in two ways: 2 × 1 digital pixel array switching and grayscale analog switching of single blue/green OLED pixel. We conclude

that our CVD MoS_2 FETs are very promising as backpanel devices for future active matrix OLED pixel display.

METHODS

MoS_2 CVD growth

The 2D MoS_2 material was grown by CVD in a quartz tube furnace. A single precursor source was used, consisting of MoS_2 powder.[33] instead of the combination of MoO_3 and S, which is more often reportedly used. The precursor was placed in a quartz boat at the center of a tube while the substrates were placed downstream. We did not use any substrate surface treatment to promote nucleation prior to growth. The growth was performed at a pressure of 10 mbar under 20 sccm Ar flow, with the furnace temperature ramped to 950 °C, for a duration of 20 min. This high temperature leads to the thermal evaporation of the MoS_2 precursor, which nucleates and redeposits onto the substrates located at a cooler region of the furnace (estimated to be ~200 °C lower). The substrate temperature (~800 °C with a temperature of 900 °C for the powder precursor) is therefore also higher than those reported when a combination of MoO_3 and S was used. We believe this higher growth temperature leads to enhanced surface diffusion during growth and therefore, in combination with the use of a single precursor, contributes to the larger area MoS_2 monolayer film obtained here. Finally, the furnace was allowed to cool down naturally. Thermally oxidized silicon substrates were used in this work. The substrates were oxidized prior to growth under an O_2/Ar at 1000 °C at an atmospheric pressure for the durations of 60, 120, 180, and 240 min, resulting in an oxide thickness of approximately 45, 75, 90, and 145 nm, respectively, as confirmed by ellipsometry. In addition, we have used commercially available 300 nm SiO_2/Si wafer for comparison. To the best of our knowledge, this represents the first comparative study of MoS_2 growth on different oxide thickness, while the majority of reported data was on thick 300 nm oxide.

Transfer process

As-grown MoS_2 on the SiO_2/p^+-Si substrate was spin-coated by PS layer (molecular weight = 280,000, Sigma-Aldrich) at 3500 rpm for 60 s. The sample was annealed at 85 °C for 15 min. After baking, the resultant PS/$MoS_2/SiO_2/p^+$-Si structure was dipped into deionized (DI) water, so that the PS/MoS_2 membrane might be separated from the SiO_2/p^+-Si substrate and floated on the surface of DI water. The PS/MoS_2 membrane was picked up and transferred onto the target (ultrathin PS/gate-patterned atomic layer deposition (ALD) Al_2O_3/glass or gate-patterned ALD Al_2O_3/glass) substrate. After the transfer to the target substrate, the sample was baked at 85 °C for 1 h and 180 °C for 30 min. The top PS residues were peeled-off by using toluene.[48] (Supporting Information, Figure S4)

Device fabrication

The glass substrates were cleaned in acetone and ethanol using an ultrasonicator for 15 min. The Au/Ti (20 nm/10 nm) bilayer was deposited by DC magnetron sputtering system and patterned for bottom gate-electrodes by photolithography and lift-off process (lift-off layer: LOR 3A, Micro Chemical, and photoresist layer: AZ GXR-601, AZ electronic materials). For dielectric layers, ultrathin PS/50 nm-thick Al_2O_3 (or 50 nm-thick Al_2O_3 only) layer was prepared by ALD system and PS coating. For hydrophobic PS layer spin-coating, dimethyl chlorosilane-terminated PS (Polymer Source, Product No. P3881-SSiCl) was initially dissolved in toluene (Aldrich) solvent, and the oxygen plasma cleaning (150 W, 50 sccm, 20 s) was applied to the prepared Al_2O_3 dielectric surface. The PS-brush solution (10 mg/mL) was spin-coated onto the Al_2O_3 surface and then heated at 170 °C for 48 h inside a vacuum oven, so that the ultrathin PS layer may be covalently bonded to the plasma-treated Al_2O_3 surface.[49,50] As stated in the above transfer process, as-grown monolayer was transferred from SiO_2/p^+-Si substrate to patterned bottom gate substrate using PS transfer method (Supporting Information, Figure S4).[48] After transfer, CVD MoS_2 flakes were patterned by photolithography and O_2 plasma dry etching process. For the source (S) and drain (D) ohmic contact electrodes, Au (50 nm) was deposited and patterned using conventional photolithography and lift-off processes. Finally, we annealed the device at 250 °C in N_2 ambient to improve the S/D contact for MoS_2 channel.

Measurements

The device current-voltage (*I-V*) characterizations were carried out by a semiconductor parameter analyzer (HP 4155C, Agilent Technologies) and the capacitance-voltage (*C-V*) measurements were carried out by a LCR meter (HP4284A, Agilent Technologies). Electrical dynamics were investigated with a function generator (AFG 310, Sony/Tektronix). SEM images were taken with an Field Emission SEM (JSM-7800F, JEOL Ltd.). OLED sample pixels were supplied from Samsung Display Co.

DATA AVAILABILITY

The datasets generated during and/or analyzed during the current study are available from the corresponding author on reasonable request.

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AUTHOR CONTRIBUTIONS

H.K. performed the fabrication and measurements of the MoS_2 transistors and demonstration of the AMOLED pixel, S.G. and P.K. performed the synthesis and characterization of the MoS_2 films, S.M.K. performed Raman and PL measurement, J. H.P. and Y.J. helped with PS layer, S.Y. helped with 3D figure scheme techniques, and S.I. designed whole device experiments. All authors discussed the results.

ADDITIONAL INFORMATION

Supplementary Information accompanies the paper on the *npj 2D Materials and Applications* website (https://doi.org/10.1038/s41699-019-0091-9).

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