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Embedded gate CVD MoS_2 microwave FETs

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Recent studies have increased the cut off frequencies achievable by exfoliated MoS_2 by employing a combination of channel length scaling and geometry modification. However, for industrial scale applications, the mechanical cleavage process is not scalable but, thus far, the same device improvements have not been realized on chemical vapor deposited MoS_2. Here we use a gate-first process flow with an embedded gate geometry to fabricate short channel chemical vapor deposited MoS_2 radio frequency transistors with a notable f_T of 20 GHz and f_{max} of 11.4 GHz, and the largest high-field saturation velocity, $v_{sat} = 1.88 \times 10^6$ cm/s, in MoS_2 reported so far. The gate-first approach, facilitated by cm-scale chemical vapor deposited MoS_2, offers enhancement mode operation, I_{ON}/I_{OFF} ratio of 10^8, and a transconductance (g_m) of 70 μS/μm. The intrinsic f_T (f_{max}) obtained here is 3X (2X) greater than previously reported top-gated chemical vapor deposited MoS_2 radio frequency field-effect transistors. With as-measured *S*-parameters, we demonstrate the design of a GHz MoS_2-based radio frequency amplifier. This amplifier has gain greater then 15 dB at 1.2 GHz, input return loss > 10 dB, bandwidth > 200 MHz, and DC power consumption of ~10 mW.

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INTRODUCTION

Molybdenum disulfide (MoS_2) is a two-dimensional (2D) semiconductor in the family of transition metal dichalcogenides. Its single layer direct bandgap of ~ 1.8 eV[1] allows for high I_{ON}/I_{OFF} metal-oxide semiconducting field-effect transistors (FETs).[2] More relevant for radio frequency (RF) applications, theoretical studies predict MoS_2 can afford saturation velocities, v_{sat}, greater than 3×10^6 cm/s.[3] While the RF applications of MoS_2 are still in their infancy, recent studies have pushed exfoliated MoS_2 cut off frequencies significantly higher.[4–6] The study by Krasnozhon et al. employed edge contacts to achieve an intrinsic f_T of 25 GHz in trilayer exfoliated MoS_2.[5] The work by Cheng et al. used transferred gate stacks on multilayer exfoliated MoS_2 to obtain an intrinsic f_T of 42 GHz.[6] However, for industrial scale applications, the mechanical cleavage process is not scalable and, thus far, there have been few studies on chemical vapor deposited (CVD) MoS_2 RF FETs.[7, 8] Our prior results demonstrated monolayer CVD MoS_2 top-gated FETs with an f_T of 6.2 GHz.[7] Furthermore, the work of Chang et al. used transferred monolayer CVD MoS_2 on a flexible substrate to achieve an f_T of 5.6 GHz.[8] As has been done with exfoliated MoS_2, optimized device configurations must be applied to CVD MoS_2 to push cut off frequencies higher. In this study, we take a step in this direction by taking an embedded gate approach to CVD MoS_2 FETs.

The embedded gate transistor has been well established in literature, particularly for the most prototypical 2D material, graphene.[9] Graphene RF FETs using embedded gate transistors have achieved sub-THz cut off frequencies.[10] However, the Dirac cone band structure of graphene results in a zero bandgap, which limits current saturation in graphene devices.[11] The embedded gate structure has been shown to significantly improve current saturation in graphene RF FETs, resulting in improved voltage and power gain.[12] Embedded gate FETs using CVD MoS_2 for digital circuits were recently studied, which found increased scalability, with higher yield and uniformity vs. their top-gated counterparts.[13] Additionally, embedded gate CVD MoS_2 FETs show enhancement mode operation, which is essential for complex multistage integrated circuits. The common theme allowing improved performance among all 2D materials using embedded gates is a resist-free channel-dielectric interface with a reduced number of fabrication process steps after the transfer of the active material.

Motivated by the advantages described above, in this work, we employ an embedded gate structure to advance the RF characteristics of CVD MoS_2. Our devices exhibit enhancement mode operation, I_{ON}/I_{OFF} ratio of 10^8, and the highest CVD MoS_2 g_m of 70 μS/μm. Using the measured *S*-parameters, we demonstrate a MoS_2-based cascode amplifier showing gain greater than 15 dB at 1.2 GHz.

RESULTS AND DISCUSSION

Figure 1a shows the Raman spectra of the as-grown and transferred MoS_2. The slight shift in the in-plane vibrational mode, E_{2g}, corresponds to a release of strain that exists in as-grown samples due to the mismatch of thermal coefficients between MoS_2 and the SiO_2 substrate.[14] The result of the same effect is also observed in the blue shift in the peak position of the photoluminescence spectra (Fig. 1a inset). Figure 1b shows an optical image of a fabricated CVD MoS_2 device array. Figure 1b inset (*bottom-right*) shows the zoomed-in image of the gate fingers while Fig. 1b inset (*top-left*) is a schematic of the cross-sectional view of the embedded gate device structure.

Figure 2a shows the I_{ds}–V_{gs} transfer characteristics of an embedded gate MoS_2 FET with a physical gate length, L_g = 150 nm. The embedded gate structure preserves a clean

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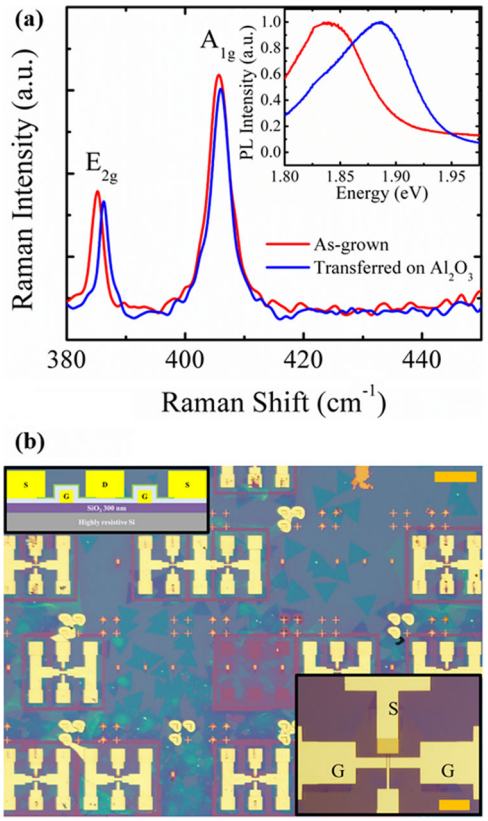

Fig. 1 Material characterization and optical image **a** Raman and photoluminescence (inset) spectra before and after transfer confirming the preserved CVD MoS_2 quality. The slight shift in the in-plane vibrational mode, E_{2g}, and the blue shift in the photoluminescence peak correspond to a release of thermal mismatch induced strain. **b** Optical image of a CVD MoS_2 device array with close-up gate finger layout (*bottom-right* inset) and a cross-sectional schematic of an embedded gate MoS_2 FET (*top-left* inset). The scale bar for the array (*top-right*) is 150 µm and the scale bar for the inset (*bottom-right*) is 10 µm

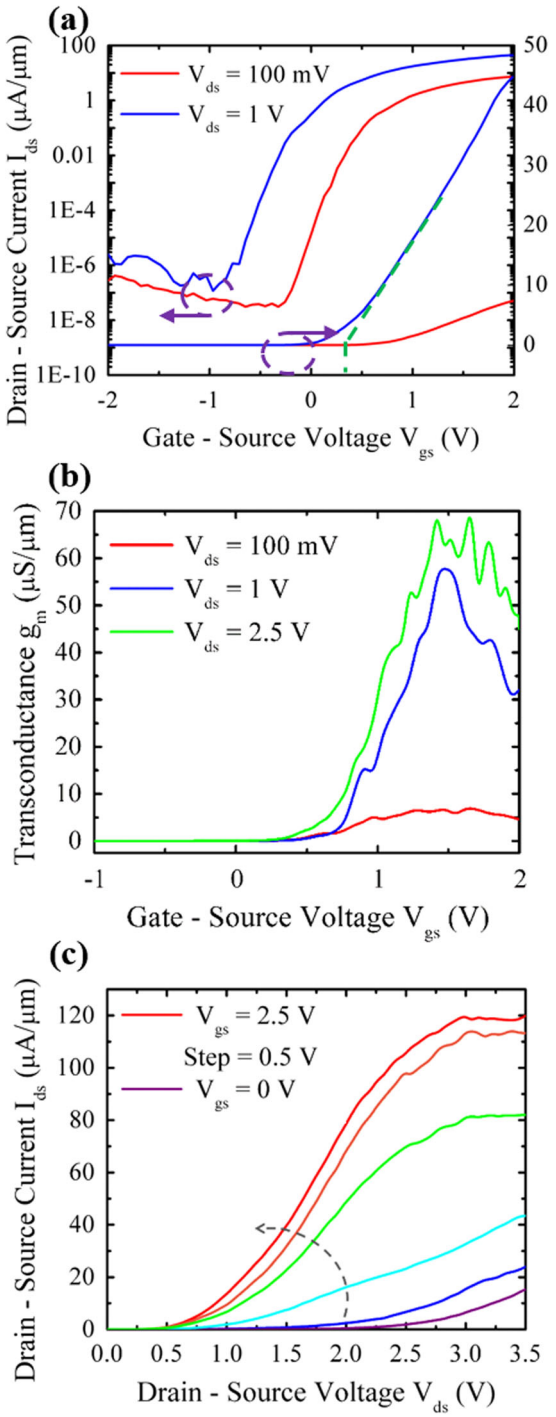

Fig. 2 DC characteristics **a** Transfer curves, I_{ds}–V_{gs}, for a 150 nm gate length CVD MoS_2 device. The device shows enhancement mode operation with an I_{ON}/I_{OFF} ratio of 10^8 at 100 mV of drain bias. **b** Transconductance curves, g_m–V_{gs}, for the same device. The device has a peak g_m of 70 µS/µm at a V_{ds} of 2.5 V. **c** Output curves, I_{ds}–V_{ds}, for the same device. The device has a current density of 120 µA/µm at a V_{ds} of 3.5 V. The device shows current saturation beyond a V_{ds} of 3 V

MoS_2-dielectric interface with less fixed-charge and organic impurities.[13] As a result, the threshold voltage, V_{th}, is positive and close to 0 V, in contrast to many top-gated structures, which suffer from uncompensated charge at the surface.[7] As shown in Fig. 2b, we measure a transconductance, g_m, of 70 µS/µm at a V_{ds} = 2.5 V. This is among the highest reported g_m for MoS_2 FETs on exfoliated or CVD grown films, at equivalent electric fields.[5, 7] The maximum field-effect mobility, μ_{FE}, is 21.2 cm^2/Vs, and after contact resistance correction is 81.6 cm^2/Vs.[15] In addition to the improved MoS_2-dielectric interface, the embedded gate structure provides improved gate control over the channel. After transfer, the MoS_2 wraps conformally to the rectangular gate fingers. The electrostatic control is improved over top-gated devices because the electric field flux reaching the MoS_2 channel is increased at an equivalent gate voltage. As an enhancement mode device, we can sufficiently deplete the channel to achieve an I_{ON}/I_{OFF} ratio of 10^8.

Figure 2c shows the I_{ds}–V_{ds} output characteristics for the same device. The device achieves current densities of 120 µA/µm at V_{ds} = 3.5 V. There is clear current saturation beyond V_{ds} of 3 V, resulting in a drain conductance, g_{ds}, within 5 µS/µm in the current saturation region (3 to 3.5 V of V_{ds}). The sub-linear curves at low V_{ds} indicate a significant Schottky barrier. We attribute this to undoped contacts and access regions. Our previous top-gated CVD MoS_2 RF FETs [7] employed sub-stoichiometric $HfO_{1.56}$ which extrinsically doped the MoS_2 contacts and access regions. This *n*-doping helped reduce the contact/access resistance due to thinning of the Schottky barrier width. The difference in surface charge transfer doping between oxygen-deficient HfO_{2-x} and stoichiometric Al_2O_{3+x} has been observed and well quantified in literature.[16–18] The elemental composition and chemical stoichiometry of atomic layer deposition (ALD) alumina were investigated

by x-ray photoelectron spectroscopy (XPS), as shown in Figure S6. The chemical composition of the Al_2O_x was quantified using the Casa XPS software, in which x was found to be about 3.1. The $Al_2O_{3.1}$ used in this study is oxygen-rich and closer to stoichiometric composition, providing minimal extrinsic doping. As a result, the extracted contact resistance for the devices in this study is $R_c = 3.5$ kΩ·µm, which is larger than that of our sub-stoichiometric $HfO_{1.56}$ devices.[7] However, using a higher bandgap dielectric, alumina, and a carefully deposited uniform gate finger surface allows for the scaling of the dielectric thickness down to 10 nm. We note that in our devices the top MoS_2 is exposed to ambient, allowing further dielectric/passivation layers or sensor measurements. The choice of top dielectric can provide the needed charge transfer to further improve the DC and RF characteristics.

Microwave performance was characterized from 0.1–15 GHz using an Agilent two-port vector network analyzer (VNA-E8361C). To accurately subtract the effects of the parasitic capacitances and resistances in the ground-signal-ground layout, we employed the standard de-embedding method using OPEN and SHORT measurements on the same device. Figure 3a shows the short circuit current gain $|h_{21}|$ vs. frequency. Operating at $V_{ds} = 3.5$ V with $L_g = 150$ nm, we achieve an extrinsic f_T of 3.3 GHz and, after de-embedding, an intrinsic f_T of 20 GHz. The intrinsic f_T is corroborated with the Gummel approach, as shown in Figure S3 of the Supplementary Information (SI). The lateral electric field used for the f_T measurement is in the high-field limit where carrier transport is determined by $v_{sat} = 2\pi \cdot f_{T,int} \cdot L_g$, and in our device is 1.88×10^6 cm/s. This is the highest extracted v_{sat} for room temperature MoS_2 RF FETs, either exfoliated or CVD (Table 1). Following Equation 1 of the SI, a higher f_T can be achieved by improving the g_m (by shortening the L_g), optimizing the layout to reduce parasitic capacitances, and reducing the contact resistance.

Another figure of merit for high-frequency transistors is the maximum frequency of oscillation, f_{max}. This is the frequency limit at which there is power gain, given matched input and output impedances, and can be expressed by Equation 2 of the SI. Figure 3b shows the maximum available power gain vs. frequency. Operating at the same DC bias, we measure an extrinsic f_{max} of 9.8 GHz and an intrinsic f_{max} of 11.4 GHz. This is the highest extrinsic f_{max} for MoS_2 reported so far, and the highest intrinsic value for CVD MoS_2. We attribute the high f_{max} to good current saturation, leading to a small g_{ds} and a large output resistance, r_o. Mason's unilateral gain, U_g, is shown in Figure S4 of the SI, which is 10.3 GHz. Figure 3c shows the scaling of f_T and f_{max} with gate length. In the high-field limit, the f_T generally scales inversely with length while f_{max} does not follow any trend due to varying individual device gate resistance and output conductance. In RF circuit design, it is important to know the intrinsic voltage gain A_v. The general expression for A_v is g_m/g_{ds}, but it can also be measured *vs.* frequency with impedance Z-parameters. Figure 3d shows the extrinsic and intrinsic unity voltage gain cut off frequency as 4.6

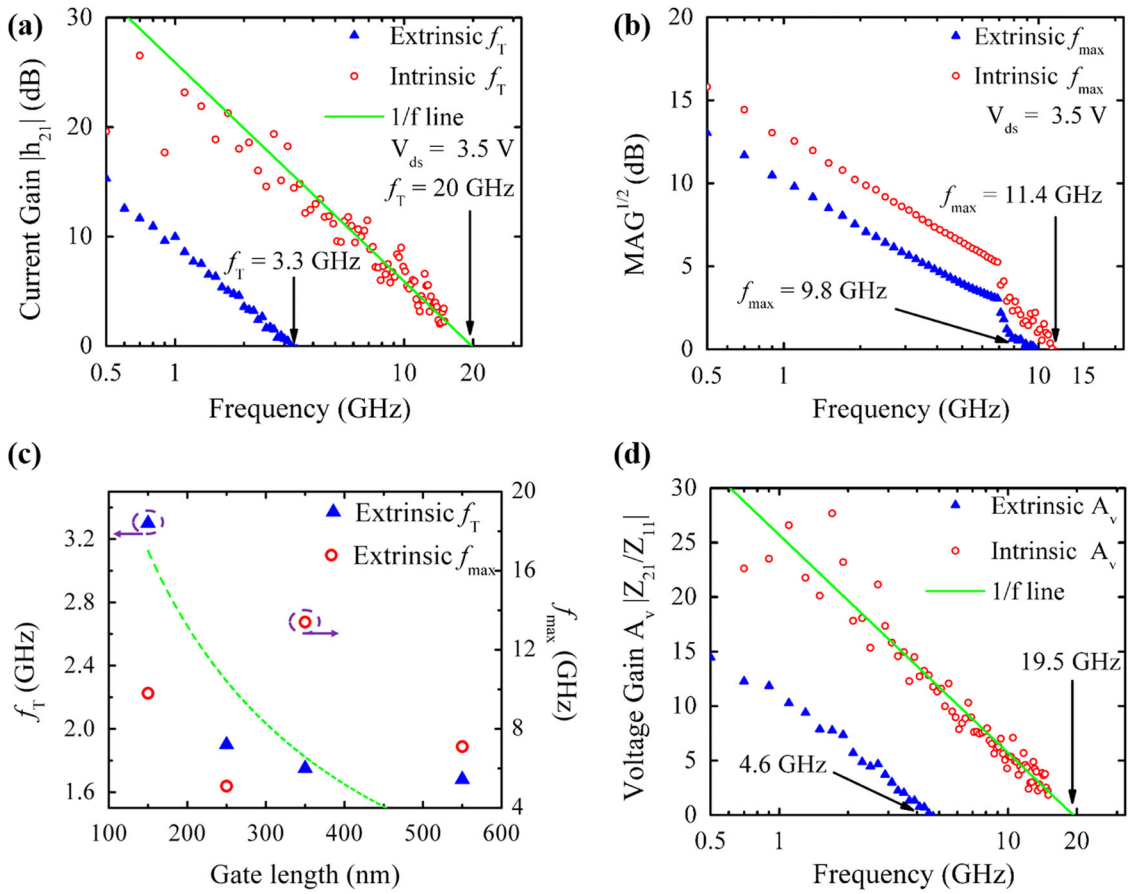

Fig. 3 RF characterization **a** Short circuit current gain, $|h_{21}|$, vs. frequency showing an extrinsic f_T of 3.3 GHz and an intrinsic f_T of 20 GHz. The device shows good linearity with the expected −20 dB/dec slope. **b** Maximum available power gain, $MAG^{1/2}$, *vs.* frequency showing an extrinsic f_{max} of 9.8 GHz and an intrinsic f_{max} of 11.4 GHz. We attribute the high f_{max} to current saturation-mediated low output conductance, g_{ds}. **c** Extrinsic f_T and f_{max} as a function of gate lengths from 150–550 nm. The dashed line is a fit of the f_T–L_g data to a 1/L line. **d** Voltage gain, A_v, expressed in Z-parameters as $A_v = Z_{21}/Z_{11}$ vs. frequency. The extrinsic A_v gain is unity at 4.6 GHz. After de-embedding the unity gain frequency is 19.5 GHz

Table 1. Comparison of RF MoS_2 FETs performance in literature. The saturation velocity (v_{sat}), calculated from the intrinsic f_T, is the highest reported to date for both exfoliated and CVD MoS_2 RF systems

MoS_2 RF Literature Comparison							
Device	Configuration (active/substrate/structure)	f_T ext/int (GHz)	f_{max} ext/ int (GHz)	A_v, cut off frequency ext/ int (GHz)	L_g(nm)	V_d(V)	v_{sat} ($\times 10^6$ cm/s)
This work	CVD 1L/Si/ embedded gate	3.3/20	9.8/11.4	4.6/19.5	150	3.5	1.88
[3]	Exf 3L/Si/ top gate	1.9/14	–/14	–/29	40	2.5	0.35
[3]	Exf 3L/Si/ top gate with "edge contacts"	6/25	–/16	–/45	70	2.5	1.1
[4]	Exf 2–7 nm/Si/ transferred gate	–/42	–/50	–/–	68	5	1.79
[5]	CVD 1L/Si/ top gate	2.8/6.7	3.6/5.3	3/11	300	3.5	1.26
[6]	CVD 1L/Flex/ top gate	2.7/5.6	2.1/3.3	–/–	500	2	1.76

and 19.5 GHz, respectively. The outstanding RF device performance achieved here can be attributed to (i) a resist-free MoS_2-dielectric interface, (ii) a reduced number of post-transfer fabrication process steps, compared with a top gate flow, and (iii) current saturation leading to a large r_o.

Variability is an important factor in obtaining high yield with device-to-device uniformity on a large-scale RF transistor integration. The sources of variability in the fabrication process presented here include intrinsic material non-uniformity, e-beam lithography, and local differences in the various device capacitances. Switching to a gas-based precursor system such as metalorganic chemical vapor deposition (MOCVD) can improve the material coverage and uniformity,[19] however, further work is needed to achieve the same device performance. A fully photolithographic process can help mitigate device-to-device feature size variations, which will also allow predictable device parasitics. To give some insight into the variability and scalability of our CVD MoS_2 RF devices, we have shown the data from a single wafer device array in Table S1 of the SI. We note that the non-functioning devices are not necessarily due to poor CVD MoS_2 sites, but were also caused by fabrication failures and electrical failures during biasing. An example of a fabrication failure is poor lift-off of the metal while an example of an electrical failure is gate breakdown during DC biasing.

Using the as-measured *S*-parameters, we designed a RF amplifier to demonstrate CVD MoS_2 as a viable material for a front-end low noise amplifier (LNA). We chose a cascode topology to minimize the Miller effect, provide input-output isolation, and improve the overall gain-bandwidth product. The amplifier schematic is shown in Fig. 4a. Figure 4b shows the amplifier gain (S_{21} in dB) and the input match (S_{11} in dB). We see a gain greater than 15 dB operating at 1.2 GHz, attributed to good current saturation. Figure 4c shows the input-output isolation greater than 20 dB at 1.2 GHz as afforded by the cascode topology. The high gain of our front-end amplifier helps with setting the noise floor of the RF receiver. An input match network (IMN) is designed for matching the input impedance (Z_{in}) to the source impedance, R_s = 50 Ω. With the IMN we see input return loss greater than 10 dB. An output match network is employed to improve the gain over the frequency bandwidth of 1.1–1.3 GHz. A standard Chebyshev Nth-order band pass filter topology can be modified for the design of the match networks.[20] We plan to further improve this design to take into account noise parameters for the practical design of MoS_2-based GHz LNAs.

In conclusion, we presented embedded gate CVD MoS_2 RF FETs with an intrinsic f_T and f_{max} of 20 and 11.4 GHz, respectively. From a minimum L_g of 150 nm, we extract a MoS_2 v_{sat} of 1.88×10^6 cm/s, higher than previously reported experimental values. Our devices exhibit enhancement mode operation, I_{ON}/I_{OFF} ratio of 10^8, and the highest CVD MoS_2 g_m of 70 μS/μm. Using the measured *S*-parameters, we demonstrate a MoS_2-based cascode amplifier showing gain greater than 15 dB at 1.2 GHz. Our results advance the state-of-the-art cut off frequencies achievable by CVD MoS_2 and represent a step towards fully integrated MoS_2 smart nanosystems.

MATERIALS AND METHODS

Growth

Large area atomic single layer MoS_2 was grown by a standard vapor transfer process starting from molybdenum trioxide (MoO_3) and sulfur (S) powder in a quartz tube (inner diameter = 22 mm) with a single zone Lindberg/Blue M furnace. Controlled large area growth was accomplished by using masking and target substrates. Both the masking and target substrates used were from the same wafer. The polished side of the substrates faced the MoO_3 precursor. By controlling the distance between individual masking substrates, we could control the area of the continuous

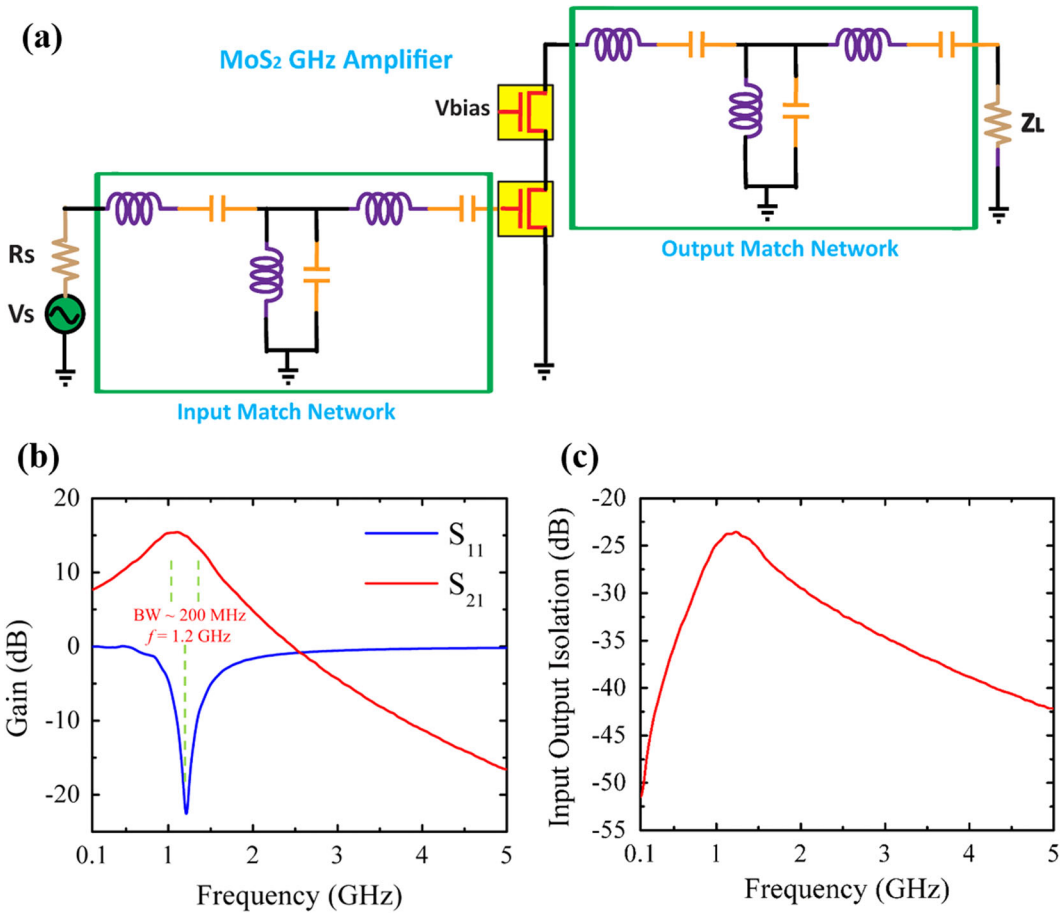

Fig. 4 MoS_2 RF Amplifier **a** Circuit schematic for a MoS_2 GHz cascode amplifier. An input match network is used match to the 50 Ω source impedance. An output match network improves gain and bandwidth. The DC bias is not shown but can be provided by inductors connected to ground. **b** The input match return loss, S_{11}, and the output gain, S_{21}, vs. frequency. We see a gain greater than 15 dB at 1.2 GHz with a bandwidth of about 200 MHz and an input return loss better than 10 dB. **c** Input and output isolation vs. frequency. The cascode topology allows better than 20 dB of isolation as it mitigates the Miller effect

monolayer region. Additional detailed growth methods are available in Section 1 of the SI.

Characterization

Raman and photoluminescence (PL) spectroscopy were done using a Witec Alpha 300 micro-Raman confocal microscope, with the laser operating at a wavelength of 488 nm. Parameters in our mapping were (i) grating (Raman) = 1800 g/mm, (PL) = 600 g/mm; (ii) integration time/pixel = 1 s; (iii) resolution = 3 pixels/μm.

Fabrication methods

The RF MoS_2 transistor fabrication begins with patterning two embedded gate fingers on intrinsic Si/SiO_2 (>20 k Ω·cm). Electron beam lithography (EBL) and e-beam evaporation were used to define and deposit the embedded gate metal stack consisting of 2/23 nm Ti/Au. Horizontal gate lengths were verified to be between 100 and 500 nm. The shortest total L_g is 150 nm; the sum of the horizontal length (100 nm) and the two heights of the sidewalls (50 nm). ALD at 200°C was used to deposit 10 nm of Al_2O_3 as the gate dielectric. Large area CVD MoS_2 was then transferred by poly(methyl methacrylate)-assisted wet transfer. A via to connect the embedded gate fingers with the gate pad was etched with phosphoric acid. The active MoS_2 channel was etched using Cl_2/O_2 plasma. A final EBL step patterned source and drain (S/D) contacts consisting of 2/70 nm Cr/Au.

Electrical measurements

Electrical DC characterization was done on a Cascade Microtech Summit 11000B-AP probe-station using an Agilent B1500A parameter analyzer. The measurements were taken at room temperature, in ambient atmosphere, and in the dark. Microwave performance was characterized from 0.1–15 GHz using an Agilent two-port vector network analyzer (VNA-E8361C) at room temperature, in ambient atmosphere, and in the dark. The OPEN de-embedding was performed on the as-measured device-under-test by etching away the MoS_2 in the active regions. The SHORT de-embedding is subsequently performed by depositing a strip of metal across the channel region, shorting out all pads. The intrinsic parameters are extracted using Equation 3 of the SI.

Data availability

The authors declare that [the/all other] data supporting the findings of this study are available within the paper [and its supplementary information files]. Any additional data that supports the findings of this study are available from the corresponding author upon reasonable request.

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AUTHOR CONTRIBUTIONS

A.S. and S.P. contributed equally to this work and co-wrote the manuscript. R.G. and C.L. performed the synthesis and characterization of the MoS_2 films. A.S. and S.P. performed the design conception, fabrication, and measurements of the MoS_2 transistors. M.N.Y. designed and simulated the MoS_2-based RF amplifier. L.M., R.R., D.A., and S.K.B. directed and supervised the overall experiment. All authors revised and approved the final manuscript.

ADDITIONAL INFORMATION

Supplementary Information accompanies the paper on the *npj 2D Materials and Applications* website (doi:10.1038/s41699-017-0029-z).

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