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Double-gate structure enabling remote Coulomb scattering-free transport in atomic-layer-deposited IGO thin-film transistors with HfO_2 gate dielectric through insertion of SiO_2 interlayer

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In this paper, high-performance indium gallium oxide (IGO) thin-film transistor (TFT) with a double-gate (DG) structure was developed using an atomic layer deposition route. The device consisting of 10-nm-thick IGO channel and 2/48-nm-thick SiO_2/HfO_2 dielectric was designed to be suitable for a display backplane in augmented and virtual reality applications. The fabricated DG TFTs exhibit outstanding device performances with field-effect mobility (μ_{FE}) of 65.1 ± 2.3 $cm^2V^{-1} s^{-1}$, subthreshold swing of 65 ± 1 $mVdec^{-1}$, and threshold voltage (V_{TH}) of 0.42 ± 0.05 V. Both the (μ_{FE}) and *SS* are considerably improved by more than two-fold in the DG IGO TFTs compared to single-gate (SG) IGO TFTs. Important finding was that the DG mode of IGO TFTs exhibits the nearly temperature independent μ_{FE} variations in contrast to the SG mode which suffers from the severe remote Coulomb scattering. The rationale for this disparity is discussed in detail based on the potential distribution along the vertical direction using technology computer-aided design simulation. Furthermore, the DG IGO TFTs exhibit a greatly improved reliability with negligible V_{TH} shift of – 0.22 V under a harsh negative bias thermal and illumination stress condition with an electric field of – 2 $MVcm^{-1}$ and blue light illumination at 80 °C for 3600 s. It could be attributed to the increased electrostatic potential that results in fast re-trapping of the electrons generated by the light-induced ionization of deep level oxygen vacancy defects.

Amorphous oxide semiconductors (AOSs), such as indium–gallium–zinc–oxide (IGZO) and indium–gallium–zinc–tin-oxide (IGZTO), are widely used in display backplane technology for large-area active matrix-liquid crystal display (AMLCD) and -organic light emitting diodes (AMOLED) due to the remarkable electrical characteristics, such as reasonable field-effect mobility (μ_{FE}) of > 10 $cm^2V^{-1} s^{-1}$, ultralow off-currents of < 10^{-18} $A\mu m^{-1}$, and steep switching characteristics[1–12]. However, the emerging augmented and virtual reality (AR/VR) headsets requiring display backplanes with ultrahigh resolution (≥ 2000 ppi) are fabricated using Si CMOS backplanes unlike the traditional flat panel displays, such as mobile and television, where the AOS thin-film transistors (TFTs) have been successfully implemented[13]. To achieve such an ultrahigh resolution using the AOS TFTs, the facile integration process and architecture of submicron scale AOS TFTs should be developed on the glass substrate. Furthermore, their lower on-current (I_{ON}) compared to Si transistors makes it more challenging to utilize the AOS TFTs for AR/VR applications.

In this context, several approaches have been proposed to ensure high mobility AOS TFTs, such as heterojunction structures using quasi-two-dimensional electron gas (q2DEG)[5,11], crystallization[10,12], hydrogen doping[7], and multi-gate architecture[14–19]. Amongst, adopting the multi-gate architecture, such as double-gate (DG), tri-gate

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and gate-all-around (GAA), is considered promising due to the outstanding current boosting ability. In practice, Mativenga et al. reported that IGZO TFTs with DG structure reveal seven times higher I_{ON} than those with single gate (SG) structure due to the bulk accumulation[15]. In addition to the current boosting, it was also confirmed that the DG structure greatly enhances a reliability for positive gate-bias thermal stress (PBTS) duration[16]. More importantly, the multi-gate structure is highly advantageous for overcoming short-channel effects (SCEs). Note that the natural length (λ) which determines the minimum gate length can be described as follows[19,20]:

$$\lambda = \sqrt{\frac{\varepsilon_{ch} t_{ch} t_{OX}}{N \varepsilon_{OX}}} \tag{1}$$

where t_{ch}, t_{ox}, ε_{ch}, ε_{ox}, and N are the thickness and dielectric constants of the bulk channel and dielectric layer, and the effective gate number, respectively. As such, the λ can be reduced by increasing not only the dielectric permittivity (κ) but also the N. For these reasons, the multi-gate structure as well as the high-κ gate dielectric have been adopted for the continual scaling down of Si transistors in the semiconductor industry[8]. Likewise, the AOS TFT based on them should be intensively investigated for its diverse potential applications.

In this study, high-performance IGO TFTs with the DG structure were developed using atomic layer deposition (ALD). Mostly, previous AOS TFTs with the DG structure have been fabricated using the sputtering method for the channel layer deposition. However, it is unsuitable for the three-dimensional (3D) muti-gate architecture due to its poor step coverage[21,22]. In contrast, the ALD-derived gate/channel stack employed in this work offers excellent step coverage and thickness controllability, which is highly suitable for the 3D structure such as GAA and channel-all-around (CAA) etc[23,24]. The choice of 10-nm-thick IGO as a channel layer is due to its low effective electron mass and high μ_{FE}[10]. 2-/48-nm-thick high-κ SiO_2/HfO_2 dielectric films were used as a gate dielectric layer. That is, the λ was designed to be approximately 12.3 nm, which is expected to allow for a short channel length of $\leq$ 100 nm without the noticeable SCEs[25]. An important finding in this study is that the IGO TFTs with the DG structure exhibit the remote Coulomb scattering (RCS)-free transporting mechanism unlike those with the SG structure where the RCS and polar phonon scattering significantly occur[26]. This disparity can be explained by the concept of bulk accumulation, which was demonstrated through technology computer-aided design (TCAD) simulation. This phenomenon helps the Fermi-level (E_F) reach the conduction band edge (E_{CB}) rapidly, greatly improving both the μ_{FE} and subthreshold swing (*SS*) in the DG TFTs. Finally, the photo-bias stability of DG IGO TFTs was found to be superior to that of SG IGO TFTs even under negative bias thermal and illumination stress (NBTIS), which could be attributed to the increased electrostatic potential by the DG structure which greatly promotes the re-trapping of electrons originating from light illumination-induced oxygen vacancy (V_O) ionization.

Methods

Preparation of semiconducting and dielectrics films

Semiconducting oxide film

10-nm-thick IGO thin-films as a channel layer were grown by plasma-enhanced ALD (PEALD) (NexusBe Co. Ltd.). The liquid metal precursors [3-(dimethylamino)propry]-dimethyl indium (DATI) and trimethyl gallium (TMG) were used as the In and Ga precursor, respectively. The DATI canister was heated to approximately 80 °C to provide a sufficient vapor pressure while the TMG canister was kept at room temperature. Each precursor was injected into the source line where high-purity Ar gas (99.999%) was used as a carrier gas for precursor delivery. O_2 plasma was used as an oxidant, which was provided by applying an electric field (plasma power = 150 W) to the Ar/O_2 mixed gas.

Dielectric film

Hafnium oxide (HfO_2) and silicon oxide (SiO_2) films were deposited by the PEALD (iSAC Research, South Korea). The metal precursors used for Hf and Si were diisopro-pylamino silane (DIPAS) and tetrakis ethylmethylamino hafnium (TEMAHf), respectively. The TEMAHf canister was heated to approximately 110 °C to provide a sufficient vapor pressure while the DIPAS canister was kept at room temperature. Likewise, each precursor was carried and purged by high-purity Ar gas.

Film characterizations

The thickness of channel and dielectric films was measured using spectroscopic ellipsometry (Ellipso Technology Co.). The chemical properties of channel and dielectric films were examined through depth-profiling of X-ray photoelectron spectroscopy (XPS) (K-Alpha +, Thermo Fisher Scientific Co.) with an X-ray source of monochromatic Al K_α at 1486.6 eV.

Device characterizations

The DG IGO TFTs were fabricated on thermally grown SiO_2/Si substrate. 50-nm-thick indium-in oxide (ITO) films were deposited by DC magnetron sputtering at room temperature as bottom gate (BG) electrodes. The cation composition ratio is 9:1 (In:Sn). The BG electrodes were patterned through a conventional photolithography and wet etching process. Then, 2-/48-nm-thick SiO_2/HfO_2 gate dielectric stacks were grown by the PEALD at 250 °C. Note that the ultrathin SiO_2 acts as an interfacial stabilizer. Subsequently, 10-nm-thick IGO thin-films were deposited by PEALD at 150 °C, followed by patterning using the photolithography and wet etching process. Next, 50-nm-thick ITO was deposited as source/drain (S/D) electrodes. The S/D electrodes were patterned by the standard photolithography with wet etching process, followed by postdeposition annealing (PDA) at 400 °C in ambient air for 1 h. The fabricated TFTs have the channel width (*W*) and length (*L*) of 60 and 30 µm, respectively. To fabricated the DG TFTs, the same gate dielectric stacks were deposited onto the underlying BG TFTs

and annealed at 400 °C in ambient air for 1 h. Contact holes were formed by reactive ion etching (RIE). Top gate (TG) electrodes were deposited and patterned using the same method with the BG electrodes. Finally, the fabricated TFTs were annealed at 250 °C in ambient air for 1 h. Figure 1 shows a cross-sectional device schematic, an optical top view image, and the entire fabrication process.

Results and discussion

Electrical properties of DG IGO TFTs

Electrical performances of IGO TFTs were evaluated using transfer characteristics at drain-to-source voltage (V_{DS}) of 10 V. Note that the μ_{FE} under a saturation region was calculated using the following equation:

$$\mu_{FE} = \left(\frac{\partial\sqrt{I_D}}{\partial V_{GS}}\right)^2 \frac{2L}{WC_{OX}} \tag{2}$$

where I_D, V_{GS}, and C_{ox} are the drain current, the gate voltage, and, the dielectric capacitance per unit area, respectively. The V_{TH} and SS were determined using linear extrapolation of $I_D^{0.5}$ versus V_{GS} (see Figure S1) and the equation $SS = dV_{GS}/d\log(I_D)$, respectively. Before covering the electrical characteristics, it should be noted that TG (BG) mode means that the input gate voltage is applied to the top (bottom) gate with a floating state of bottom (top) gate. DG mode denotes that the top gate is electrically wired to the bottom gate. BG IGO TFTs with HfO_2 gate dielectric (48 nm) have the reasonable μ_{FE} of 18.1 ± 1 cm^2V^{-1} s^{-1}, SS of 130 ± 5 $mVdec^{-1}$, V_{TH} of 0.22 ± 0.2 V and current modulation ratio ($I_{ON/OFF}$) of ~ 10^9 (Figure S2a and Table S1). It sufferes from the clock-wise hysteresis of 0.3 V, indicating the free electron carrier trapping into the HfO_2 dielectric. Insertion of 2-nm-thick SiO_2 interfacial layer between the IGO and HfO_2 films greatly mitigates the operational hysteresis (0.05 V) in the resulting IGO TFTs (Figure S2b). Simultaneously, the μ_{FE} and SS are improved to 24.7 ± 0.7 cm^2V^{-1} s^{-1} and 110 ± 5 $mVdec^{-1}$, respectively, while the comparable $I_{ON/OFF}$ is maintained (also see Table S1). TG IGO TFTs have almost the same device performances with the reasonable μ_{FE} of 25.8 ± 0.5 cm^2V^{-1} s^{-1}, SS of ~ 134 ± 5 $mVdec^{-1}$, V_{TH} of 0.82 ± 0.1 V and $I_{ON/OFF}$ ratio of ~ 10^{10} (Fig. 2a and Table 1). Meanwhile, DG IGO TFTs exhibit significantly improved device performances with μ_{FE} of 65.2 ± 2.3 cm^2V^{-1} s^{-1}, SS of 65 ± 1 $mVdec^{-1}$, V_{TH} of 0.42 ± 0.05 V, and $I_{ON/OFF}$ of ~ 10^{10}. The enhancement in the μ_{FE} can be explained by a bulk accumulation conduction mechanism, which could occur when the depth of band bending is larger than half of the channel thickness (t_{ch})[15]. The greatly improved SS in the DG mode is attributed to the increased electrostatic potential enabling the E_F to rapidly rise toward the E_{CB}, which can be experimentally demonstrated through the V_{GS}-dependent change of activation energy (E_A) (Fig. 2c): the falling rate (F_R), defined as $|\Delta E_A/\Delta V_{GS}|$, was extracted to 1.13 eVV^{-1} in the DG mode, which is twice as high as the SG mode (~ 0.6 eVV^{-1}). This higher F_R also indicates fast transition from trap-limited conduction to percolation conduction. This improved electron transport can be also observed in the output characteristics, which have a fivefold higher I_D than the SG mode (Fig. 2b). The detailed output characteristics can be seen in Figure S3.

One thing we should identify is which scattering mechanism, phonon scattering or RCS, dominantly affects the electron transport in the IGO TFTs with SiO_2/HfO_2 gate dielectrics. The dominant scattering mode can be distinguished by the differential function for temperature (T) of Matthiessen's rule as follows:

$$d\left(\frac{1}{\mu_{FE}}\right)/dT = \beta\alpha T^{\alpha-1} - \frac{\gamma}{T^2} \tag{3}$$

where α, β, and γ are the positive constants independent of T. A negative value in the $1/\mu_{FE}$-T curve indicates that the RCS is dominant[26]. The larger absolute values, the greater scattering effect. SG IGO TFTs with the 48-nm-thick HfO_2 gate dielectric have the high negative slope of − 15.4 (see Figure S2b and Table S1). It indicates the dominance of RCS, which is greatly mitigated by inserting 2-nm-thick SiO_2. The extracted slope values are − 7.1 ~ − 7.8 in the TG and BG IGO TFTs with the 2-/48-nm-thick SiO_2/HfO_2, respectively (Fig. 2d). More

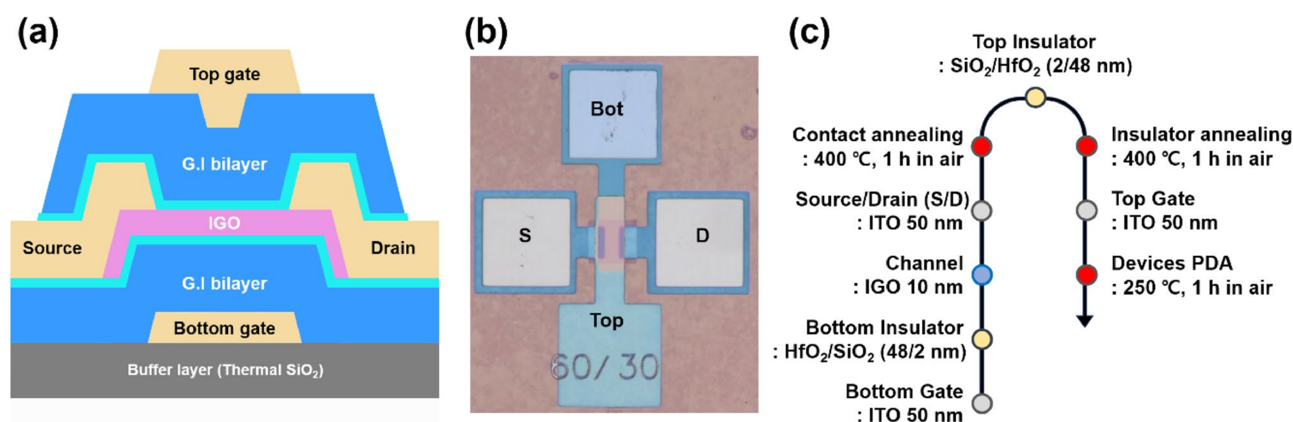

Figure 1. (**a**) A cross-sectional schematic of a DG IGO TFT. (**b**) A false colored top view image. (**c**) The device fabrication procedure.

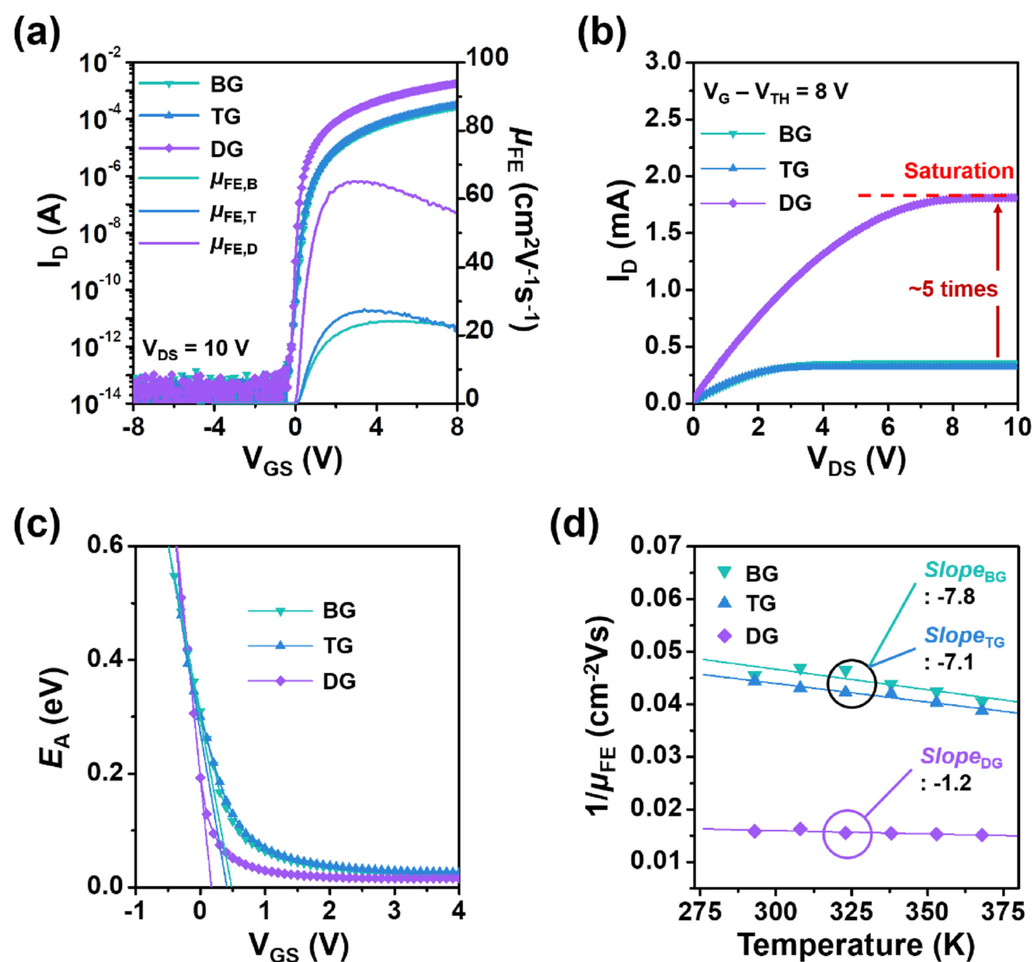

Figure 2. Sweeping gate electrode-dependent electrical characteristics: (**a**) transfer characteristics at $V_{DS} = 10$ V; (**b**) output characteristics; (**c**) variation of E_A; and (**d**) $1/\mu_{FE}$-T characteristics.

	BG	TG	DG
μ_{FE} [cm^2V^{-1} s^{-1}]	24.5 ± 0.8	25.8 ± 0.5	65.2 ± 2.3
SS [$mVdec^{-1}$]	146 ± 5	134 ± 5	65 ± 1
V_{TH} [V]	0.94 ± 0.1	0.82 ± 0.1	0.42 ± 0.05
$I_{ON/OFF}$	~ 10^{10}	~ 10^{10}	~ 10^{11}
I_D @ $V_{GS} - V_{TH} = 8$ V [mA]	0.38	0.33	1.85
Falling rate [eVV^{-1}]	0.62	0.67	1.13
Slope value	− 7.8	− 7.1	− 1.2

Table 1. Summary of electrical figures of merit of the IGO TFTs with different driving gate electrodes.

importantly, it is further reduced down to – 1.2 in the DG TFTs, which implies that the RCS effect revealed in the SG TFTs (either BG or TG) greatly diminishes (Fig. 2d and Table 1). That is, it could be possible that the RCS-free zone is formed and contributes to the improvements in the electrical characteristics in the DG IGO TFTs.

Chemical and dielectric properties of SiO_2/HfO_2

Chemical states of the SiO_2/HfO_2 film stack were examined through XPS analysis to investigate the possible origin of RCS in the SG IGO TFTs. Figure 3a,b show the deconvoluted O 1*s* XPS spectra into five bases, corresponding to oxygen bonded to fully coordinated metal ions (Hf–O: 530.0 ± 0.1 eV, Hf–O–Si: 531.5 ± 0.1 eV, Si–O: 533.0 ± 0.1 eV) and under-coordinated oxygen related to oxygen vacancies (V_O: 531.0 ± 0.1 eV), and impurity oxygen species (532.0 ± 0.1 eV)[27–30]. In the bulk region of HfO_2, the Hf–O related peak is dominant (~ 91.3%). Meanwhile, hafnium silicate (Hf–O–Si) related sub-peak becomes dominant (~ 87.0%) in the SiO_2/HfO_2 interfacial area, indicating that the Hf element diffuses into the ultrathin SiO_2 film during thermal annealing process.

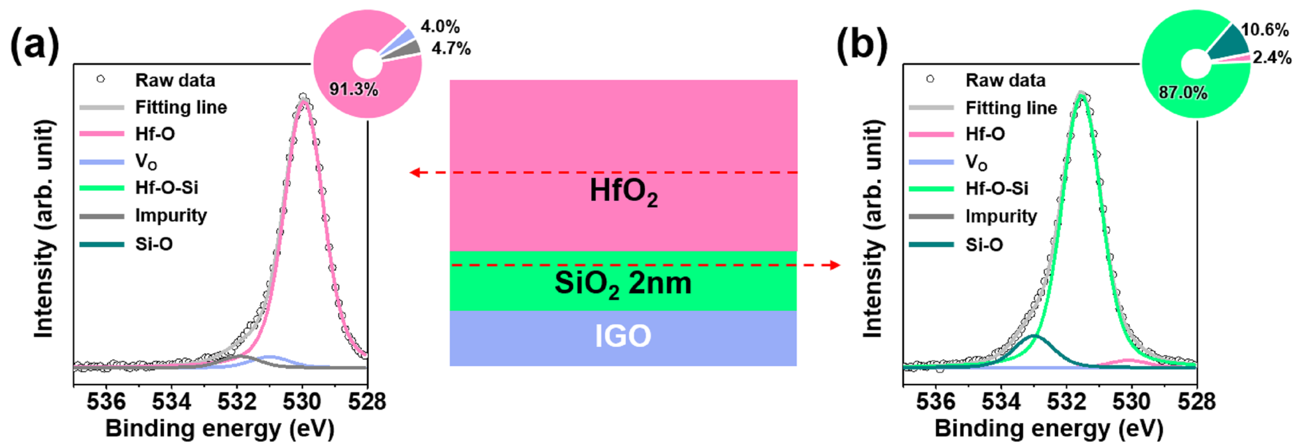

Figure 3. Deconvolution of the O 1*s* XPS spectra peak for (**a**) HfO_2 and (**b**) SiO_2 films.

The increase in the Hf–O–Si bond can be partially attributed to the strong binding nature of Si resulting in second neighbor effect[30]. To double-check the formation of Hf–O–Si layer, Si *2p* and Hf *4f* XPS spectra were also analyzed as shown in Figure S4. In the interfacial area, the main subpeak in the Si *2p* spectra appears at 103 eV, which implies the Hf–O–Si formation[29,31]. The blue-shift of Hf *4f* XPS spectra which occurs at the interface also indicates the strong bond formation of Hf–O–Si (Figure S4c)[32].

The chemical properties are anticipated to affect their dielectric properties. The dielectric permittivity (κ) of SiO_2, HfO_2 and SiO_2/HfO_2 film stack was characterized by fabricating metal–insulator–metal (MIM) capacitors. The capacitances of MIM capacitors with SiO_2 (8 nm) and HfO_2 (48 nm) films were investigated through capacitance-frequency measurements. The κ values are obtained to 3.9 and 18.0 for the SiO_2 and the HfO_2, respectively (Fig. 4a). Using these values, the κ of the 2-/48-nm-thick SiO_2/HfO_2 can be estimated using the following equation:

$$\frac{1}{C} = \frac{1}{C_{Hf}} + \frac{1}{C_{Si}} \rightarrow \frac{t_{HS}}{\kappa_{HS}} = \frac{t_{Hf}}{\kappa_{Hf}} + \frac{t_{Si}}{\kappa_{Si}} \tag{4}$$

where t_{HS}, t_{Hf}, and t_{Si} are physical thickness of SiO_2/HfO_2, HfO_2, and SiO_2, respectively, and κ_{HS}, κ_{Hf}, and κ_{Si} are the corresponding films' κ values. While the value calculated from the Eq. (4) is 15.7, the κ_{HS} value of SiO_2/HfO_2 extracted from the capacitance measurements is 16.5 (Fig. 4b). This disparity supports that the ultrathin SiO_2 is converted to the hafnium silicate with the substantially higher permittivity ($\kappa \sim 12$)[29,33] during the thermal annealing process. Reduced hysteresis and higher μ_{FE} for the IGO TFTs with the SiO_2/HfO_2 could be attributed to the less interfacial trap density of hafnium silicate than the HfO_2 film.

Figure 5a,b show schematic band diagrams to understand the RCS effect on electron transport during SG mode and DG mode, respectively. As the V_{GS} increases, the energy band of IGO with a number of subgap trap states (N_T) bends downward. Note that the depth of band bending, which is often defined as the screening length,

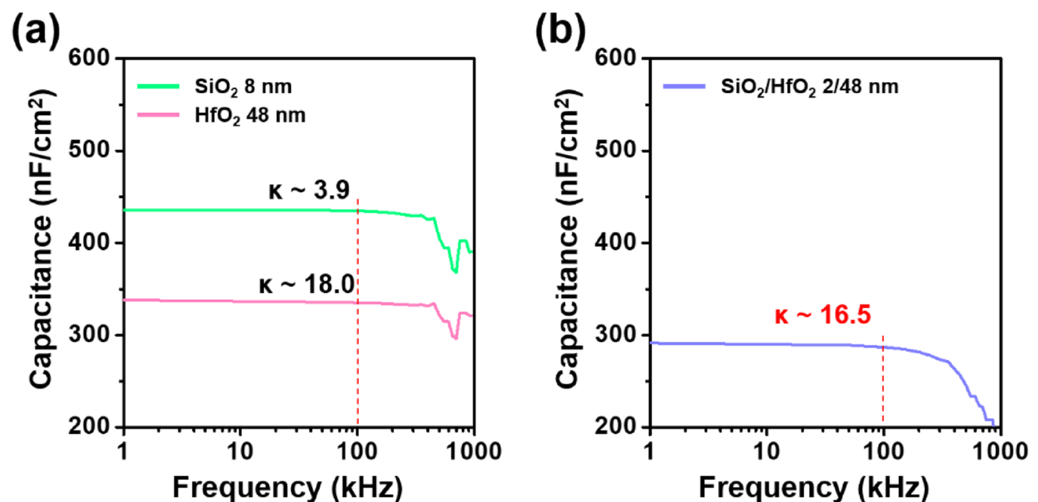

Figure 4. Capacitance-frequency characteristics of MIM capacitors with (**a**) SiO_2 and HfO_2, and (**b**) SiO_2/HfO_2 films.

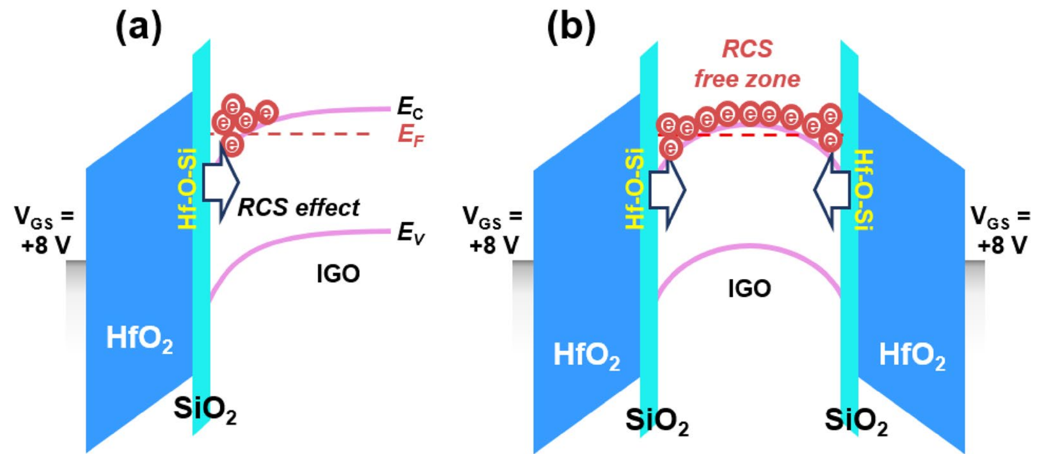

Figure 5. (**a**,**b**) Band diagram schematics with different driving types: (**a**) SG mode; (**b**) DG mode.

is inversely proportional to the concentration of N_T[34,35]. Given that the depth of V_{GS}-driven band bending is less than T_{ch}, most of the free electrons exist only near the channel/gate dielectric interface (Fig. 5a). In this context, the electron transport is hampered by the RCS in the SG mode. In contrast, the free electrons can be distributed throughout the entire channel for the DG mode (Fig. 5b), because the V_{GS}-driven band bending occurs at both sides. As a result, the RCS-free zone can be formed via the bulk accumulation in the DG IGO TFTs, improving the electron transport.

TCAD simulation and NBTIS reliability of DG IGO TFTs

Our interpretation on basis of screening length versus T_{ch} relation was confirmed by performing the TCAD simulation. The band structure, the density gradient quantum effect model, the remote Coulomb/phonon scattering models and the subgap density of states (DOS) were incorporated into SILVACO ATLAS. More accurate subgap density of interface states (D_{it}) was extracted by unified subthreshold coupling factor technique[36,37]. Figure 6a shows comparison of D_{it} distributions for different driving mode of TFTs, which were modelled by using two exponential functions as follows:

$$D_{it}(E) = N_{tail}exp\left(-\frac{E_{CB}-E}{kT_{tail}}\right) + N_{deep}exp\left(-\frac{E_{CB}-E}{kT_{deep}}\right) \quad (5)$$

where N_{tail}, N_{deep}, kT_{tail} and kT_{deep} are the density of acceptor-like tail states, the acceptor-like deep states (N_{deep}), the characteristic energy of tail states, and the characteristics energy of deep states, respectively. The parameters are summarized in Table 2. It was confirmed that the DG mode possesses a lower D_{it} compared to to the SG mode, even if the DG TFTs have physically two interfaces. This D_{it} reduction can be understood as a result reflected by the RCS-free zone as discussed earlier. Figure 6b,c show the energy level and the current density depending on the driving mode. It was confirmed that the E_F is closely located to the E_{CB} throughout the entire channel due to the bulk accumulation in the DG mode unlike the SG mode. As a result, the drain-current density in the DG mode is significantly higher than the SG modes, which also can be seen in Fig. 6d–f that show the cross-sectional drain-current density contours. Overall, these results demonstrate that the electron transport is greatly improved by the bulk region, the RCS-free zone, in the DG mode, which affirms the relatively minor influence of interfacial effects compared to the SG mode. Note that the simulated transfer characteristics for each driving mode is well matched with the experimental results (Figure S5). The detailed parameters of the materials and structures used in TCAD are summarized in Table S2.

Finally, negative gate bias illumination stress (NBIS) reliability was investigated for the different driving modes under the external stress conditions with an electric field of − 2 $MVcm^{-1}$ ($V_{GS} - V_{TH} = -10$ V) and the green light illumination of 0.3 $mWcm^{-2}$ (λ = 533 nm, 2.3 eV). The representative stress time-dependent transfer characteristics during the NBIS duration can be seen in Figure S6. It was confirmed that there are parallel shifts without involving the stretch-out of subthreshold I_D region regardless of the driving mode, suggesting that there is no noticeable defect creation during the NBIS duration. More importantly, the V_{TH} shift (ΔV_{TH}) is remarkably reduced in the DG mode (Fig. 7a). While the BG (TG) IGO TFTs show an inferior NBIS instability with the ΔV_{TH} of − 4.5 (− 3.6) V, respectively, after 3600 s, the DG TFTs exhibit the negligible ΔV_{TH}. Furthermore, the DG IGO TFTs reveal the outstanding reliability with the ΔV_{TH} of − 0.22 V even under the NBTIS with the blue light illumination of 64 μWcm^{-2} (λ = 463 nm, 2.7 eV) at 80 ℃ (Fig. 7b). These highly improved reliabilities could be related to the electron generation by the light illumination-driven transition from deep-level neutral V_O defects to V_O^{2+} states[38–40]. In detail, the photo-induced V_O^{2+} defects and free electron carriers are separated by the negative gate bias during the NBIS duration. In the SG mode, the photo electrons are repelled in the direction opposite to the biased gate electrode and accumulated. As a result, they greatly increase the electron concentration of IGO (Fig. 7c), deteriorating the NBIS reliability. Meanwhile, in the DG mode, the photo electrons cannot be

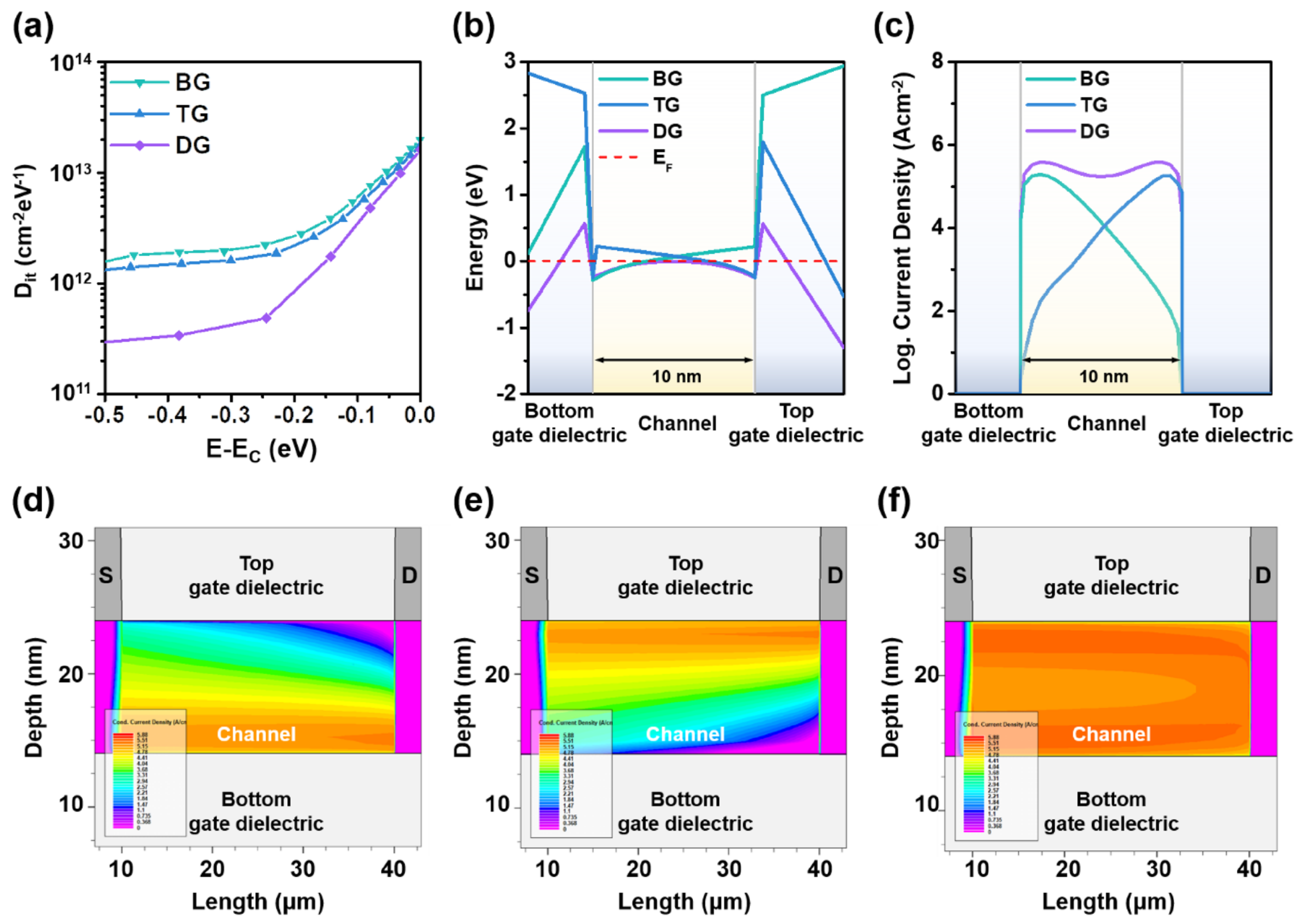

Figure 6. Driving mode-dependent (**a**) the D_{it} distributions, (**b**) the energy band diagrams, and (**c**) the depth profiles of current density. Profiles of the current density for the TFTs with (**d**) the BG, (**e**) the TG, and (**f**) the DG mode. Note that the applied V_{GS} and V_{DS} are 8 and 10 V, respectively.

	BG	TG	DG
N_{tail} [cm^{-2} eV^{-1}]	1.60×10^{13}	1.55×10^{13}	1.50×10^{13}
kT_{tail} [eV]	0.060	0.058	0.058
N_{deep} [cm^{-2} eV^{-1}]	3.5×10^{12}	2.5×10^{12}	8.0×10^{11}
kT_{deep} [eV]	0.45	0.45	0.25

Table 2. Electrical parameters used in the TCAD simulation for the comparison of D_{it} distributions.

accumulated at one side, which results in significant shrinkage of the electron transverse path, leading to fast re-trapping (Fig. 7d). For this reason, the electron concentration does not increase in the DG mode, showing the high reliabilities even under the light illumination.

It is noteworthy that the electrical characteristics of DG IGO TFTs obtained in this study is comparable to state-of-the-art DG AOS TFTs. The μ_{FE} and *SS* values of DG AOS TFTs with different gate dielectric materials are summarized in benchmarking graphs (Fig. 8)[40–49]. These promising performances of fabricated DG IGO TFTs should be attributed to (1) the usage of a high-quality ALD-derived IGO and high-κ HfO_2 dielectric films, (2) RCS-free device design on basis of bulk accumulation mode.

Conclusion

In this study, high-performance DG IGO TFTs were fabricated using PEALD. The SG IGO TFTs with 2-/48-nm-thick SiO_2/HfO_2 exhibited the moderate device performances with μ_{FE} of 24.7 cm^2V^{-1} s^{-1}, *SS* of 110 $mVdec^{-1}$, and $I_{ON/OFF}$ of ~ 10^9. Importantly, the DG IGO TFTs revealed greatly improved device performances with μ_{FE} of 65.2 ± 2.3 cm^2V^{-1} s^{-1}, *SS* of 65 ± 1 $mVdec^{-1}$, and $I_{ON/OFF}$ of ~ 10^{10}. This disparity can originate from the bulk accumulation, the formation of RCS-free zone, because the electron transport via the RCS-free zone helps the E_F reach the E_{CB} rapidly. This elucidation was supported through TCAD simulation. Finally, it was confirmed that the DG IGO TFTs show the photo-bias stability much superior to the SG IGO TFTs, which can be attributed

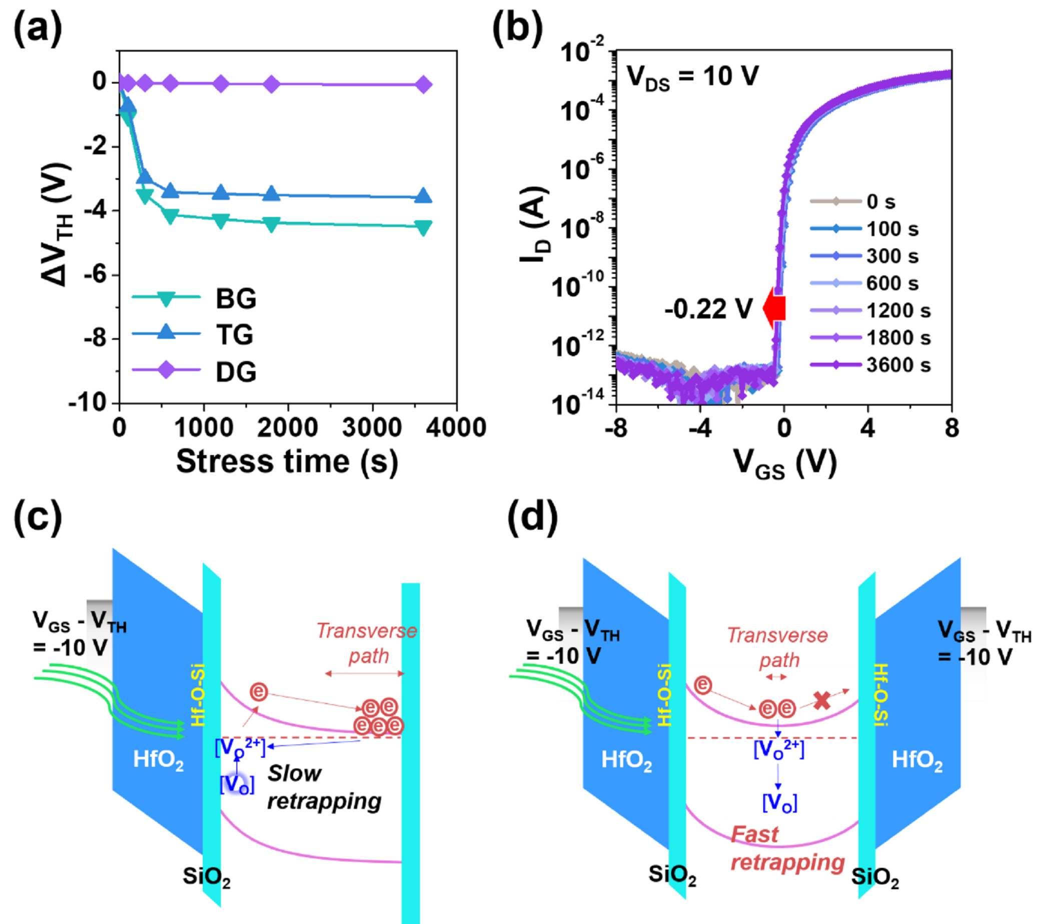

Figure 7. (**a**) Variations of ΔV_{TH} under the NBIS condition. (**b**) Stress-time dependent change of transfer characteristics of the DG IGO TFTs under the NBTIS condition. Band diagram schematics under the NB(T)IS condition for (**c**) the SG mode and (**d**) the DG mode.

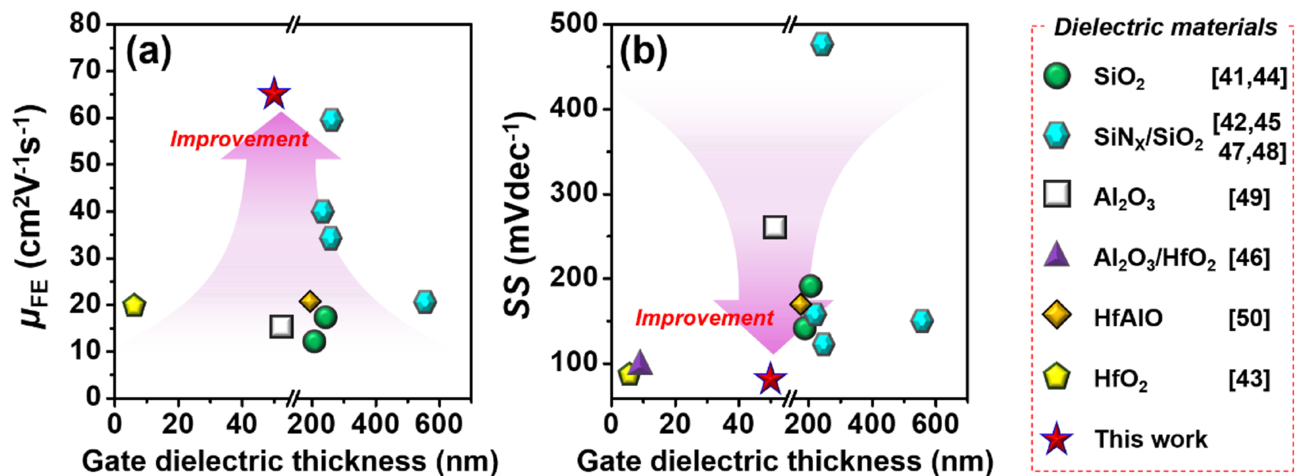

Figure 8. Benchmarks of (**a**) the μ_{FE} and (**b**) the *SS* for the DG AOS TFTs.

to the fast re-trapping of the photo electrons released from deep-level V_O defects. It should be emphasized that even if this study focuses on effects of the DG structure on the IGO TFTs, the obtained results can be applicable to more advanced multi-gate AOS TFTs.

Data availability

The datasets used and/or analyzed during the current study available from the corresponding author on reasonable request. Correspondence and requests for materials should be addressed to J.K.J. (email: jkjeong@hanyang.ac.kr).

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Author contributions

C.H.C. and J.K.J. designed this work. C.H.C., T.K. and J.K.J. wrote the main text. C.H.C. fabricated and characterized the devices. M.J.K., G.-B.K. and J. E. O. assisted the preparation of TCAD simulation and oxide films by PEALD. All author discussed the results and commented on the manuscript. The project was supervised by J.K.J.

Competing interests

The authors declare no competing interests.

Additional information

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