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Core-insulator embedded nanosheet field-effect transistor for suppressing device-to-device variations

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Nanosheet field-effect transistors (NSFETs) have attracted considerable attention for their potential to achieve improved performance and energy efficiency compared to traditional FinFETs. Here, we present a comprehensive investigation of core-insulator-embedded nanosheet field-effect transistors (C-NSFETs), focusing on their improved performance and device-to-device (D2D) variability compared to conventional NSFETs through three-dimensional device simulations. The C-NSFETs exhibit enhanced direct-current (DC) performance, characterized by a steeper subthreshold slope and reduced off-current, indicating better gate electrostatic controllability. Furthermore, the structural design of C-NSFETs enables to demonstrate a notable resilience against D2D variations in nanosheet thickness and doping concentration. In addition, we investigate the effects of interface traps in C-NSFETs, emphasizing the importance of thermal oxidation processes in the formation of core-insulating layers to maintain optimal device performance.

In the ongoing pursuit of advancements in semiconductor device technology aimed at augmenting the performance and minimizing the power consumption, diverse transistor structures have been investigated. Among these, nanosheet field-effect transistors (NSFETs) have emerged as promising alternatives to the conventional transistor structure, which consists of thin layers of channel material enclosed by horizontal gate electrodes[1,2]. An advantage of the NSFET is its superior electrostatic control over the channel with higher current drivability compared to other structures, such as nanowire-FETs[3–5]. Moreover, the performance of the NSFET can be easily adjusted by modifying the nanosheet width or stacking multiple nanosheets. Another critical advantage of NSFETs is their compatibility with the conventional FinFET fabrication processes. This compatibility, along with the enhanced performance metrics of NSFET, establishes them as an increasingly feasible alternative to FinFET technology, especially for advanced semiconductor technologies beyond the 5 nm node[1].

However, as devices continue to scale down, NSFETs face challenges in sustaining improved performances. To address this issue, a structural modification involving the integration of an ultrathin SiGe shell layer within or around an Si nanosheet has been proposed[6–8]. These shell-type NSFETs exhibited improved DC performance and reduced negative-bias temperature instability, which was attributed to the modified energy band configuration. Additionally, the lattice mismatch between the nanosheet and shell induces strain effects, which consequently elevate the carrier mobility, contributing to improved on/off current ratios and subthreshold slopes. Despite these advancements, a comprehensive understanding of the shell-type NSFETs is crucial. A key concern is the device-to-device (D2D) variability, which primarily stems from fluctuations in nanosheet thickness, variations in shell layer dimensions, and inconsistencies in channel doping concentrations[9,10]. Additionally, interface traps resulting from defects at the nanosheet-shell interfaces are another source of variability. These traps can adversely affect device characteristics, including mobility degradation and threshold voltage instability[11–13]. Therefore, understanding the nature and impact of these D2D variabilities is imperative to improve the performance and reliability of advanced NSFETs.

Notably, an alternative structural design for NSFET, that is, core-insulator-embedded NSFET (C-NSFETs), has been proposed recently[14]. It incorporated a thin insulating layer within the nanosheet to reduce the leakage current relative to conventional NSFET. While the initial conception of C-NSFET highlighted its potential in

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improving DC performance metrics, several critical aspects of the C-NSFET remain unexplored. In this study, we aim to bridge this knowledge gap by presenting a comprehensive analysis of the C-NSFET, particularly focusing on its device-to-device (D2D) variability. We investigate the variations in nanosheet thickness, channel doping concentration, and the impact of interface traps on the performance of the C-NSFET. Our approach involves an examination of the additional fabrication processes required for the C-NSFET, such as oxidation and epitaxial silicon growth, and their potential to induce variabilities that could compromise device performance. By employing a three-dimensional device simulation, we demonstrate that the C-NSFET not only maintains enhanced DC performance but also exhibits improved resilience against D2D variations. These findings indicate that the C-NSFET represents a feasible pathway for further device scaling in semiconductor technology, potentially exceeding the capabilities of conventional NSFET, particularly in terms of reliability and stability.

Result and discussion

Device structure and simulation methodology

Figure 1a presents three-dimensional schematics of the C-NSFET, accompanied by two-dimensional cross-sectional views. Figure 1b presents details of the design parameters, which conform with the International Technology Roadmap for Semiconductors (ITRS) guidelines for 5 nm technology node. In our analysis, subsequent parameters are held constant: nanosheet width (50 nm), spacer length (5 nm), number of nanosheets (3 nanosheets), equivalent oxide thickness (0.76 nm), workfunction of TiN gate (4.6 eV), source/drain doping concentrations (5×10^{20} cm^{-3}), supply voltage (0.7 V, which is equivalent to the gate and drain voltages), and thickness of core-insulating layer (2 nm). The nanosheet thickness (t_N), gate length (L_G), channel doping concentration (N_{ch}), and interface trap density (N_{it}) were treated as variables in this study. Figure 1c shows a comparison of the fabrication process of the C-NSFET with that of a conventional NSFET. This process involves the selective etching of SiGe layers from cross-stacked SiGe/Si layers, which is the standard process for NSFET fabrication. Notably,

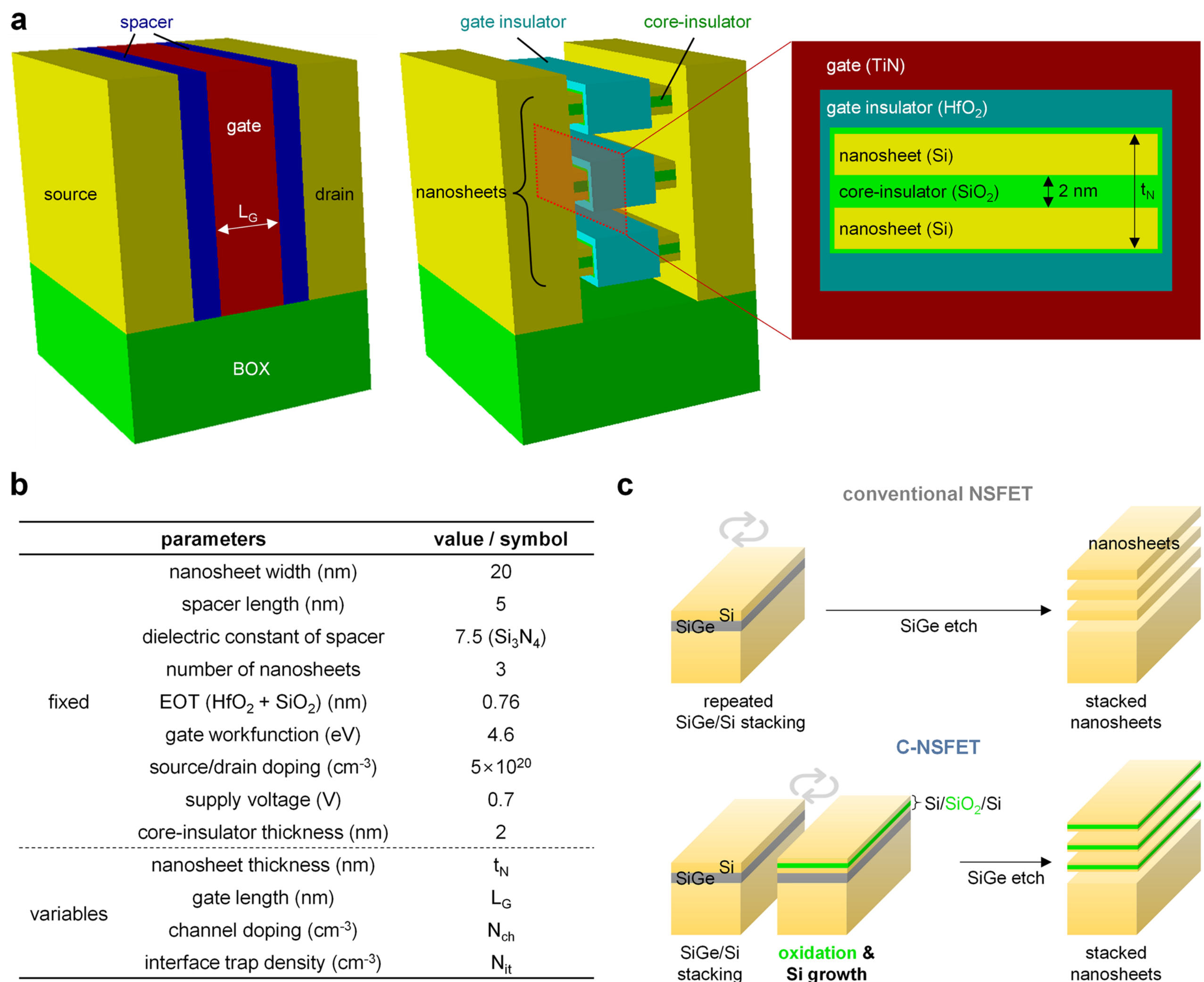

Figure 1. Device structure and parameters for C-NSFET. (**a**) Three-dimensional and cross-sectional views of the C-NSFET. (**b**) Design parameters of C-NSFET. (**c**) Fabrication process flow comparison between the conventional NSFET and C-NSFET.

the C-NSFET process incorporated additional thermal oxidation and Si growth steps, forming a core-insulating layer within the Si nanosheets. Here, thermal oxidation permits a minimized N_{it} at the interfaces between the Si nanosheet and SiO_2 core-insulating layer, in the order of ~ 10^{10} cm^{-2}[15] Additionally, thermal oxidation enables precise control over the thickness of the core-insulating layer[16], which is essential for mitigating D2D variations and will be further elucidated in subsequent discussions.

All device simulations in this study were executed using the SILVACO ATLAS software. We employed a series of sophisticated models to align our simulations with empirical data. The Boltzmann transport equation enabled an accurate simulation of the carrier transport dynamics within the devices. Both the Shockley–Read–Hall model and trap-assisted Auger recombination models are crucial for evaluating the effects of carrier generation and recombination phenomena, particularly those associated with interface traps. In addition, Lombardi's mobility model accounts for various scattering mechanisms, including phonon/Coulomb and surface roughness scattering. Moreover, our simulations integrated field- and concentration-dependent mobility models to precisely capture any potential degradation in carrier mobility. To assess the influence of interface traps at the interfaces between the Si nanosheet and core-insulating layer, we included the observed characteristics of interface traps in Si/SiO_2[17] in our simulations. These trap energy levels were assigned to a single energy level located 0.2 eV away from both the conduction-band and valence-band edges. The capture cross-sections for electrons and holes were assigned as 10^{-13} and 10^{-14} cm^2 respectively. Unless specifically analyzing the impact of changing N_{it}, N_{it} was maintained at a fixed value of 10^{10} cm^{-2}. To validate the robustness and accuracy of our simulation methodology, we compared our simulation with experimental data[1], as depicted in Fig. 2. Our simulation results agree with the empirical data, demonstrating the effectiveness of our method in providing reliable and accurate predictions of the C-NSFET performance and behavior.

DC performances

Figure 3a presents the transfer characteristics (i.e., drain current-gate voltage, I_D–V_G) for both the C-NSFET and conventional NSFET. Notably, the C-NSFET exhibited a steeper subthreshold slope and suppressed the off-current compared to the conventional NSFET, indicating enhanced gate electrostatic control in the C-NSFET. Figure 3b illustrates the electron density distribution near the source junction under the fully on-state condition ($V_G = V_D = 0.7$ V) for both device structures. The conventional NSFET exhibits a concentration of electron density predominantly near the nanosheet surface, with a notable decrease toward its core, indicating limited gate control over the core region of the nanosheet. In contrast, the C-NSFET has a more uniform electron density distribution across the nanosheet. This phenomenon is known as volume inversion, which is observable in an ultra-thin body[18,19]. Consequently, the C-NSFET enhanced the gate controllability over the entire nanosheet region, preventing short-channel effects (SCEs). Figure 3c and 3d further elaborate on this aspect by depicting the drain-induced barrier lowering (DIBL) and subthreshold slope (SS) behaviors as functions of the gate length (L_G), providing a measure of the resistance of the devices to SCEs. The C-NSFET exhibits reduced DIBL and SS values compared to the conventional NSFET, confirming its superior gate controllability.

Device-to-device variations

As discussed previously, D2D variations have become a critical concern in modern device technology. These variations arise from diverse sources, intricacies in fabrication processes, inherent properties of the materials used, and specific geometries of the devices. NSFETs with extremely scaled dimensions of approximately 5 nm for t_N and < 10 nm for L_G are vulnerable to D2D variations. Consequently, even minor deviations in these dimensions in the order of 1–2 nm, can have a significant impact on the device performance. Random dopant fluctuation (RDF) is another critical source of D2D variability in NSFETs. The inherently stochastic nature of ion implantation and diffusion processes in the fabrication of nanosheets can lead to inconsistencies in doping concentration and dopant placement within the channel region. Such variations directly influence the performance metrics of

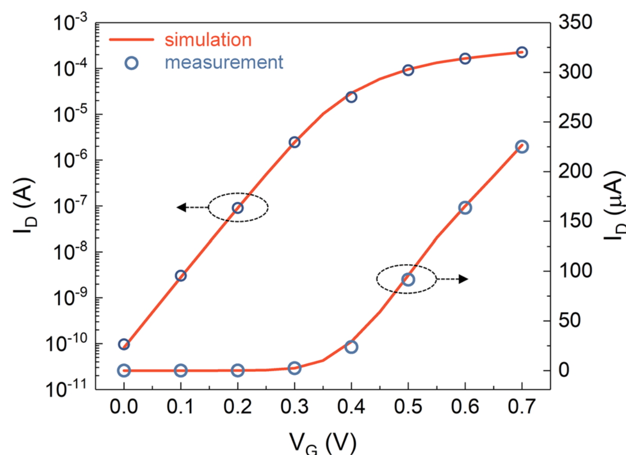

Figure 2. Validity of our simulation methodology. Calibration of simulation result with experimental in Ref.[1].

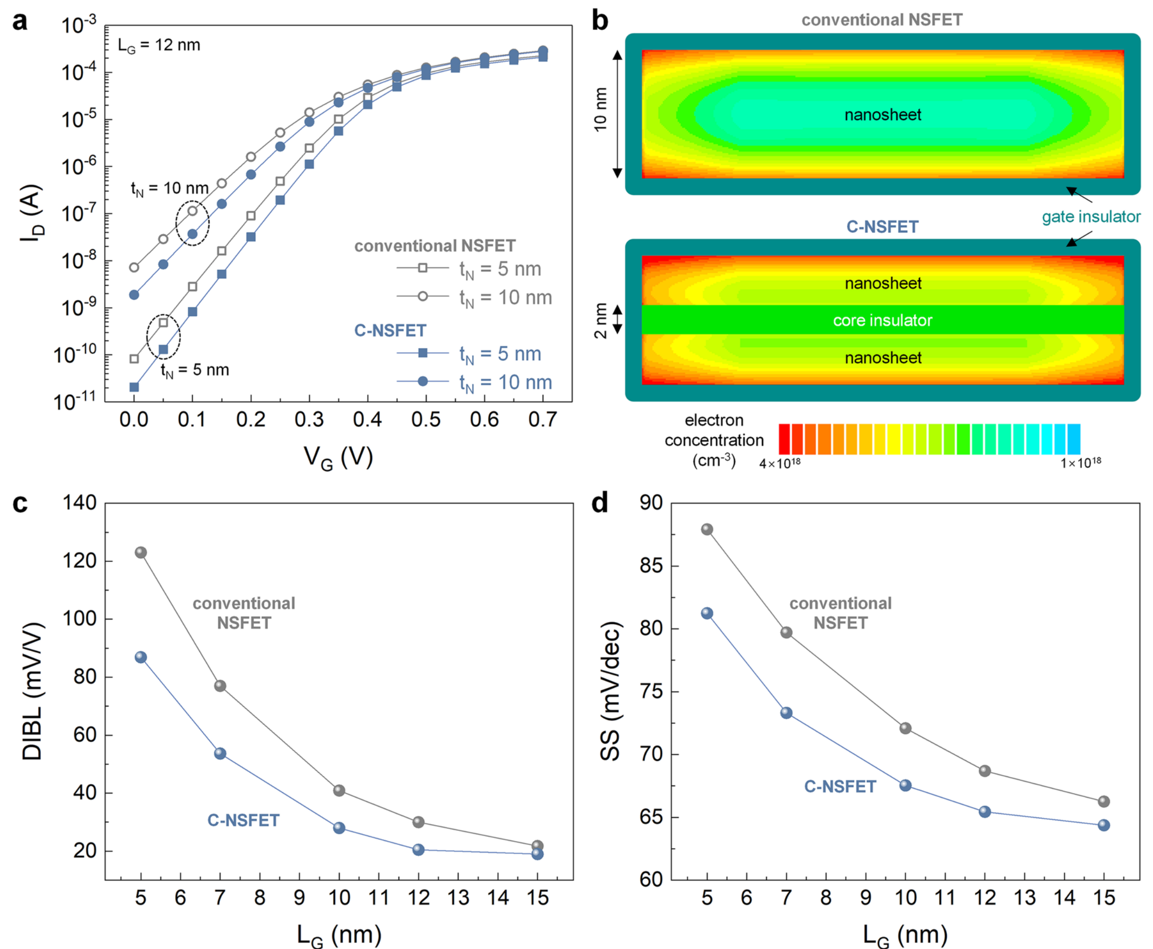

Figure 3. DC performance comparison. (**a**) Transfer characteristics of both the C-NSFET and conventional NSFET, in the case of t_N are 5 and 10 nm. Here, L_G and V_D are fixed to 12 nm and 0.7 V, respectively. (**b**) The cross-sectional contour map of electron concentration near the source junction, when both devices are fully on-state ($V_G = V_D = 0.7$ V). (**c**) DIBL and (d) SS characteristics of both devices, as a function of L_G.

the NSFETs, including the threshold voltage, drive current, and power efficiency. Given these considerations, a comprehensive characterization of D2D variations is imperative to ensure reliable performance of NSFETs.

Figure 4a presents the simulated results of the threshold voltage (V_T) for both the conventional NSFET and the C-NSFET, considering the variations in t_N and N_{ch}. To analyze these results comprehensively, Fig. 4b and c were reconstructed into box-and-whisker plots, where the boxes represent the lower and upper quartiles, and the whiskers indicate the minimum and maximum values. Specifically, Fig. 4b focuses on the V_T variation in response to fluctuations in N_{ch} (ranging from 10^{16} to 10^{18} cm^{-3}), under a fixed t_N. This analysis aims to ascertain the impact of RDF on V_T. Notably, the C-NSFET exhibits a smaller V_T variation than the conventional NSFET. This enhanced resistance to RDF can be attributed to the narrower nanosheet thickness of the C-NSFET. As already discussed in Fig. 3b, the higher gate controllability achieved from thinner nanosheets can suppress the V_T variation due to RDF, which is the same result studied previously in fully-depleted silicon-on-insulator (FDSOI) FETs[20–22]. This enhanced gate controllability results in a more uniform potential distribution in the channel region. Consequently, the influence of localized dopants is diminished. Moreover, volume inversion, that is, uniformity in the inversion charge distribution, also helps mitigate the local fluctuations in the potential caused by random dopants.

Additionally, Fig. 4c illustrates the V_T variation in response to fluctuations in t_N (ranging from 5–10 nm) while maintaining a constant N_{ch}. The main focus of this analysis is to investigate the potential impact of the additional oxidation process in the C-NSFET, because fluctuations in t_N may occur during the formation of the core-insulating layer. Remarkably, the C-NSFET exhibits a V_T variation that was almost equivalent to that of a conventional NSFET. In the C-NSFET, the embedded core-insulating layer reduces the channel thickness, leading to a larger relative change in the channel thickness for the same absolute t_N variation. Nevertheless, both devices exhibit comparable V_T variations, suggesting that the D2D variation caused by oxidation in the C-NSFET is minimal. Consequently, the C-NSFET demonstrates enhanced resistance to D2D variations compared with the conventional NSFET in terms of fluctuations in t_N and N_{ch}. Such stability is particularly crucial in advanced very-large-scale integration (VLSI) technology, in which the integration of a vast number of devices onto a single chip with high uniformity in device performance is required.

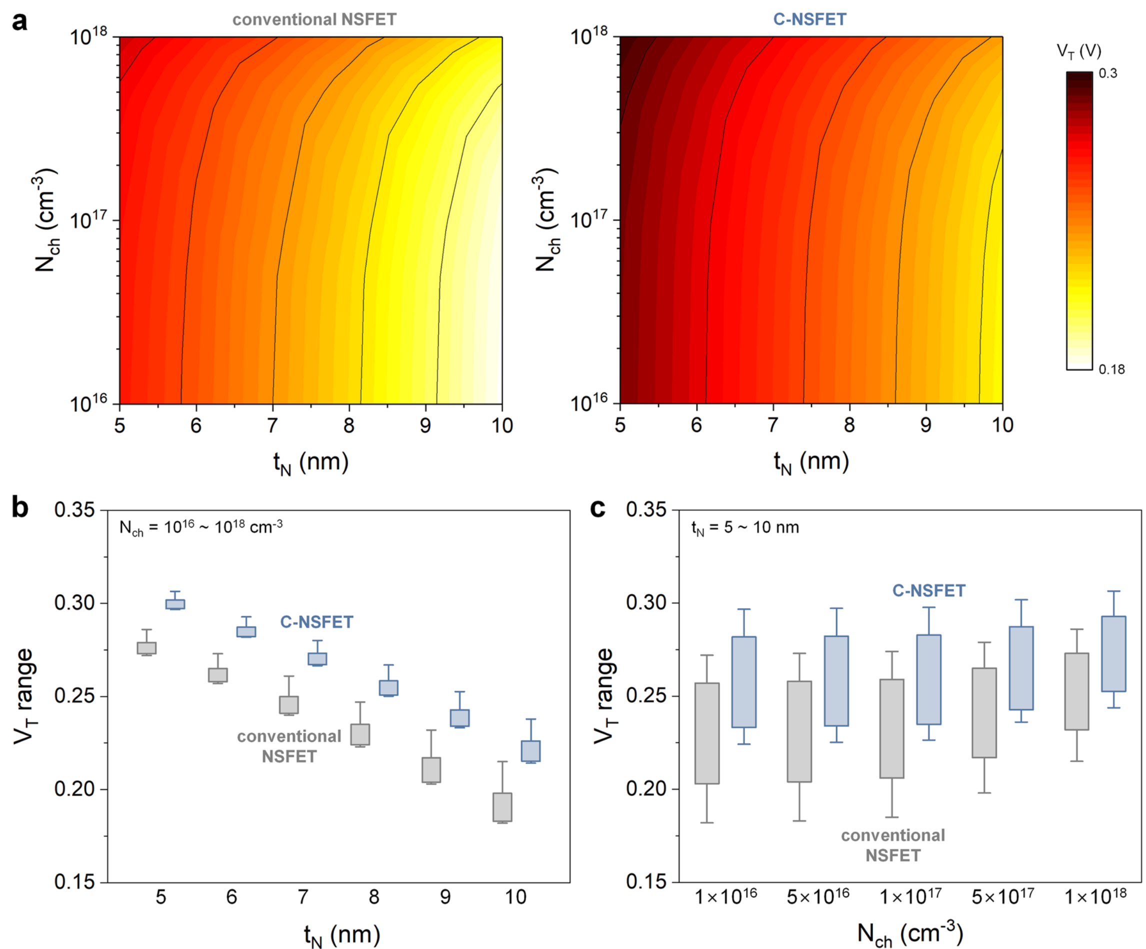

Figure 4. D2D variability of C-NSFET. (**a**) V_T values corresponding to the variations of N_{ch} and t_N. The C-NSFET displays a slightly larger V_T than the conventional NSFET in all cases. Figure 4(**a**) is reconstructed to box-and-whisker plots, representing V_T variations in response to (**b**) fluctuations of N_{ch} ($10^{16} \sim 10^{18}$ cm^{-3}) with a fixed t_N, and (**c**) fluctuations of t_N (5 ~ 10 nm) with a fixed N_{ch}.

The effects of interface traps

The emergence of traps at the interfaces between the nanosheets and core-insulating layers is a critical concern in the development of C-NSFETs. The incorporation of core-insulating layers within these nanosheets inherently introduces additional interfaces, potentially increasing N_{it} relative to that of conventional NSFET. The carrier scattering or trapping induced by these interface traps can detrimentally affect the device performance. To mitigate the generation of interface traps, we employed thermal oxidation to form the core-insulating layer in the C-NSFET, maintaining N_{it} of 10^{10} cm^{-2}[17] However, thermal oxidation did not prevent the increase in the number of interface traps along the sidewalls of the nanosheet[23]. Moreover, the utilization of high-k dielectrics for the core-insulating layer can increase N_{it} to approximately 10^{12} cm^{-2}[24]. Consequently, a thorough understanding of the impact of these interface traps is imperative to ensure the reliability and consistency of C-NSFET performance.

Figure 5a and 5b show the DIBL and SS behaviors in both the conventional NSFET and the C-NSFET as a function of N_{it}. As already discussed in Fig. 3c and d, the C-NSFET shows lower DIBL and SS values than the conventional NSFET, with a low N_{it} (10^{10} cm^{-2}). When N_{it} is increased to 10^{11} cm^{-2}, noticeable differences could not be observed in DIBL and SS values compared to the 10^{10} cm^{-2} level. However, with a further increase in N_{it} to 10^{12} cm^{-2}, both the DIBL and SS values were significantly degraded. These findings indicate that the thermal oxidation process is critical in forming the core-insulating layer to minimize N_{it} below 10^{11} cm^{-2}. Notably, the C-NSFET exhibits higher SS values than the conventional NSFET when N_{it} exceeds 10^{11} cm^{-2}. Therefore, the utilization of alternative high-k dielectrics for the core insulating layer may contribute to higher N_{it} levels, potentially degrading the performance of C-NSFETs.

Conclusions

In this study, we comprehensively evaluated the C-NSFET, focusing on its enhanced performance and immunity against D2D variations. The C-NSFET exhibited superior gate electrostatic control, as evidenced by a steeper subthreshold slope and reduced off-current, ensuring improved short-channel effect prevention. Additionally, the C-NSFET exhibits notable resilience to D2D variability, where the minimized impact of the RDF and stability

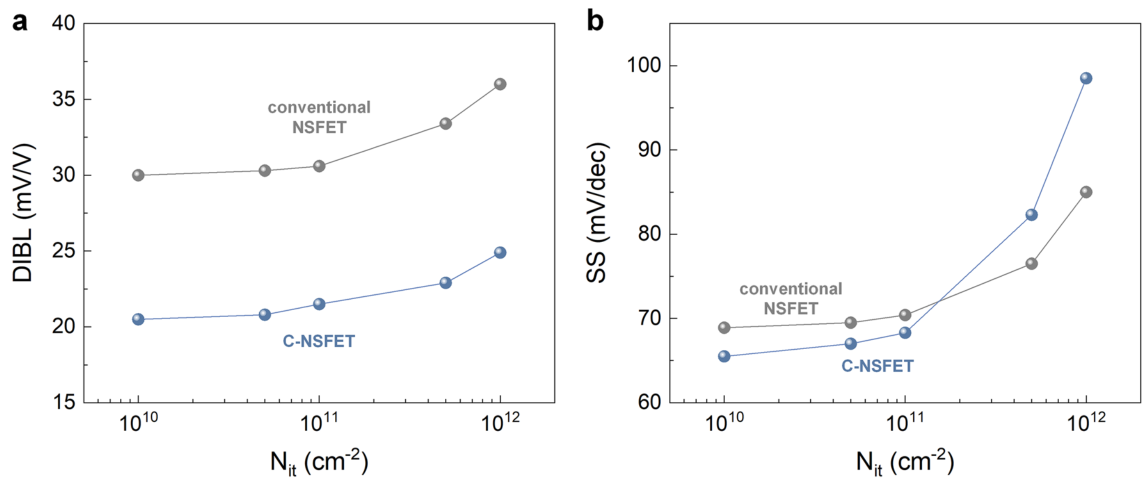

Figure 5. Effects of interface traps. (**a**) DIBL and (**b**) SS characteristics in both devices, as a function of N_{it}.

against nanosheet thickness variations are pivotal in ensuring consistent device performance. Additionally, the strategic use of thermal oxidation to form a core-insulating layer effectively controls the N_{it}. Despite the inherent increase in N_{it} owing to the additional interfaces in the C-NSFET structure, this does not significantly degrade the device performance, especially when compared with conventional NSFETs. Therefore, the C-NSFET has emerged not only as a feasible but also as a superior alternative for next-generation semiconductor device technologies, offering a combination of enhanced performance and reduced variability, which are essential for progression beyond the 5 nm technology node.

Data availability

The datasets used and/or analyzed during the current study available from the corresponding author on reasonable request.

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Author contributions

D.S., H.L., and H.K. developed the simulation model. D.S. and H.L. conducted numerical simulations and analyze the results. J.-H.A. supports the data analysis. S.K. wrote the manuscript based on the obtained data and supervised the project.

Competing interests

The authors declare no competing interests.

Additional information

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