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## Extendable high gain low current/high pulse modified quadratic–SEPIC converter for water treatment applications

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Substantial attention has been drawn over the past few years by high step-up dc-dc converters owing to their applications in a wide range. Apart from renewable energy applications, high voltage/ high pulse converters are efficiently used in water treatment applications. The converter suggested a combination of Quadratic and SEPIC converters with a diode-capacitor cell. This topology generates high-voltage repetitive pulses with a single semiconductor switch and reduced component count. The stress across the components is less than the high-gain converters reported in the literature. The topology has an extendable feature by increasing the number of diode-capacitor cells without affecting the stress. The superiority of the high pulse generating topology is validated with a similar converter in the literature. This paper discusses the nL5 simulator results for the proposed rated topology required for water treatment. A scaled-down 50 W prototype is tested for various input voltages to generate high voltage pulse, and the analytical study is validated.

**Keywords** Water treatment, High voltage pulse, High gain, Multiplier cell, HPSQB

### Abbreviations

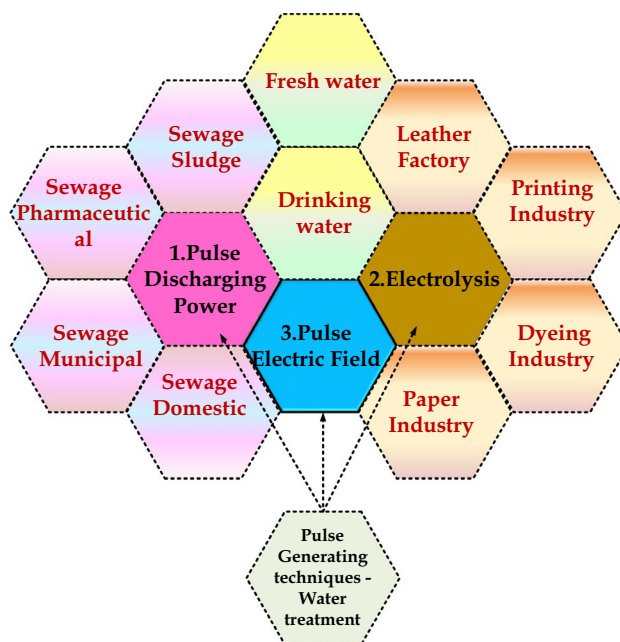
$G_V$	Voltage gain
$G_I$	Current gain
$M$	Number of Multiplier cell
CDVM	Capacitor–diode voltage multiplier
PEF	Pulsed Electric Field
PFN	Pulse Forming Network
$D$	Duty Cycle
$V_g$	Input voltage
$V_o$	Output voltage
$V_{Gate}$	Gate pulse
$V_C$	Capacitor voltage
$V_L$	Inductor voltage
$R_L$	Internal resistance of the inductor
$R_O$	Load resistance
CCM	Continuous conduction mode
HPSQB	High pulse SEPIC–Quadratic Boost

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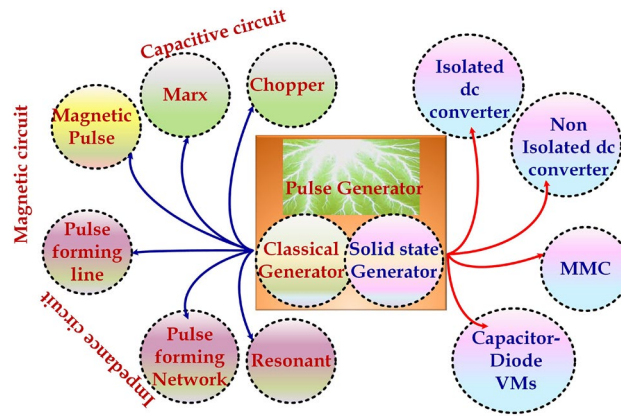
The necessity for water treatment is increasing due to various reasons like water pollution, climatic changes resulting from global warming, drinking water shortage, mainly due to the growing population, etc. Water treatment is crucial in protecting the terrestrial environment from contaminated water from industrial chemicals. The common methods for elimination of microbial contamination in water are chemical treatment<sup>1–4</sup>, application of intense heat<sup>5</sup>, filtration by UV<sup>6,7</sup>, electro dialysis<sup>8</sup> and reverse osmosis process<sup>9</sup>. Conventional water treatment techniques have harmful chemical by-products during their processing. The appropriate solution to overcome the demerits of old water treatment techniques is the implementation of power electronic pulse generators, which can be used effectually for bacterial decontamination in water treatment applications. Three key water treatment techniques are involved: Electrolysis, Pulse discharging power technique and Pulse Electric field technique. The electrolysis technique used in wastewater treatment is based on the electrochemical reaction. Pulsed electric field techniques with high-voltage pulses are used to sterilize drinking water. Pulse discharge water treatment is utilized for sewage water treatment. The applications of these techniques in various water treatment sectors are illustrated in Fig. 1.

High gain conversion is generally achieved by increasing the multiplier cell stages. Topologies discussed in the literature include a modular bipolar high-voltage pulse generator capable of generating bipolar pulses with high voltage and output flexibility<sup>10–13</sup>. A two-stage high-voltage pulse generator converter topology with key features like scalability, modularity, and redundancy is used for electroporation applications is discussed<sup>14</sup>. Sequential pulse generators producing repetitive pulses were discussed as suitable for disinfection applications<sup>15</sup>. Pulsed Electric Field (PEF) method has had promising applications in several fields in the last few years. Pathogenic bacteria and other antibiotic-resistant microorganisms are treated with the high pulse of the electric field. For water treatment applications, pulsed arc discharge and underwater pulsed streamer corona discharge are the two main types of Pulsed Electric Field (PEF) treatments<sup>16,17</sup>. The effect of microorganisms and their removal by comparing the two methods is presented in<sup>17</sup>. It is also observed from the literature that the underwater pulsed streamer corona discharge requires lesser power compared to pulsed arc discharge. The application of bipolar pulses is even more effective compared to its counterpart. Even though electroporation successfully applies pulsed electric fields, permanent cell membrane damage is caused by the electric voltage of very high<sup>18–20</sup>. Generally, the pulse generation for water treatment based on power electronic switches can be classified into two types precisely classical and solid-state pulse generation methodology. Different pulse generation methodologies are depicted in Fig. 2. The Chopper and Marx circuits generate pulses with capacitor storage in classical methods. In Magnetic Pulse Compressor (MPC), a storage capacitor and a magnetic switch is employed for pulse generation. PFL is a crucial method to generate high-power short pulses of the nanoseconds pulse width. For generating rectangular pulses with a pulse width greater than 500 ns, PFL is unsuitable; therefore, Pulse Forming Network (PFN) is used. Small and medium power pulses are generated in a dual resonant Tesla transformer circuit.

In solid-state pulse generation methodology, solid-state switches generate definite pulses. DC-DC isolated and non-isolated converters generate high-voltage pulses with single or multiple controls. This methodology can be used wherever high-voltage pulses are required in water treatment applications. Capacitor–diode voltage multipliers (CDVMs) are also used in electric pulse generators which are highly reliable, efficient, lightweight, and smaller in size<sup>19</sup>. However, they pose a risk of increasing voltage ripples of capacitors and falling output pulse frequency. Low pulsed dc voltages effectively deactivating microbes generally found diffused in water from dead animals



**Figure 1.** Water treatment techniques.



**Figure 2.** Pulse generation methodologies.

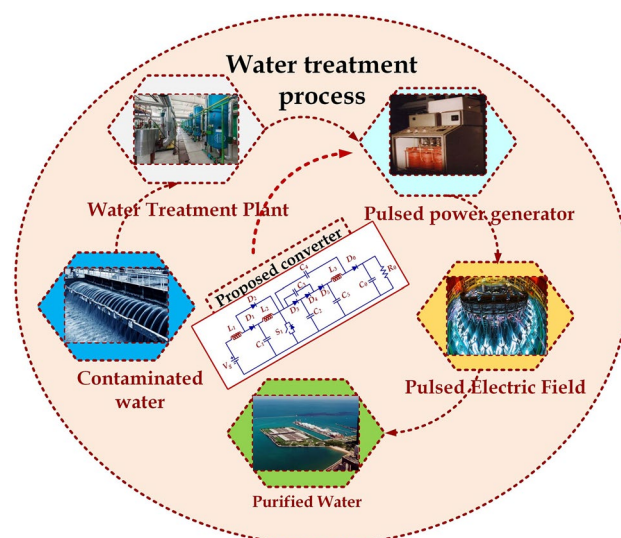
is discussed in<sup>21–23</sup>. *Taphylococcus aureus* is deactivated with 50–80 V pulses for 5 min for 3 days<sup>21</sup> followed by *pichia rhodanensis* with 400–500 V pulses<sup>22</sup> and *pseudomonas aeruginosa* with 500 V pulses for 100  $\mu$ s<sup>23</sup>.

An adjustable pulse magnitude, pulse width and pulse count electric pulse generator are validated with PSIM simulation for 1.5 kV to produce unipolar and bipolar pulses leading to longevity and reliability<sup>24</sup>. Apart from voltage source topology, a current source topology is made with a series-connected Bi-MOSFET switch. A repetitive pulse or single pulse is produced as desired and the current controls the voltage magnitudes of the output pulses through the inductor in every discharge cycle of the load<sup>25</sup>. A state-space model is derived for another continuous inductor current operation mode and results are validated with a 50W prototype<sup>26</sup>. A 10 kV and 1 kW prototype experimental results were presented for a solid-state pulse power modulator for producing short pulses with high switching speed using a new gate driving circuit<sup>27</sup>. The role of the pulsed electric field in the water treatment process is illustrated with a flow diagram in Fig. 3. Based on the challenges addressed in the literature<sup>28–36</sup>, the following topology is proposed in this paper.

In this paper, a novel high-voltage pulse generator based on Quadratic and SEPIC dc converters in combination with multiple diode-capacitor cell is proposed. The derived high pulse generator affords the following features:

- (i) Single switch topology
- (ii) Extendable feature
- (iii) Lesser component count.

Despite these advantages, the suggested high-pulse generator requires a high-voltage switch to chop the continuous dc voltage to a high-voltage pulse. However, this issue can be overcome by using a series-connected switch. The major contributions of the article are.



**Figure 3.** Block diagram of water treatment application.

- Proposed novel single switch topology with extendable features.
- Reliability analysis of proposed topology is performed by considering annual mission profile of the water treatment plant and compared with similar topology in the literature.
- With the process parameters, water sample is tested before and after treatment and the presence of microbes are analyzed.
- Sample is tested with 360 V and 5000 V to observe the significance of the magnitude of pulsed voltage.

This paper is organized as follows: Following the introduction, a description of the proposed topology is presented in Section "Proposed repetitive high pulse generating topology". The design of the derived topology with the voltage stress across the components is illustrated in Section "Design and component analysis". The superiority of the suggested converter is highlighted by comparing it with a similar topology in the literature in Section "Performance analysis". Simulation results are presented in Section "Comparative Study" by using nL5 software. The scaled-down prototype is tested and the results are depicted in Section "Simulation results". Finally, the article is concluded in the last section.

### Proposed repetitive high pulse generating topology

This section performs the derivation, operating principle, and steady-state analysis of the topology. The operating principle is discussed with a single diode-capacitor cell for simplicity.

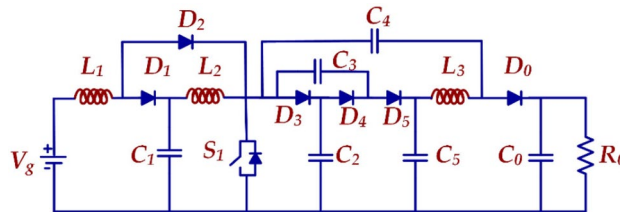
### High pulse modified SEPIC-quadratic boost DC converter

The schematic circuit of the HPSQB converter is presented in Fig. 4. The converter's gain increases by proportionately increasing the voltage multiplier stages.

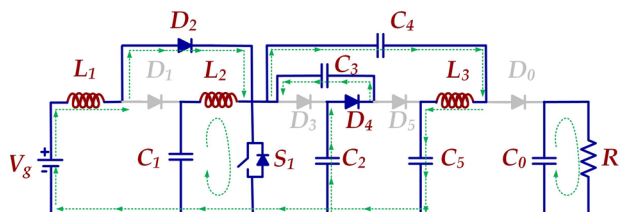
### Operating principle

Based on the conducting and non-conducting conditions of the semiconductor switch, the working of the converter is divided into two modes.

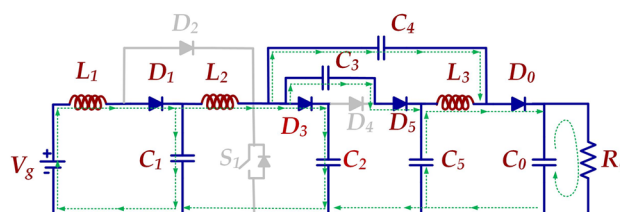
*Mode-I:* Fig. 5a depicts the equivalent circuit of the proposed topology in the ON mode of the switch. In Fig. 5a, the Mode-I is from 0 to DTs, representing the duty cycle as 'D' and the switching period as Ts. The switch is in 'ON' condition in this mode. During this mode, the input supply,  $V_g$ , charges the inductor 'L1' and forms a closed circuit with diode D2 while diode D1 is not conducting. Inductor L2 is charged from the capacitor C1. The non-conducting state of the diodes D3 and D5 and conducting state of diode D4 connects the capacitors C2



**Figure 4.** High pulse modified Sepic- Quadratic Boost dc-dc converter.



(a)



(b)

**Figure 5.** Operating principle (a) Mode-I (b) Mode-II.

and  $C_3$  in series and capacitors  $C_4$  and  $C_5$  in series. The series combination of  $C_2$ ,  $C_3$  and  $C_4$ ,  $C_5$  branches falls in parallel with each other and forms a closed circuit. The load at this condition is fed from the output capacitor ' $C_0$ '. Diodes  $D_1$ ,  $D_3$ ,  $D_5$ , and  $D_0$  are in a non-conducting state during this mode. The key waveforms of the HPSQB converter are also depicted in Fig. 6.  $V_{pulse}$  is the voltage obtained after the high voltage switch which is used to chop the output voltage of the converter.

**Mode-II:** As given in Fig. 5b. The Mode-II is from  $D_T$ s to  $T_s$ . In this mode, the inductors  $L_1$  and  $L_2$  discharges to the load along with the input supply  $V_g$ . Diodes  $D_2$  and  $D_4$  are in blocking state and diodes  $D_2$ ,  $D_3$ ,  $D_5$  and  $D_0$  moves into conduction state. The output voltage in this mode is equal to  $V_{C5} + V_{C4} - V_{C3}$ .

**Steady-state analysis in CCM**

The voltage gain of the proposed converter is derived mathematically by applying the magnetic flux principle on charging and discharging state of the inductor. Considering the internal resistance of the proposed converter as zero or negligible. Table 1 presents the voltage expression of the inductor in ON and OFF modes. The derivation of the voltage gain is derived as follows:

On application of the volt-sec balance principle, the voltage gain of the proposed converter is thus derived as,

$$G_V = \frac{V_O}{V_g} = \frac{(2 + D)}{[1 - D]^2} \tag{1}$$

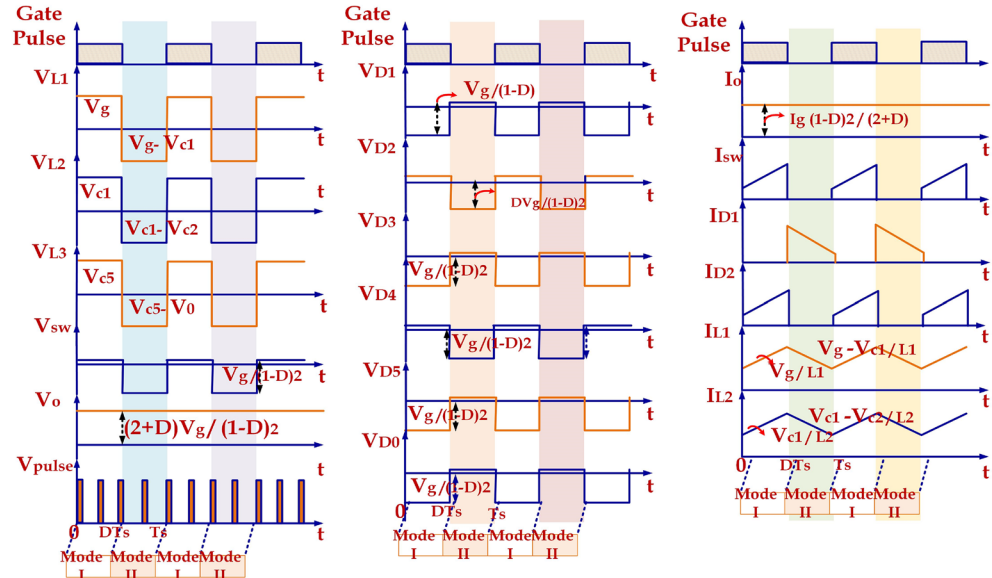
The generalized expression of the converter proposed with 'M' number of multiplier stages is given as,

$$G_V = \frac{V_O}{V_g} = \frac{M(2 + D)}{[1 - D]^2} \tag{2}$$

The current gain of the converter proposed is obtained as,

$$\frac{I_O}{I_g} = \frac{[1 - D]^2}{(2 + D)} \tag{3}$$

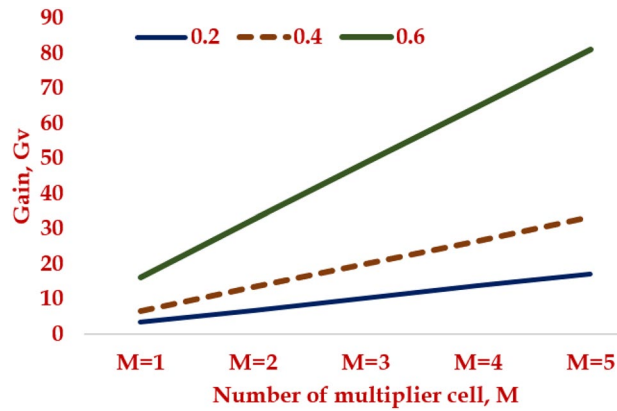
The variation of voltage gain,  $G_v$  with the multiplier cell,  $M$  is presented in Fig. 7 for  $M = 1$  to 5.



**Figure 6.** Key waveforms of the proposed topology.

ON state	OFF state
$V_{L1} = V_{Cg}$	$V_{L1} = V_g - V_{C1}$
$V_{L2} = V_{C1}$	$V_{L2} = V_{C1} - V_{C2}$
$V_{L3} = V_{C5} - V_{C4}$	$V_{L3} = V_{C5} - V_O$

**Table 1.** Voltage expression of the inductor.



**Figure 7.** Gain of the HPSQB topology with increase in multiplier cell, M.

### Design and component analysis

This section elaborates on the steps to design the proposed high-pulse generator. Since the required pulse for the water treatment application is observed to be in kV. Accordingly, the passive components of the converter are acquired. The stress across the topology components is also analyzed and presented to highlight the advantage of the derived topology.

#### Design of passive components

The design expression of the inductors ( $L_1$ ,  $L_2$  and  $L_3$ ) in the proposed topology (number of multiplier cell,  $M = 1$ ) is

$$L_1 = \frac{R_O(1-D)^4 D}{2(2+D)^2 f_s} \quad (4)$$

$$L_2 = \frac{R_O(1-D)^2 D}{2(2+D)^2 f_s} \quad (5)$$

$$L_3 = \frac{R_O(1-D) D}{2(2+D) f_s} \quad (6)$$

The capacitor ( $C_1$ ,  $C_2$ ,  $C_3$ ,  $C_4$ ,  $C_5$  and  $C_O$ ) formula

$$C_1 = \frac{(2+D) D I_O}{f_s(1-D) \Delta[V_g/(1-D)]} \quad (7)$$

$$C_2 = C_3 = \frac{I_O(1-D)}{f_s \Delta[V_g/(1-D)^2]} \quad (8)$$

$$C_4 = \frac{I_O D}{f_s \Delta[V_g(1+D)/(1-D)^2]} \quad (9)$$

$$C_5 = \frac{I_O D}{f_s \Delta[2V_g/(1-D)^2]} \quad (10)$$

$$C_O = \frac{I_O}{f_s \Delta[(2+D)V_g/(1-D)^2]} \quad (11)$$

#### Stress across the components

The voltage and current stress of the passive and semiconductor components are derived from the steady-state analysis for designing the converter. Table 2 illustrates the voltage stress across the semiconductor devices for a different number of multiplier cells, M. From this Table, it is observed that the stress across the components is independent of the number of multiplier cells. The increase in the M number of multiplier cells does not affect the stress value.

Number of multiplier cell	Voltage gain	Voltage stress on switch in terms of $V_g$	Voltage stress on Diode D1	Voltage stress on Diode D2	Voltage stress on Diode D3 and D4	Voltage stress on Diode D5	Voltage stress on Diode Do
1	$\frac{(2+D)}{[1-D]^2}$	$\frac{V_g}{[1-D]^2}$	$\frac{V_g}{[1-D]}$	$\frac{V_g D}{[1-D]^2}$	$\frac{V_g}{[1-D]^2}$	$\frac{V_g}{[1-D]^2}$	$\frac{V_g}{[1-D]^2}$
2	$\frac{2(2+D)}{[1-D]^2}$						
3	$\frac{3(2+D)}{[1-D]^2}$						
n	$\frac{M(2+D)}{[1-D]^2}$						

**Table 2.** Voltage expression of the inductor.

### Stress across the capacitors

Pulsed electric field application mainly depends on charging and discharging the capacitors in the converter. The voltage stress across the capacitors  $C_1, C_2, C_3, C_4, C_5$  and  $C_0$  is

$$V_{C1} = \frac{V_g}{[1-D]} \tag{12}$$

$$V_{C2} = V_{C3} = \frac{V_g}{[1-D]^2} \tag{13}$$

$$V_{C4} = \frac{V_g(1+D)}{[1-D]^2} \tag{14}$$

$$V_{C5} = \frac{2V_g}{[1-D]^2} \tag{15}$$

### Current stress of the components

The RMS current through the inductor is given as

$$I_{L1} = \frac{I_O(2+D)}{[1-D]^2} \tag{16}$$

$$I_{L2} = \frac{I_O(2+D)}{1-D} \tag{17}$$

$$I_{LO} = I_O \tag{18}$$

The RMS current through the switch,  $S_1$  is given as

$$I_{S1} = \frac{I_O[4-D^2]\sqrt{D}}{[1-D]^2} \tag{19}$$

### Performance analysis

#### Efficiency analysis

Figure 8 presents the equivalent circuit of the HPSQB converter for efficiency analysis. For efficiency calculation of the proposed converter, the parasitic resistance of components is considered as shown in the equivalent circuit and the equations as follows:

$$P_s = I_{s(rms)}^2 R_{ds(on)} \tag{20}$$

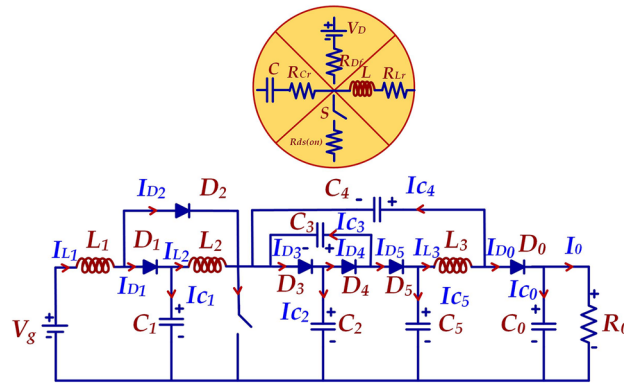
$$P_{D1} = [V_F(i_{D1(avg)} + i_{D2(avg)} + i_{D3(avg)} + i_{D4(avg)} + i_{D5(avg)}) + V_F i_{D0(avg)}] \tag{21}$$

$$P_{D2} = R_f [i_{D1(rms)}^2 + i_{D2(rms)}^2 + i_{D3(rms)}^2 + i_{D4(rms)}^2 + i_{D5(rms)}^2] + R_F i_{D0(rms)}^2 \tag{22}$$

$$P_D = P_{D1} + P_{D2} \tag{23}$$

$$P_L = I_{L1(rms)}^2 r_{L1} + I_{L2(rms)}^2 r_{L2} + I_{L3(rms)}^2 r_{L3} \tag{24}$$

$$P_C = I_{C1(rms)}^2 r_{C1} + I_{C2(rms)}^2 r_{C2} + I_{C3(rms)}^2 r_{C3} + I_{C4(rms)}^2 r_{C4} + I_{C5(rms)}^2 r_{C5} + I_{C0(rms)}^2 r_{C0} \tag{25}$$



**Figure 8.** Equivalent circuit of the HPSQB topology.

The power rating of HPSQB converter is considered as 500 W. The input and output voltage are chosen as 300 V and 35.1 kV respectively as mentioned in simulation section.

Table 3 presents the specification considered for the efficiency study of the HPSQB converter. With (20–25), the losses across the converter components are obtained and the efficiency analysis is performed. Efficiency analysis is performed for the specification, as shown in Table 3, similar to the simulation study. The average and RMS current few diodes in the topology are given in Table 4, along with the losses in the components. Similarly, the capacitor loss is also performed and the total loss is observed to be 67 W. With this loss, the efficiency of the HPSQB topology is calculated as 87%.

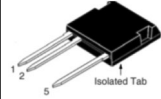



### Sensitivity analysis

Sensitivity analysis is recommended in designing a novel converter because it portrays the sensitivity of voltage gain for the change in D, duty cycle, and RL, the internal resistance of the inductor. The efficiency of the topology is

$$\eta = G_V G_I \tag{26}$$

$$G_V = \frac{\eta(2 + D)}{(1 - D)^2} \tag{27}$$

The voltage conversion ratio of the HPSQB topology with the  $R_L$  of inductor is

Parameters	Rating	Type/model
Power	500 W	-
Duty cycle	0.61	
Switching frequency	50 kHz	
Switch	2 kV/5 A $R_{ds(on)} = 4.2 \Omega$	IXTF6N200P3 
Diode	3.3 kV/10 A $V_f = 1.5 \text{ V}/R_f = 0.3 \Omega$	GB05MPS33-263 
Inductor	10 mH $R_L = 165 \text{ m}\Omega$	
Capacitor	1 $\mu\text{F}/2.5 \text{ kV}$	

**Table 3.** Specification considered for efficiency analysis.



Components	Expression	Loss	Total loss
Switch	$I_{S1(rms)} = \frac{I_O[4-D^2]\sqrt{D}}{[1-D]^2}$	$P_{sw(cond)} = 46\text{ W}$ $P_{sw( switching)} = 13\text{ W}$	59 W
Diode	$I_{D1( avg)} = \frac{I_O(2+D)}{1-D}$	$P_{D1} = 1.29\text{ W}$ $P_{D2} = 2.02\text{ W}$	3.6 W
	$I_{D2( avg)} = \frac{I_O(2+D)D}{[1-D]^2}$	⋮	
	$I_{D1( rms)} = \frac{I_O(2+D)(\sqrt{1-D})}{[1-D]^2}$	$P_{D0} = 0.1\text{ W}$	
	$I_{D2( rms)} = \frac{I_O(2+D)(\sqrt{D})}{[1-D]^2}$		
Inductor	$I_{L1} = \frac{I_O(2+D)}{[1-D]^2}$	$P_{L1} = 3.23\text{ W}$ $P_{L2} = 0.069\text{ W}$	3.3 W
	$I_{L2} = \frac{I_O(2+D)}{1-D}$	$P_{L3} = 0.01\text{ W}$	
	$I_{LO} = I_O$		

**Table 4.** Losses across the components.

$$G_V = \frac{(2 + D)}{(1 - D)^2 \left[ 1 + \frac{(2+D)^2 R_{L1}}{R_O(1-D)^4} + \frac{(2+D)^2 R_{L2}}{R_O(1-D)^2} + \frac{R_{L3}}{R_O} \right]} \tag{28}$$

The voltage conversion ratio is simplified by considering same internal resistance for all the inductor ( $R_{L1} = R_{L2} = R_{L3}$ )

$$G_V = \frac{R_O(2 + D)(1 - D)^2}{R_O(1 - D)^4 + (5 - 2D)^2 R_L} \tag{29}$$

Sensitivity analysis of voltage gain is accomplished by differentiating (29) with respect to D. After mathematical manipulation, the final yielded equation is

$$\frac{dG_V}{dD} = \frac{[R_O(1 - D)^4 + (5 - 2D)^2 R_L][3D^2 - 3] + [R_O(2 + D)(1 - D)^2][4R_O(1 - D)^3 + (10 - 4D)R_L]}{[R_O(1 - D)^4 + (5 - 2D)^2 R_L]^2} \tag{30}$$

Similarly, the sensitivity of the output voltage with respect to D is

$$\frac{dV_O}{dD} = \frac{3[D^2 - 1]}{(1 - D)^4} \tag{31}$$

The sensitivity analysis of voltage gain and output voltage for duty cycle D is performed and depicted in Fig. 9a,b. It is depicted in Fig. 9a that the variation of the non-ideal voltage gain of the HPSQB converter for a higher duty cycle is significant for the internal resistance of the inductor, RL. Similarly, the variation of ideal voltage gain for duty cycle D is predominant for the duty cycle greater than 0.5, which is illustrated in Fig. 9b.

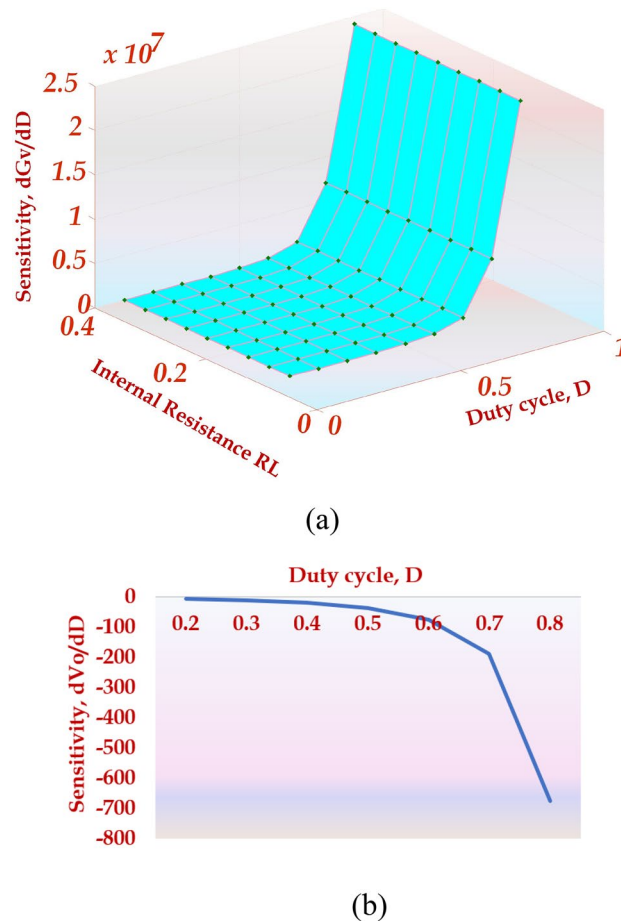
**Reliability analysis**

This section determines the failure rate based on the equations given in Fig. 10a. The military handbook calculates the failure rate in many applications to determine reliability. Accurate reliability predictions are essential in applications that depend on various parameters, such as the physical and operating characteristics of the converter and its environment. The reliability analysis of HPSQB topology determined that the semiconductor devices are failure prone compared to the passive components. Therefore, the failure rate of the switch and diodes are discussed and depicted in Fig. 10b. The failure rate of the switch is estimated to be greater than the diodes in the converter circuit considered.

The reliability analysis is extended by considering the annual mission profile of the water treatment plant in Chennai, Tamil Nadu and it is presented in Table 5. This analysis is validated by comparing the MTTF computation of Proposed HPSQB converter with the pulsed voltage converter proposed in<sup>19</sup>. Table 6 depicts the comparison performed in the MTTF calculation of HPSQB converter with the converter in<sup>19</sup>. From this comparative study, it is observed that HPSQB converter’s reliability is better compared to the topology presented in<sup>19</sup>.

**Comparative Study**

This section compares the topology with similar topologies in the literature and proves its superiority. First, the derived topology is compared with the voltage multiplier-based topology suggested for water treatment applications<sup>19</sup>. Figure 11a–d presents the comparison made on the derived topology with the topology in<sup>19</sup>. In Fig. 11a,b, the duty cycle is kept constant at 0.5 and the number of multiplier cells, M and the total component



**Figure 9.** Sensitivity analysis of HPSQB topology (a)  $dG_v/dD$  (b)  $dV_o/dD$ .

count is analyzed for various values of Gain,  $G_v$ . The comparative Table 7 shows that the proposed converter uses lesser components to achieve the same voltage gain as compared to the converter in<sup>19</sup>. In Fig. 11c, the total component count is kept constant at 16 and the duty cycle is compared for various values of Gain,  $G_v$ .

It is noted that the suggested topology requires a low duty cycle,  $D$ , to achieve the required voltage gain compared to the converter chosen for comparison<sup>19</sup>, which ultimately reduces the conduction losses of the semiconductor losses and increases the efficiency of the converter. Next, the required input voltage to achieve the desired output voltage is compared by setting the duty cycle to 0.5 and fixing the total component count as 16. This study depicts in Fig. 11d that the derived topology requires lesser input voltage,  $V_g$ , compared to the topology in<sup>19</sup> for various output voltages,  $V_o$ . Since the losses across the power semiconductor devices are more compared to the passive component's losses, the HPSQB topology offers better efficiency compared to<sup>19</sup>. It is observed that to achieve the voltage gain of 10, the number of semiconductor devices required for<sup>19</sup> is 10 whereas the proposed topology is 7.

Finally, the comparative study is extended by choosing similar topologies with diode-capacitor cell and extendable capability. Figure 11e illustrates the analysis carried out and it shows that the derived topology exhibits high gain compared to other topologies. The gain expression and the component breakup are depicted in Table 8. Furthermore, topologies in literature are extended to derive the high voltage pulses in bipolar mode<sup>30</sup>. This bipolar pulse generation is extended as a future scope with the suggested topology.

### Simulation results

The proposed topology is simulated with a 500 W power rating for generating a high voltage pulse of 5 kV. The specification of the derived topology is depicted in Table 9. The load resistance for the simulation study is obtained based on the dimension considered for analysis. The area of the plate and the distance between the plates are chosen as 1 cm and 1 cm, respectively. Considering the conductivity of water as 20  $\mu\text{s/cm}$ , the equivalent resistance of the water sample is calculated as 50 k $\Omega$ . Figure 12a–e presents the simulation result obtained from the nL5 simulator.

Figure 12a depicts the output and switch voltage before the pulse forming unit for 300 V input voltage. The voltage stress across the switch is validated with the analytical study,  $V_{sw} = V_g/(1-D)^2 = 1.9$  kV. Similarly, the output voltage for  $M = 1$  and  $D = 0.5$  is  $(2 + D)/(1-D)^2 = 5.1$  kV. The diode voltage is obtained and illustrated in Fig. 12b. The voltage across diode D2 is  $V_g(1-D) = 0.8$  kV. The voltage across diodes D3 and D4 is  $V_g/(1-D)^2 = 1.9$  kV, which is presented in Fig. 12b,c. The capacitor voltage is presented in Fig. 12d. Finally, the output

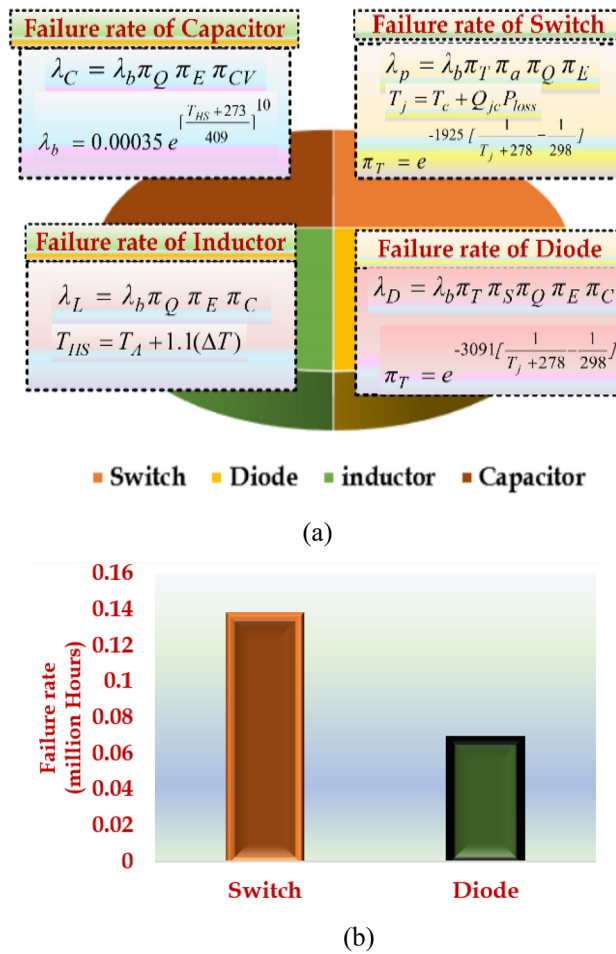


Figure 10. Parameters related to failure rate calculation.

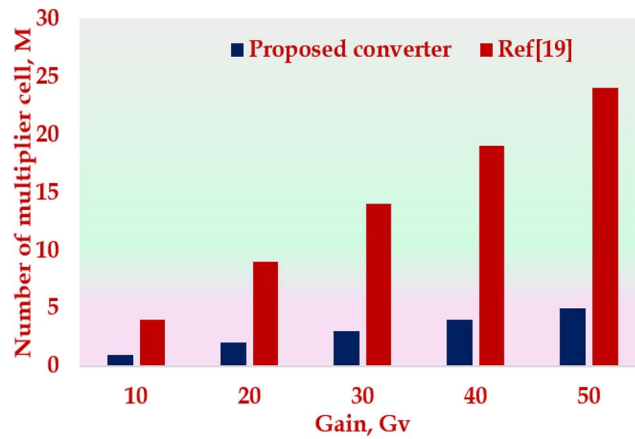
Condition	Time (hrs)	On/Off	Ambient Temperature (°C)	Relative Humidity %	ΔT (°C)	Number of Cycles per year	Duration of Cycles (hrs)	Maximum temperature during cycling (°C)
Day/On	3600	On	40	50	15	300	12	45
Day/Off	780	Off	35	35	10	65	12	40
Night/Off	4380	Off	30	40	5	365	12	35

Table 5. Annual mission profile of water treatment plant.

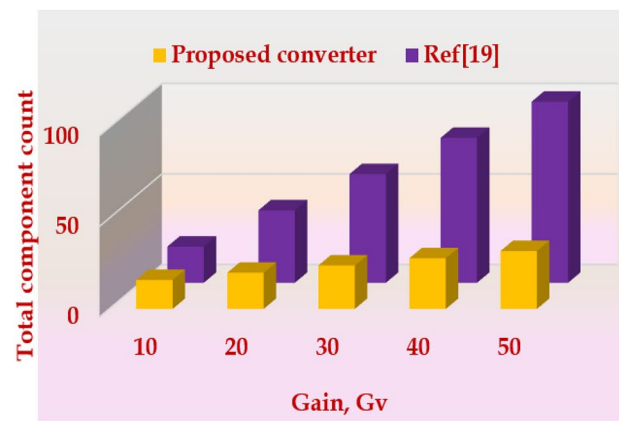
Component failure rate	Proposed HPSQB converter	Converter in Ref <sup>19</sup>
$\lambda_s$	$2.24 \times 10^{-6}$	$2.32 \times 10^{-6}$
$\lambda_D$	$3.49 \times 10^{-6}$	$5.43 \times 10^{-6}$
$\lambda_C$	$0.0002 \times 10^{-6}$	$0.009 \times 10^{-6}$
$\lambda_L$	$0.82 \times 10^{-6}$	$0.022 \times 10^{-6}$
Mean time to failure (MTTF)	17.44Years	14.67Years

Table 6. MTTF computation.

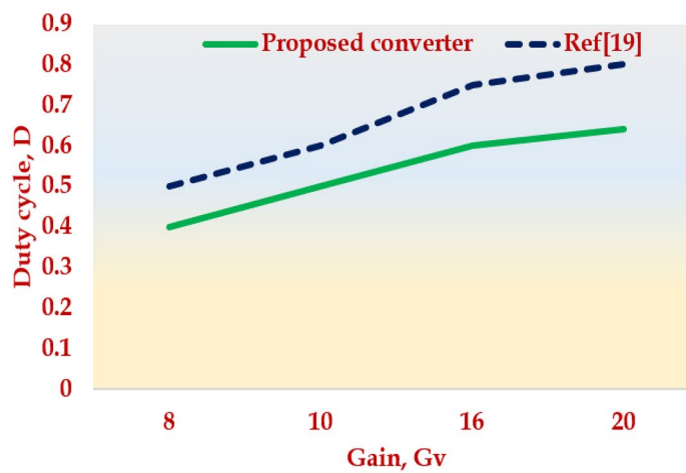
high pulse is obtained after incorporating pulse forming unit. The acquired high voltage pulse of 5 kV is depicted in Fig. 12e. The switching frequency of the switch added in pulse forming unit is 500 Hz and the duty cycle is 10%. This is validated in Fig. 12e with the pulse width of 20 μs and the time period of 2 ms. The diode voltage is obtained and illustrated in Fig. 12b. The voltage across diode D<sub>2</sub> is Vg(1-D) = 0.8 kV. The Voltage across diodes D<sub>3</sub> and D<sub>4</sub> is Vg/(1-D)<sup>2</sup> = 1.9 kV which are presented in Fig. 12b,c. The capacitor voltage is presented in Fig. 12d.



(a)



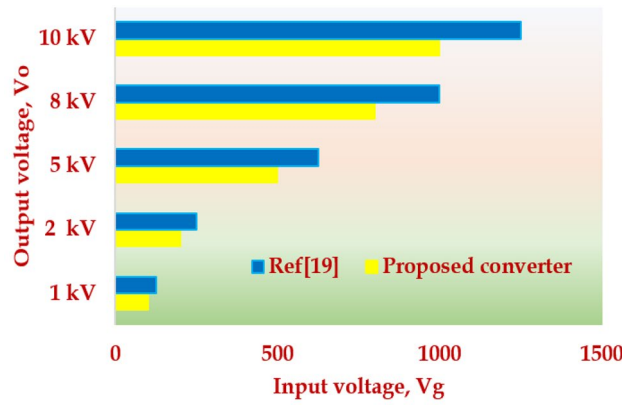
(b)



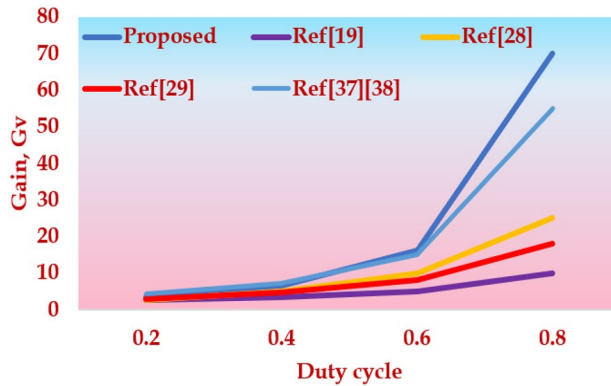
(c)

**Figure 11.** Key highlights of the HPSQB topology (a) Gain versus voltage multiplier cell (b) Gain versus total component count (c) Gain versus duty cycle (d) Input versus output voltage (e) Gain comparison with similar topologies in literature.

Finally, the output high pulse is obtained after incorporating pulse forming unit. The acquired high voltage pulse of 5 kV is depicted in Fig. 12e. The switching frequency of the switch added in pulse forming unit is 500 Hz and the duty cycle is 10%. This is validated in Fig. 12e with the pulse width of 20  $\mu$ s and the time period of 2 ms.



(d)



(e)

Figure 11. (continued)

Parameters	Topology	Duty cycle, $D = 0.5$				
		Gain, $G_v$				
		10	20	30	40	50
Number of Multiplier cell, $M$	Proposed converter	1	2	3	4	5
	Ref <sup>19</sup>	4	9	14	19	24
Total component count	Proposed converter	16	20	24	28	32
	Ref <sup>19</sup>	20	40	60	80	100
Parameters	Topology	Total component count = 16				
		Gain, $G_v$				
		8	10	16	20	
Duty cycle, $D$	Proposed converter	0.4	0.5	0.6	0.64	
	Ref <sup>19</sup>	0.5	0.6	0.75	0.8	
Parameters	Topology	Total component count = 16, Duty cycle = 0.5				
		Output voltage, $V_o$ (kV)				
		1	2	5	10	
Input voltage, $V_g$ (V)	Proposed converter	100	200	500	1000	
	Ref <sup>19</sup>	125	200	625	1250	

Table 7. Comparative study of the HPSQB topology with ref<sup>19</sup>.

### Experimental results

The proposed converter is tested for 50 W power rating to validate the theoretical analysis carried out. The specification of the topology is presented in Table 10. The experimental study is scaled down to 50 W, 300 V for high pulse generation. The photograph of the setup tested is presented in Fig. 13a. The results obtained for the validation are presented in Fig. 13a–m. The input voltage varies from 12 to 36 V to obtain 120 V to 360 V

Topology	Gain	Total component count				Suggested application
		Switch	Diode	Capacitor	Inductor	
Proposed converter	$\frac{M(2+D)}{(1-D)^2}$	1	4 + 2 M	4 + 2 M	3	Water treatment application
Ref <sup>19</sup>	$\frac{M+1}{1-D}$	1	1 + 2 M	1 + 2 M	1	Water treatment application
Ref <sup>23</sup>	$MV_{CM}$	1 + 2 M	1 + M	1 + M	0	Pulsed voltage application
Ref <sup>28</sup>	$\frac{1+(2M+3)D}{1-D}$	2 + M	6 + 5 M	1	4 + 2 M	Low input integrated application
Ref <sup>29</sup>	$\frac{2(1+MD)}{1-D}$	1	3(1 + M)	3	1 + M	Low voltage DC Source Integration
Ref <sup>37</sup>	$\frac{3-D}{(1-D)^2}$	1	6	6	3	Low voltage DC Source Integration
Ref <sup>38</sup>	$\frac{3-D}{(1-D)^2}$	2	4	4	2	Renewable power Source Integration

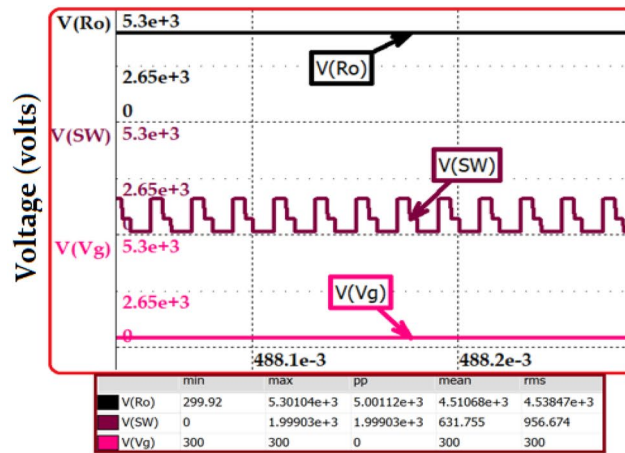
**Table 8.** Comparative study of the HPSQB converter with similar converters in literature.

Parameters	Value
Proposed converter	
Power	500 W
Input voltage	300 V
Duty ratio	0.61
Gain	17 times
Load resistance	50 k $\Omega$
Switching frequency	50 kHz
Inductor L <sub>1</sub> , L <sub>2</sub> and L <sub>3</sub>	5 mH, 20 mH, 100 mH
Capacitor C <sub>1</sub> –C <sub>5</sub> and C <sub>O</sub>	10 $\mu$ F, 1 $\mu$ F
Output voltage	5 kV
Number of multiplier cell	One
Pulse width	200 $\mu$ s
Repetitive rate of the pulses	500 pulses/sec
Load specification	
Distance between the electrode	1 cm
Area of the plate	1 cm <sup>2</sup>
Water conductivity	20 $\mu$ s/cm
Load resistance (water sample)	50 k $\Omega$
Switch to produce pulsed output	
Switching frequency	500 Hz
Duty cycle	1%

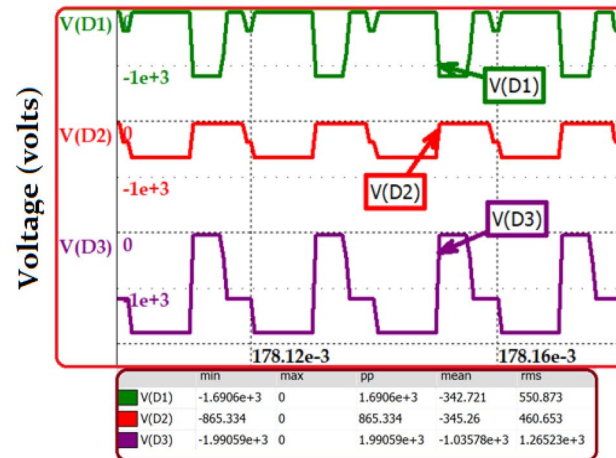
**Table 9.** Simulation Parameters of the HPSQB topology.

results. The input voltage of 12 V, 24 V and 36 V is given to the converter, which is depicted in Fig. 13c,d. The duty cycle is kept constant for 0.5 and is observed in Fig. 13d. The corresponding high pulse generated from the inputs (12 V–36 V) is presented in Fig. 13e–g. The high voltage pulses of 120 V, 240 V and 360 V are presented in Fig. 13e–g, respectively. These output voltages are much suitable for treatment of microbes discussed in<sup>21–23</sup>. The capacitor C<sub>5</sub> voltage (VC<sub>5</sub>) for the input 36 V is presented in Fig. 13h. It validates the steady-state analysis's theoretical result, which represents  $VC_5 = 2Vg/(1-D)^2$ . For 0.5 duty cycle and 36 V input, the capacitor voltage is 288 V which is justified in Fig. 13g. The capacitor C<sub>2</sub> and C<sub>3</sub> voltage (VC<sub>2</sub> and VC<sub>3</sub>) is  $Vg/(1-D)^2$ . This is validated for 24 V input voltage, and the result is presented in Fig. 13i. The voltage stress across the single switch in the suggested topology is observed for the input voltage of 36 V. The theoretical formula for the switch voltage stress is  $Vg/(1-D)^2$ , which is validated in Fig. 13j. The inductor L<sub>2</sub> voltage is presented in Fig. 13k to validate the volt-sec balance principle applied to the topology. Finally, the diode D<sub>1</sub>–D<sub>4</sub> voltages are observed and presented in Fig. 13l–m.

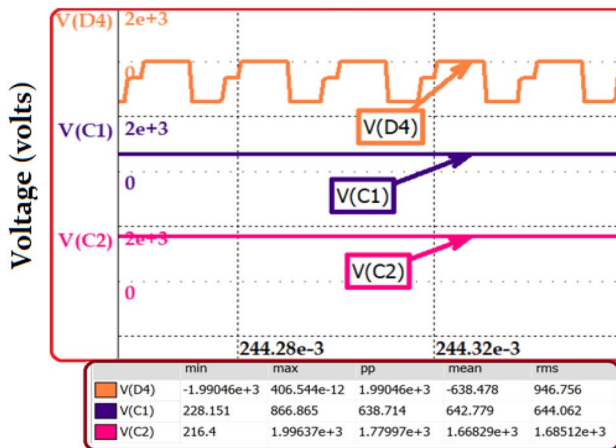
From the above sections, it is noted that the simulation results are obtained for 5 kV output voltage and hardware results are worked for 360 V output voltage. To validate the significance of these magnitude of voltage in water treatment, we planned to take water sample from our kitchen which is supplied from the municipality and decided to go for testing. The specification of the pulsed voltage considered for testing is given in Table 11. Raw water sample and the water samples subjected to 360 V and 5 kV in pulsed electric field chamber are tested in Indian analytical testing Lab, Bangalore. Finally, the obtained result from the lab before and after treatment is presented in Table 12. From the results, it is observed that all the microbes are absent after the treatment with 5 kV. With 360 V output voltage, the Coliform Bacteria is reduced from 10 cfu/gm to 2 cfu/gm whereas other microbes are completely absent.



(a)



(b)

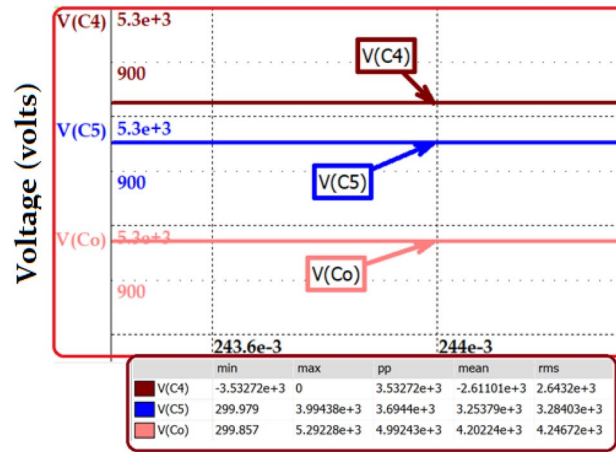


(c)

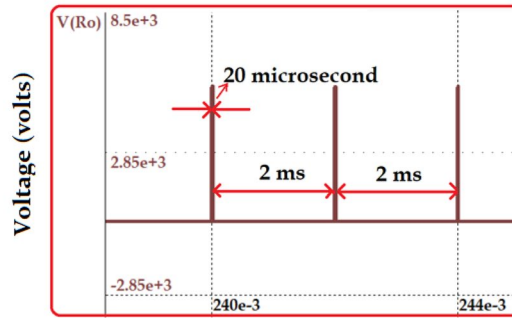
**Figure 12.** Simulation results (a) Output and switch voltage at steady state condition (b) Diode voltage (c) and (d) capacitor voltage (e) High pulse voltage.

### Conclusion

This paper validates the performance of high voltage pulse generating topology derived from quadratic and modified SEPIC converter with voltage multiplier cells for water treatment applications. A wide-ranging analysis of the operating principle and design of the HPSQB converter is conducted. The steady-state performance of the topology is mathematically proven with the test results. The derived topology generates a rectangular unipolar pulse with flexibility in the variation of pulse duration and amplitude. The proposed HPSQB converter has



(d)



(e)

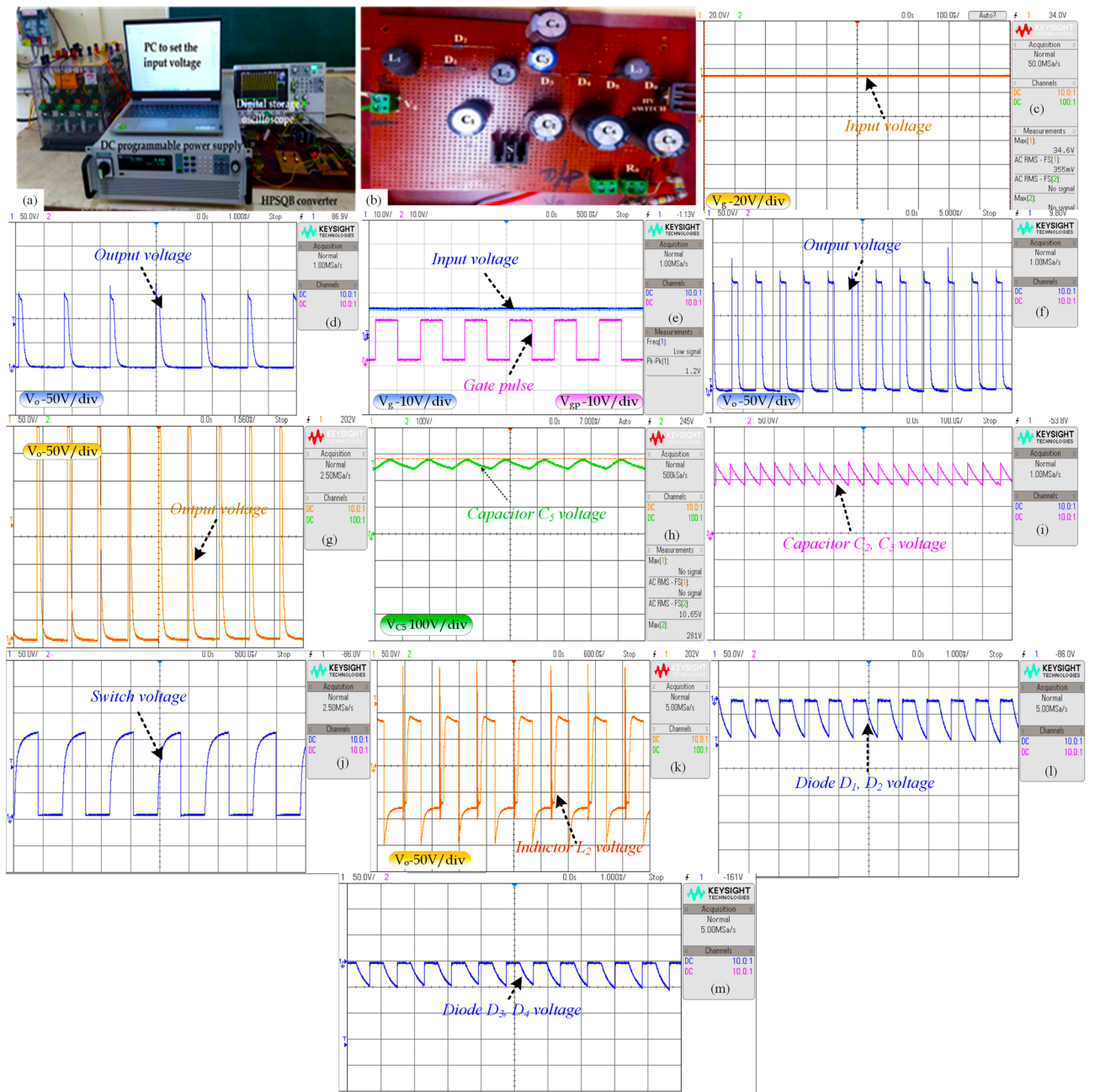
Figure 12. (continued)

Parameters	Value
Proposed converter	
Power	50 W
Input voltage	12 V to 36 V
Duty ratio	0.5
Gain	10 times
Load	1 kΩ
Switching frequency	50 kHz
Output voltage	120 V–360 V
Number of multiplier cell	One
Pulse width	200 μs
Repetitive rate of the pulses	500 pulses/sec
Switch to produce pulsed output	
Switching frequency	500 Hz
Duty cycle	1%

Table 10. Specification of the laboratory HPSQB prototype.

unique features such as (i) high gain is achieved with the lesser component count, (ii) it can be integrated into low voltage input supply even for domestic applications, (iii) more efficient and reliable, (iv) voltage stress across the power semiconductor devices is less. The comparative study indicates that the HPSQB converter requires a lesser component to achieve high voltage gain compared to similar topologies in the literature. The derived topology is extendable and flexible, where the desired gain of the converter is achieved by adjusting the number of multiplier cells,  $M$ . A scaled-down prototype of 50 W, 0.36 kV is tested to validate the analytical studies. Both experimental and simulation studies analyze the generation of the unipolar pulse from the pulse-forming unit. The obtained test results exhibit excellent accordance with theoretical and simulation analysis.





**Figure 13.** Test results (a) Photograph of the setup tested (b) Photograph of the converter (c) 20 V/div-Input voltage,  $V_g$  (d) 10 V/div-Input voltage,  $V_g$  and 10 V/div-Gate pulse,  $V_{gate}$  (e), (f) and (g) 50 V/div-Output voltage,  $V_o$  (h) 100 V/div-Capacitor voltage,  $V_{C5}$  (i) 50 V/div-Capacitor voltage,  $V_{C2}$  and  $V_{C3}$  (j) 50 V/div-Switch voltage,  $V_{SW}$  (k) 50 V/div- Inductor voltage,  $V_{L2}$  (l) 50 V/div-Diode voltage,  $V_{D1}$  and  $V_{D2}$  (m) 50 V/div-Diode voltage,  $V_{D3}$  and  $V_{D4}$ .

Sl.no	Real time treatment conditions	Simulation and prototype obtained pulsed voltages	
		360 V (prototype output)	5 kV (simulation output)
1	Frequency of Pulses	500 Hz	500 Hz
2	Pulse width	168 µs	169 µs
3	Distance between the electrodes	9.87 mm	9.87 mm
4	Current	0.4 A	0.1 A
5	Treatment time	6 min	6 min
6	Type of electrode	Stainless steel	Stainless steel
7	Sample description	Raw water	Raw water
8	Place of collection	Kitchen	Kitchen
9	Treatment temperature	26 °C	29 °C
10	Treatment chamber	Static	Static

**Table 11.** Specification of voltage considered for testing the sample.

Sl.no	Microbes identified	Sample-raw water (Municipality water collected from kitchen)		
		Before treatment	Treated under 360 V pulsed DC	Treated under 5000 V pulsed DC
1	Coliform bacteria	10 cfu/gm	02 cfu/gm	Absent
2	Staphylococcus aureus/gm	06 cfu/gm	Absent	Absent
3	Salmonella	02 cfu/gm	Absent	Absent
4	Escherichia coli	08 cfu/gm	Absent	Absent

**Table 12.** Microbes identified in the sample and the test results.

## Data availability

The datasets used and/or analysed during the current study available from the corresponding author on reasonable request.

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## Author contributions

S.P., D.N.J., J.S.M.A., L.A.: Conceptualization, Methodology, Software, Visualization, Investigation, Writing—Original draft preparation. P.V.: Data curation, Validation, Supervision, Resources, Writing—Review & Editing. M.B., L.P. and S.A.D.M.: Project administration, Supervision, Resources, Writing—Review & Editing.

## Competing interests

The authors declare no competing interests.

## Additional information

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